Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +3.97V
SCL, SDA, $\overline{RST}$.....-0.3V to +3.63V
All Other Pins to GND except
REG18 and REG274.....-0.3V to (V_{DD} + 0.5V)*
Continous Sink Current..... 20mA per pin, 50mA total
Continous Source Current..... 20mA per pin, 50mA total

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 27.8mW/°C above + 70°C) 2222.2mW
Operating Temperature Range.....-40ºC to +85ºC
Storage Temperature Range.....-55ºC to +125ºC
Lead Temperature (soldering, 10s) ..... …+300°C
Soldering Temperature (reflow)..... …+260°C

**Subject to not exceeding +3.97V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

40 TQFN

Package Code	T4055+2
Outline Number	**21-0140**
Land Pattern Number	**90-0016**

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Recommended Operating Conditions

(T_A = -40ºC to +85ºC, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Operating Voltage	V_{DD}	(Note 2)	2.85		3.63	V
Input Logic-High	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Logic-Low	V_{IL}		-0.3		0.3 x V_{DD}	V

DC Electrical Characteristics

(V_{DD} = 2.85V to 3.63V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CPU}	CPU mode, all analog disabled (Notes 3, 4)		7.25		mA
	$I_{FASTCOMP}$			2.5		
	$I_{SAMPLEHOLDS}$	Both sample/hold		1.5		
	I_{ADC}			2.5		
	I_{DACS}	Per channel (Note 5)		0.7		
Brownout Voltage	V_{BO}	Monitors V_{DD} (Note 2)		2.62		V
Brownout Hysteresis	V_{BOH}	Monitors V_{DD} (Note 2)		110		mV
1.8V Regulator Initial Voltage	V_{REG18}	(Note 2)	1.71	1.8	1.89	V
2.74V Regulator Initial Voltage	V_{REG270}	(Note 2)	2.68	2.74	2.80	V
Clock Frequencies	$f_{OSC-PERIPHERAL}$	T_A = +25°C (Note 6)		20		MHz
	$f_{MOSC-CORE}$	T_A = +25°C (Note 6)		10		
Clock Error	f_{ERR}	T_A = -40°C to +85°C			5	%
External Clock Input	f_{XCLK}		20		133	MHz
Voltage Range: GP[15:0], SHEN, DACPW[7:0], REFINA, REFINB	V_{RANGE}	(Note 2)	-0.3		V_{DD} + 0.3	V
Output Logic-Low: All Pins	V_{OL1}	I_{OL} = 4mA (Note 2)			0.4	V
Output Logic-High: All Pins Except GP2, GP3, SCL, SDA	V_{OH1}	I_{OH} = -4mA (Note 2)	V_{DD} - 0.5			V
Pullup Current: All Pins Except GP2, GP3, SCL, SDA	I_{PU1}	V_{PIN} = 0V		55		µA
GPIO Drive Strength, Extra Strong Outputs: GP0, GP1, MCS, PWM8, PWM9	R_{HISt}			9	22	Ω
	R_{LOSt}			8	22	
GPIO Drive Strength, Strong Outputs: MSDI, DACPW3, DACPW6	R_{HIA}			17	32	Ω
	R_{LOA}			12	32	
GPIO Drive Strength, Excluding Strong GPIO Outputs	R_{HIB}			27	46	Ω
	R_{LOB}			31	52	
DAC						
DAC Resolution	DAC_R		12			Bits
DAC Internal Reference Accuracy	DAC_{REFACC}	(Note 5)	-1.25		+1.25	%
DAC Internal Reference Power-Up Speed	t_{DACPUP}	99% settled		10		µs
Reference Input Full-Scale Range (REFINA, REFINB)	REFFS		1		2.5	V

DC Electrical Characteristics (continued)

(V_{DD} = 2.85V to 3.63V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC Operating Current	I_{DACS}	Per channel	See the *DC Electrical Characteristics*			mA
DAC Integral Nonlinearity	DACINL	(Note 5)		5		LSB
DAC Differential Nonlinearity	DACDNL	Not production tested (Notes 5, 7)			±1	LSB
DAC Offset	$V_{OFFSET-DAC}$	At code “0”	0		18	mV
DAC Source Load Regulation	$I_{DAC-SOURCE}$	0 to full-scale output, V_{DD} = 3.3V			3	mV/mA
DAC Sink Capability and Sink Load Regulation	$R_{DAC-SINK}$	0 to 0.5V output, limited by output buffer impedance		500		Ω
	$I_{DAC-SINK}$	0.5V to full-scale output			5	mV/mA
DAC Settling Time	t_{DAC}	Output load capacitance between 33pF to 270pF, from 10% to 90%		10		µs
FAST COMPARATOR						
Fast Comparator Resolution	FC_R		10			Bits
Fast Comparator Internal Reference Accuracy	FC_{REFTC}			±0.2		%
Fast Comparator Operating Current	$I_{FASTCOMP}$		See the *DC Electrical Characteristics*			mA
Fast Comparator Full Scale	$V_{FS-COMP}$	T_A = +25°C		2.42		V
Fast Comparator Integral Nonlinearity	INL	Differential mode, 2.2nF capacitor at input (Note 7)		±2		LSB
Fast Comparator Differential Nonlinearity	DNL	Differential mode, 2.2nF capacitor at input (Note 8)		±0.5		LSB
Fast Comparator Offset	$V_{OFFSET-COMP}$			±2		LSB
Fast Comparator Input Impedance	$R_{IN-COMP}$			15		MΩ
Fast Comparator Input Capacitance	$C_{IN-COMP}$			4		pF
Fast Comparator Sample Rate	f_{COMP}			625		ksps
ADC						
ADC Resolution	ADC_R	V_{FS} ≥ 1.2V (Note 9)	13			Bits
ADC Internal Reference Accuracy	ADC_{REFACC}		-0.85		+0.85	%
Reference Output Accuracy	REFOUT	10kΩ < REFOUT load, C_{MAX}= 2.2nF	1.214	1.225	1.236	V
ADC Operating Current	I_{ADC}		See the *DC Electrical Characteristics*			mA
ADC Full-Scale 1	$V_{FS-ADC1}$	Factory calibrated		1.2		V
ADC Full-Scale 2	$V_{FS-ADC2}$	Factory calibrated		0.6		V
ADC Full-Scale 3	$V_{FS-ADC3}$	Factory calibrated		2.4		V

DC Electrical Characteristics (continued)

(V_{DD} = 2.85V to 3.63V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Full-Scale 4	$V_{FS-ADC4}$	Factory calibrated		6.55		V
ADC Integral Nonlinearity	ADCINL	13-bit, T_A = +25°C, V_{DD} = 3.3V, $V_{FS-ADC3}$ (Note 10)		±3		LSB
ADC Differential Nonlinearity	ADCDNL	V_{FS} ≥ 1.2V		±0.5		LSB
ADC Sample-Sample Deviation		ADC full scale set to $V_{FS-ADC3}$		±2		LSB
ADC Offset	$V_{OFFSET-ADC}$	13-bit, V_{FS} ≥ 1.2V	-8	+1	+8	LSB
ADC[15:0] Input Resistance	R_{IN-ADC}			15		MΩ
ADC Sample Rate	f_{SAMPLE}	(Note 11)		40		ksps
ADC Temperature Conversion Time	t_{TEMP}	With default ADC clock		41		µs
Internal Temperature Measurement Error	$TINT_{ERR}$	(Note 12)		±2		°C
SAMPLE/HOLD						
Sample/Hold Input Range	V_{SHP}	ADC-SHN[1:0] = GND			1	V
Sample/Hold Capacitance	C_{SH}	ADC-SHP[1:0] to ADC-SHN[1:0]		5		pF
Sample Input Leakage	I_{SHLKG}	ADC-SHP[1:0] and ADC-SHN[1:0]			1.2	µA
Sample Time	t_s	ADC-SHP[1:0] and ADC-SHN[1:0] connected to 50Ω voltage source	300			ns
Sample Conversion Complete	t_h	(Note 13)			320	µs
Sample Offset	V_{SH-OFF}	Measured at 10mV	-10	-1.6	7	mV
Sample Error	ERR_{SH}	VADC-SHP_ to VADC-SHN_ = 300mV, ts = 300ns, driven with 50Ω voltage source	-4		+4	%
Sample Discharge Strength	R_{DIS}	ADC-SHP[1:0] or ADC-SHN[1:0] to GND		50		Ω
FLASH MEMORY						
Flash Erase Time (Note 14)	t_{ME}	Mass erase		25		ms
	t_{PE}	Page erase		25		
Flash Programming Time per Word	t_{PROG}	(Notes 14, 15)		75		µs
Flash Programming Temperature	T_{FLASH}		-40		+85	°C
Flash Endurance	n_{FLASH}	T_A = +50°C (Note 7)	20,000			Write Cycles
Data Retention	t_{RET}	T_A = +50°C (Note 7)	100			Years

AC Electrical Characteristics

(V_{DD} = 2.85V to 3.63V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C COMPATIBLE INTERFACE (See Figure 1)						
SCL/MSCL Clock Frequency	f_{SCL}	Timeout not enabled			400	kHz
SCL Bootloader Clock Frequency	$f_{SCL:BOOT}$				100	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 16)	0.6			µs
Low Period of SCL/MSCL Clock	t_{LOW}		1.3			µs
High Period of SCL/MSCL Clock	t_{HIGH}		0.6			µs
Setup Time for a (Repeated) START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time (Note 17)	$t_{HD:DAT}$	Receive	0			ns
		Transmit	300			
Data Setup Time	$t_{SU:DAT}$		100			ns
SCL/MSCL, SDA/MSDA Capacitive Loading	C_B	(Note 18)			400	pF
Rise Time of Both SDA and SCL Signals	t_R	(Note 18)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 18)	20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Width That Can Be Suppressed by Input Filter	t_{SP}	(Note 19)		50		ns
SCL/MSCL and SDA/MSDA Input Capacitance	C_{BIN}			5		pF
SMBusTimeout	t_{SMBUS}			30		ms
JTAG INTERFACE (See Figure 2)						
JTAG Logic Reference	V_{REF}			$V_{DD}/2$		V
TCK High Time	t_{TH}			0.5		µs
TCK Low Time	t_{TL}			0.5		µs
TCK Low to TDO Output	t_{TLQ}			0.125		µs
TMS, TDI Input Setup to TCK High	t_{DVTH}			0.25		µs
TMS, TDI Input Hold after TCK High	t_{THDX}			0.25		µs

AC Electrical Characteristics (continued)

(V_{DD} = 2.85V to 3.63V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3-WIRE DIGITAL INTERFACE (See Figure 3)						
MSCL Clock Frequency	f_{SCLOUT}			1000		kHz
MSCL Duty Cycle	t_{3WDC}			50		%
MSDIO Setup Time	t_{DS}			100		ns
MSDIO Hold Time	t_{DH}			100		ns
MCS Pulse-Width Low	t_{CSW}			500		ns
MCS Leading Time Before the First MSCL Edge	t_L			500		ns
MCS Trailing Time After the Last MSCL Edge	t_T			500		ns
MSDIO, MSCL Load	C_{B3W}	Total bus capacitance on one line		10		pF
SPI DIGITAL INTERFACE SPECIFICATION (See Figure 4 and Figure 5)						
SPI Master Operating Frequency	$1/t_{MSPICK}$	(Note 14)			5	MHz
SPI Slave Operating Frequency	$1/t_{SSPICK}$	(Note 14)			2.5	MHz
SPI I/O Rise/Fall Time	t_{SPI_RF}	C_L = 15pF, pullup = 560Ω			25	ns
MSPICK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MSPICK}/2$ - t_{SPI_RF}			ns
MSPIDO Output Hold After MSPICK Sample Edge	t_{MOH}		$t_{MSPICK}/2$ - t_{SPI_RF}			ns
MSPIDO Output Valid to MSPICK Sample Edge (MSPIDO Setup)	t_{MOV}		$t_{MSPICK}/2$ - t_{SPI_RF}			ns
MSPIDI Input Valid to MSPICK Sample Edge (MSPIDI Setup)	t_{MIS}		$2t_{SPI\_RF}$			ns
MSPIDI Input to MSPICK Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
MSPICK Inactive to MSPIDO Inactive	t_{MLH}		$t_{MSPICK}/2$ - t_{SPI_RF}			ns
SSPICK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}		$t_{SSPICK}/2$			ns
SSPICS Active to First Shift Edge	t_{SSE}		t_{SPI_RF}			ns
SSPIDI Input to SSPICK Sample Edge Rise/Fall Setup	t_{SIS}		t_{SPI_RF}			ns

AC Electrical Characteristics (continued)

(V_{DD} = 2.85V to 3.63V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SSPIDI Input from SSPICK Sample Edge Transition Hold	t_{SIH}		t_{SPI_RF}			ns
SSPIDO Output Valid After SSPICK Shift Edge Transition	t_{SOV}				$2t_{SPI\_RF}$	ns
SSPICS Inactive	t_{SSH}		t_{SSPICK} + t_{SPI_RF}			ns
SSPICK Inactive to SSPICS Rising	t_{SD}		t_{SPI_RF}			ns
SSPIDO Output Disabled After SSPICS Edge Rise	t_{SLH}				$2t_{SSPICK}$ + $2t_{SPI\_RF}$	ns

Note 1: Limits are 100% production test at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
Note 2: All voltages referenced to GND. Currents entering the IC are specified positive and currents exiting the IC are negative.
Note 3: Maximum current assuming 100% CPU duty cycle.
Note 4: The value does not include current in GPIO, SCL, SDA, MSDIO, MSDI, MSCL, REFINA, and REFINB.
Note 5: Using 2.5V internal reference.
Note 6: There is one internal oscillator. The oscillator (peripheral clock) goes through a 2:1 divider to create the core clock.
Note 7: Guaranteed by design.
Note 8: Tested at worse-case positions.
Note 9: Default or slower ADC clock settings.
Note 10: Computed using end-point best fit and histogram method.
Note 11: ADC conversions are delayed up to 1.6µs if the fast comparator is sampling the selected ADC channel. This can cause a slight decrease in the ADC sampling rate.
Note 12: Temperature readings averaged 64 times.
Note 13: Time from valid sample to ADC data available (without any averaging).
Note 14: Minimum and maximum timings depend upon $f_{MOSC-CORE}$ error.
Note 15: Programming does not include overhead associated with the utility ROM interface.
Note 16: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 17: This device internally provides a hold time of at least 75ns for the SDA signal (referred to the $V_{IH:MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 18: C_B—total capacitance of one bus line in pF.
Note 19: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Timing Diagrams

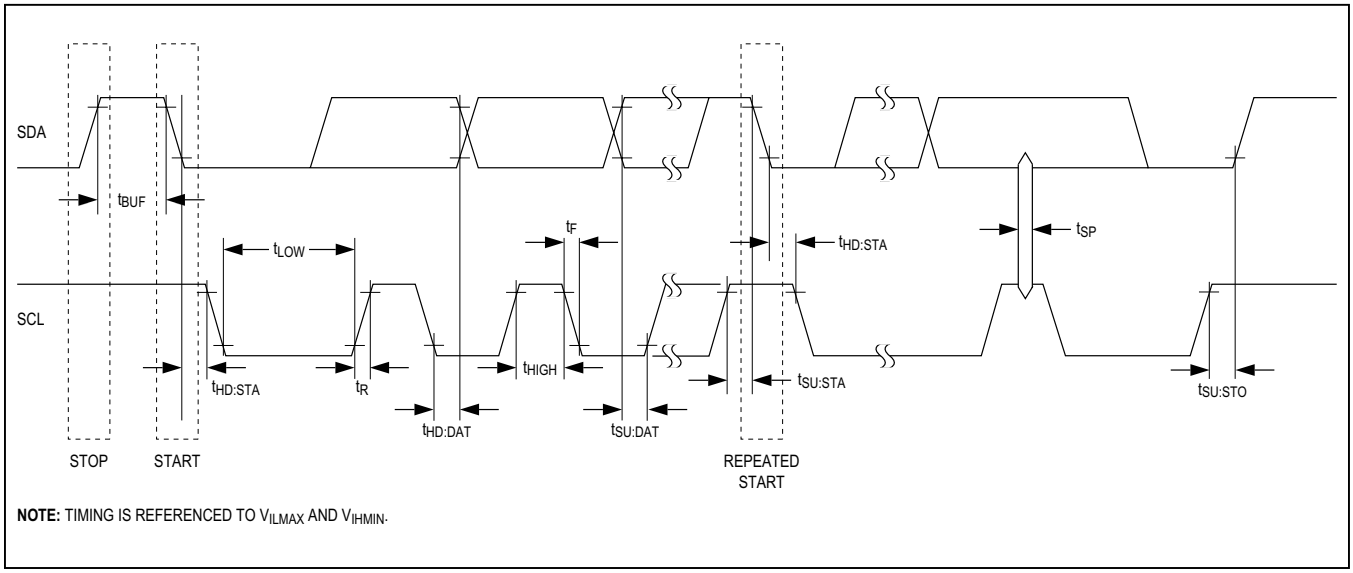


Figure 1. I²C Timing Diagram

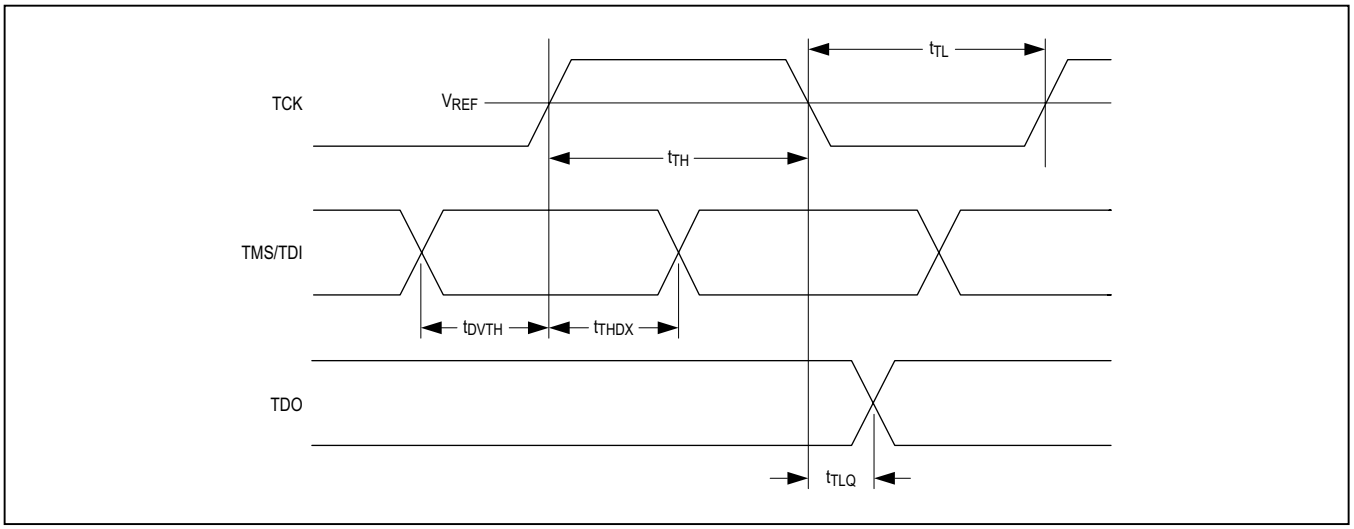


Figure 2. JTAG Timing Diagram

Timing Diagrams (continued)

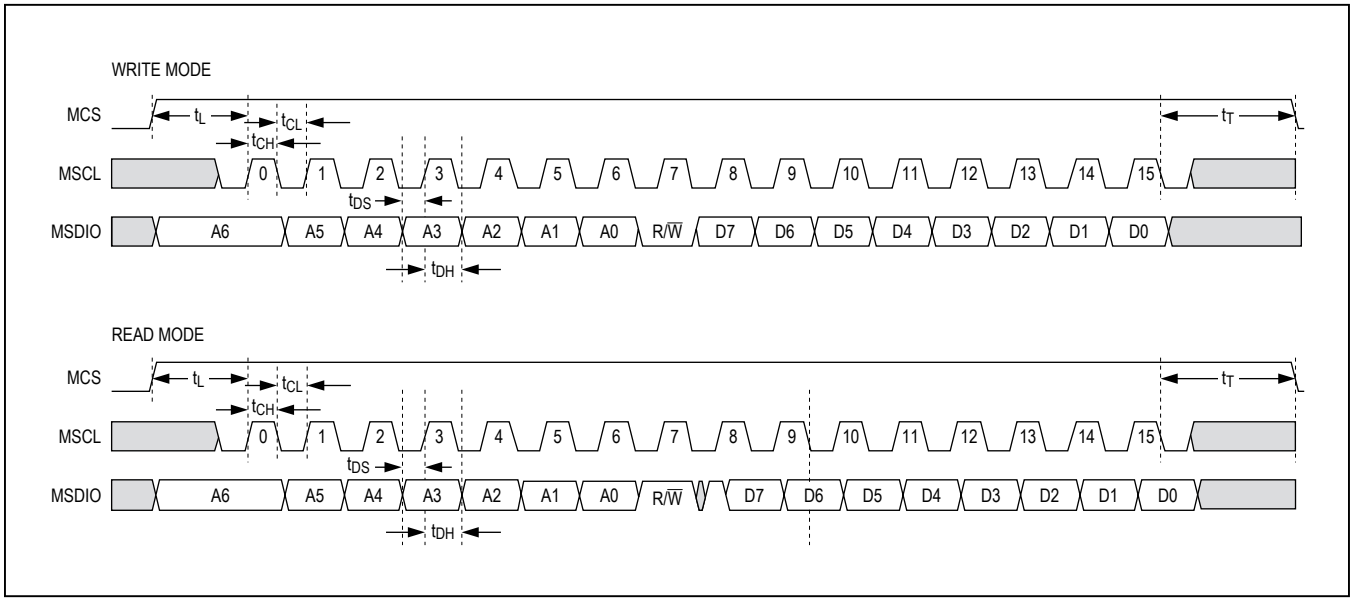


Figure 3. 3-Wire Timing Diagram

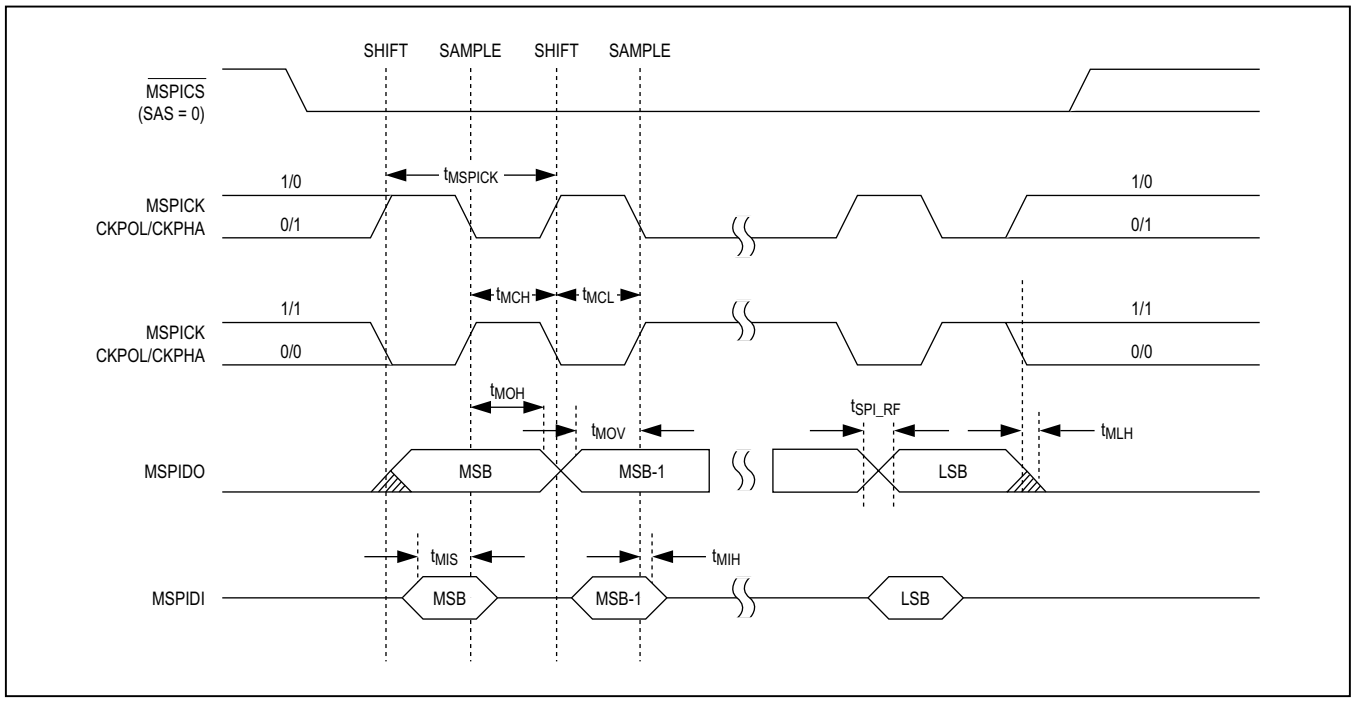


Figure 4. SPI Master Communications Timing Diagram

Timing Diagrams (continued)

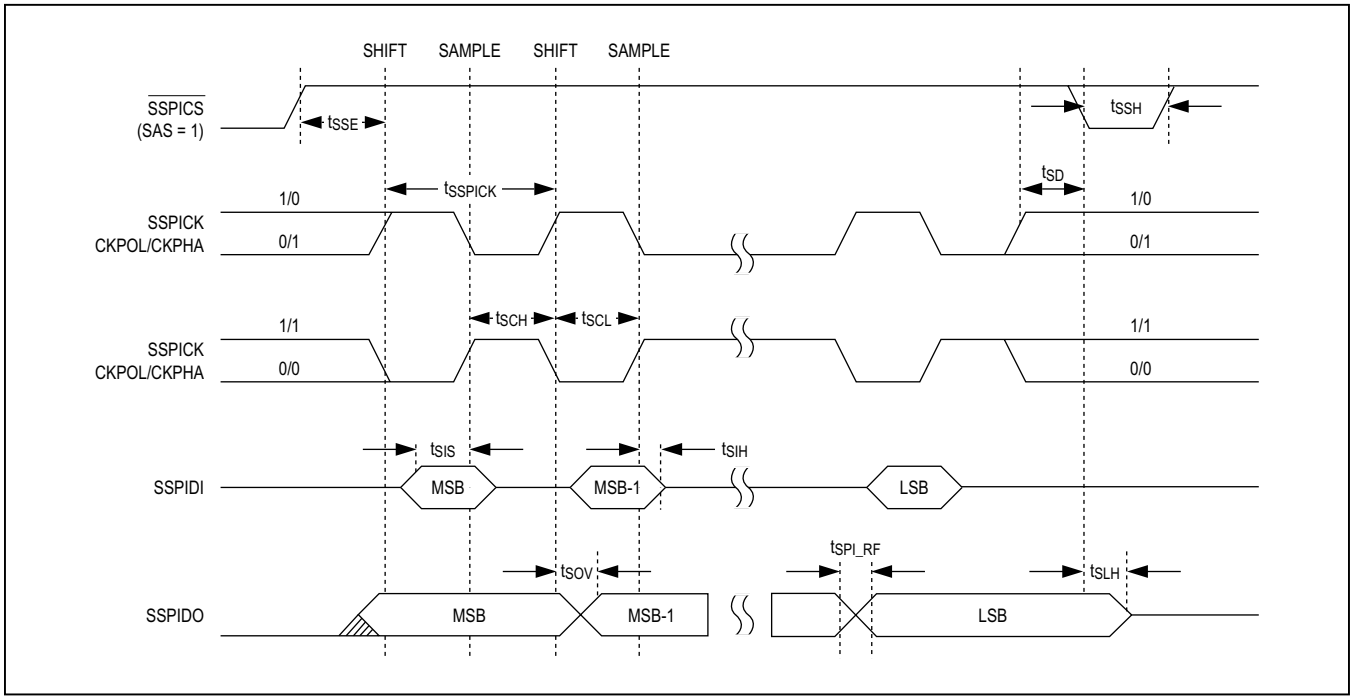
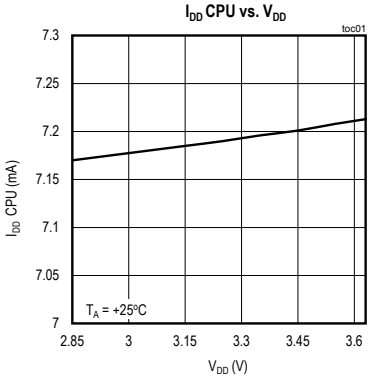


Figure 5. SPI Slave Communications Timing Diagram

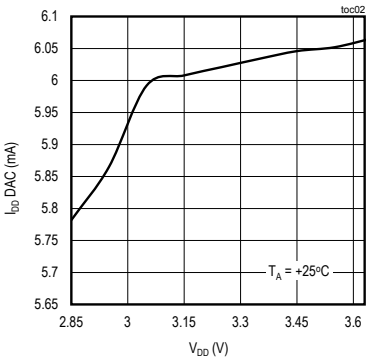
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

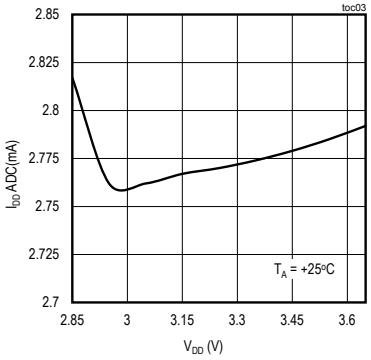
I_{DD} CPU vs. V_{DD}



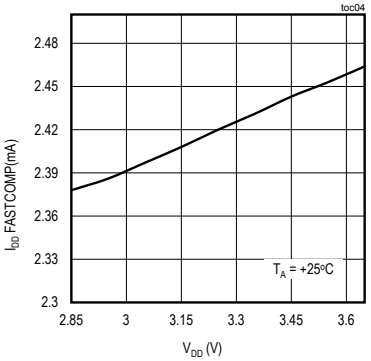
I_{DD}DAC vs. V_{DD}



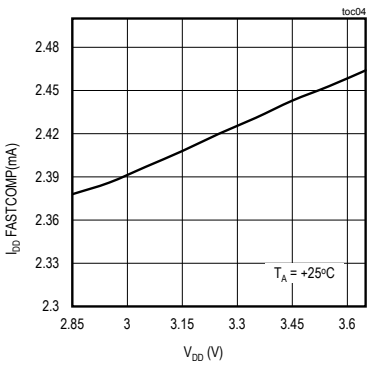
I_{DD} ADC vs. V_{DD}



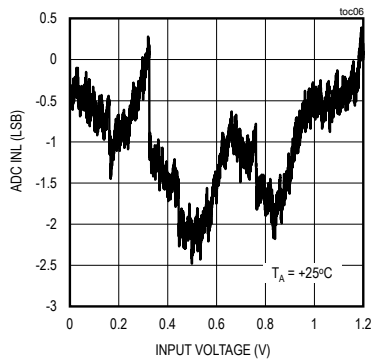
I_{DD} FASTCOMP vs. V_{DD}



I_{DD} FASTCOMP vs. V_{DD}

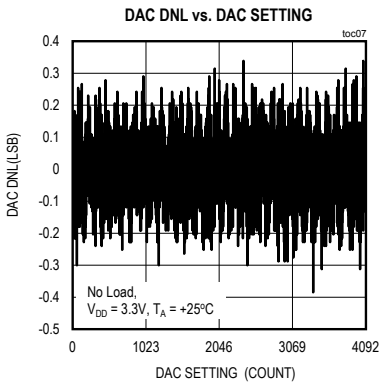


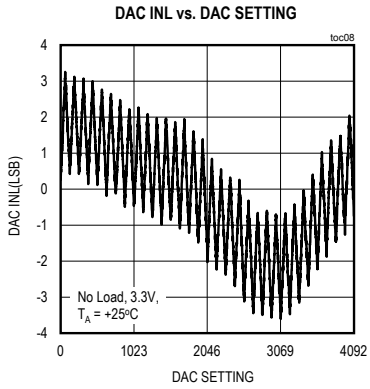
ADC INL vs. INPUT VOLTAGE

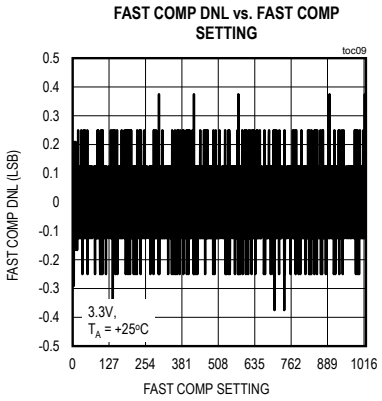


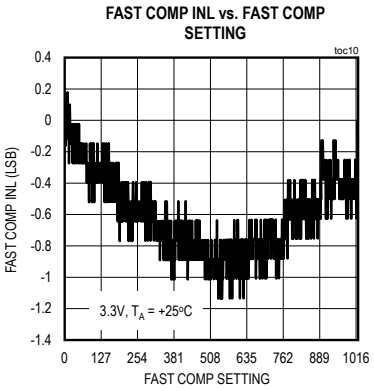
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

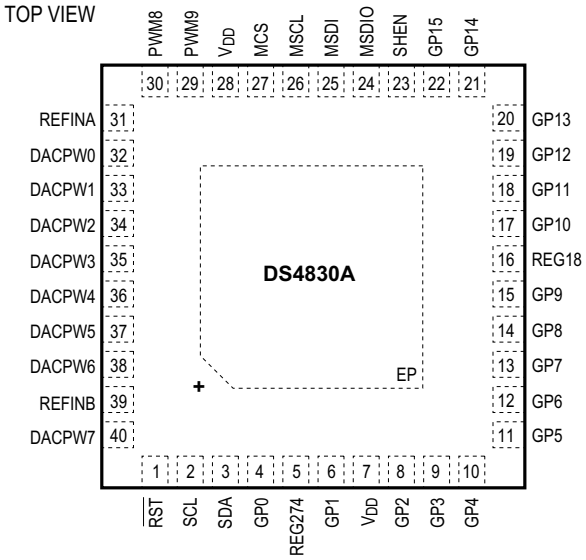








Pin Configuration



TQFN
(5mm x 5mm)

Pin Description

PIN	NAME	INPUT STRUCTURE(S)	OUTPUT STRUCTURE	POWER-ON STATE	SELECTABLE FUNCTIONS (FIRST COLUMN IS DEFAULT FUNCTION)				PORT
1	$\overline{RST}$	Digital	None	High Impedance	$\overline{RST}$	—	—	—	—
2	SCL	Digital	Open Drain	High Impedance	I^2C Slave Clock SCL	SPI SSPICK	—	—	—
3	SDA	Digital	Open Drain	High Impedance	I^2C Slave Data SDA	SPI SSPIDI	—	—	—
4	GP0	ADC/Digital Input	Push-Pull, Extra Strong	55µA Pullup	ADC-S0	ADC-D0P	PWM-ALT0	—	P2.0
5	REG274	V_{REG}	None	2.74V	Only function is for bypass capacitors for 2.74V internal regulator				—
6	GP1	ADC/Digital Input	Push-Pull, Extra Strong	55µA Pullup	ADC-S1	ADC-D0N	PWM-ALT1	REFOUT	P2.1
7	V_{DD}	Voltage Supply, ADC Input	None	V_{DD}	ADC-VDD	—	—	—	—
8	GP2	SH Input, ADC Input	None	High Impedance	ADC-S2	ADC-SHP0	ADC-D1P	—	—
9	GP3	SH Input, ADC Input	None	High Impedance	ADC-S3	ADC-SHN0	ADC-D1N	—	—

Pin Description (continued)

PIN	NAME	INPUT STRUCTURE(S)	OUTPUT STRUCTURE	POWER-ON STATE	SELECTABLE FUNCTIONS (FIRST COLUMN IS DEFAULT FUNCTION)				PORT
10	GP4	ADC/Digital Input	Push-Pull	55µA Pullup	JTAG TCK	ADC-S4	ADC-D2P	—	P6.0
11	GP5	ADC/Digital Input	Push-Pull	55µA Pullup	JTAG TDI	ADC-S5	ADC-D2N	—	P6.1
12	GP6	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S6	ADC-D3P	PWM2	SPI SSPIDO	P2.2
13	GP7	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S7	ADC-D3N	PWM3	SPI SSPICS	P2.3
14	GP8	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S8	ADC-D4P	—	—	P2.4
15	GP9	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S9	ADC-D4N	—	—	P2.5
16	REG18	V_{REG}	None	1.8V	Pin for 1.8V regulator bypass capacitor				—
17	GP10	ADC/Digital Input	Push-Pull	55µA Pullup	JTAG TMS	ADC-S10	ADC-D5P	—	P6.2
18	GP11	ADC/Digital Input	Push-Pull	55µA Pullup	JTAG TDO	ADC-S11	ADC-D5N	—	P6.3
19	GP12	SH Input, ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S12	ADC-SHP1	ADC-D6P	—	P0.0
20	GP13	SH Input, ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S13	ADC-SHN1	ADC-D6N	—	P0.1
21	GP14	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S14	ADC-D7P	SHEN1	—	P0.2
22	GP15	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S15	ADC-D7N	—	—	P0.3
23	SHEN	Digital	Push-Pull	55µA Pullup	SHEN0	—	—	—	P6.4
24	MSDIO	Digital	Push-Pull	55µA Pullup	3-Wire Data MSDIO	I^2C MSDA	SPI MSPIDO	PWM-ALT4	P1.0
25	MSDI	Digital	Push-Pull, Strong	55µA Pullup	—	—	SPI MSPIDI	PWM-ALT5	P1.3
26	MSCL	Digital	Push-Pull	55µA Pullup	3-Wire Clock MSCL	I^2C MSCL	SPI MSPICK	PWM-ALT6	P1.1
27	MCS	Digital	Push-Pull, Extra Strong	55µA Pullup	3-Wire Chip Select MCS	—	SPI MSPICS	PWM-ALT7	P1.2
28	V_{DD}	Voltage Supply	None	V_{DD}	ADC-VDD	—	—	—	—
29	PWM9	Digital	Push-Pull, Extra Strong	55µA Pullup	PWM9	—	—	—	P0.7
30	PWM8	Digital	Push-Pull, Extra Strong	55µA Pullup	PWM8	—	—	—	P0.6
31	REFINA	Reference, ADC/Digital Input	Push-Pull	55µA Pullup	ADC-REFINA	—	—	—	P2.6

Pin Description (continued)

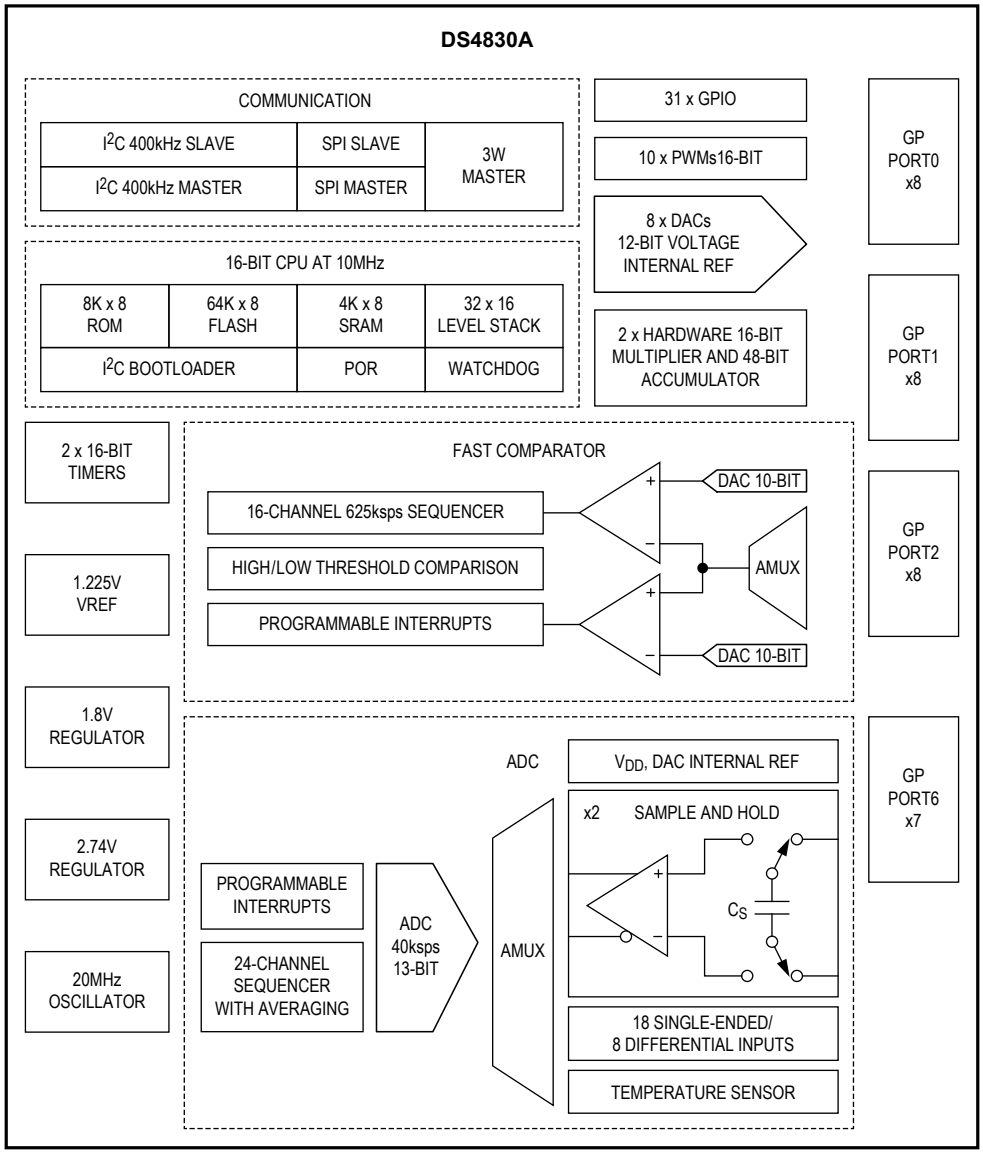
PIN	NAME	INPUT STRUCTURE(S)	OUTPUT STRUCTURE	POWER-ON STATE	SELECTABLE FUNCTIONS (FIRST COLUMN IS DEFAULT FUNCTION)				PORT
32	DACPW0	Digital	Push-Pull	High Impedance	DAC0, FS = REFINA or Internal Reference	PWM0	—	—	P0.4
33	DACPW1	Digital	Push-Pull	High Impedance	DAC1, FS = REFINA or Internal Reference	PWM1	—	—	P0.5
34	DACPW2	Digital	Push-Pull	High Impedance	DAC2, FS = REFINA or Internal Reference	PWM2	CLKIN	—	P6.5
35	DACPW3	Digital	Push-Pull, Strong	High Impedance	DAC3, FS = REFINA or Internal Reference	PWM3	—	—	P1.5
36	DACPW4	Digital	Push-Pull	High Impedance	DAC4, FS = REFINB or Internal Reference	PWM4	I^2C MSDA-ALT	—	P1.6
37	DACPW5	Digital	Push-Pull	High Impedance	DAC5, FS = REFINB or Internal Reference	PWM5	I^2C MSCL-ALT	—	P1.7
38	DACPW6	Digital	Push-Pull, Strong	High Impedance	DAC6, FS = REFINB or Internal Reference	PWM6	—	—	P6.6
39	REFINB	Reference, ADC/ Digital Input	Push-Pull	55µA Pullup	ADC-REFINB	—	—	—	P1.4
40	DACPW7	Digital	Push-Pull	High Impedance	DAC7, FS = REFINB or Internal Reference	PWM7	—	—	P2.7
—	EP	Exposed Pad (Connect to GND)	—	GND	—	—	—	—	—

Note: *Bypass V_{DD}, REG274, and REG18 each with 1µF X5R and 10nF capacitors to ground. All input-only pins and open-drain outputs are high impedance after V_{DD} exceeds V_{BO} and prior to code execution. Except for pins having DAC functions, pins configured as GPIO have a weak internal pullup at power-up. See the Selectable Functions table for more information.*

Selectable Functions

FUNCTION NAME	DESCRIPTION
ADC-D[7:0][P/N]	Differential Inputs to ADC. Also used for sample/hold inputs.
ADC-REFIN[A/B]	REFINA and REFINB Monitor Inputs to ADC
ADC-S[15:0]	Single-Ended Inputs to ADC
ADC-SH[P/N][1:0]	Sample/Hold Inputs 1 and 0
ADC-VDD	V_{DD} Monitor Input to ADC
DAC[7:0]	Voltage DAC Outputs
MSCL, MCS, MSDIO	Maxim Proprietary 3-Wire Interface: MSCL (3-Wire Master Clock), MCS (Chip Select), MSDIO (3-Wire Data). Used to control the Maxim family of high-speed laser drivers.
MSCL, MSDA	I^2C Master Interface: MSCL (I^2C Master Clock), MSDA (I^2C Master Data)
MSCL-ALT, MSDA-ALT	I^2C Master Interface: MSCL-ALT (I^2C Master Clock), MSDA (I^2C Master Data)
MSPICK, MSPICS, MSPIDI, MSPIDO	SPI Master Interface: MSPICK (SPI Master Clock), MSPICS (Chip Select), MSPIDI (Master Data In), MSPIDO (Master Data Out)
P0.n, P1.n, P2.n, P6.n	General-Purpose Inputs/Outputs. Can also function as edge interrupts.
PWM[9:0]	PWM Outputs
PWM-ALT[9:0]	PWM Alternate Outputs
$\overline{RST}$	Used by JTAG and as Active-Low Reset for Device
SCL, SDA	I^2C Slave Interface: SCL (I^2C Slave Clock), SDA (I^2C Slave Data). These also function as a password-protected programming interface.
SHEN[1:0]	Sample/Hold Trigger Inputs
SSPICK, SSPICS, SSPIDI, SSPIDO	SPI Slave Interface: SSPICK (Clock), SSPICS (Chip Select), SSPIDI (Data In), SSPIDO (Data Out). In SPI slave mode, the I^2C slave interface is disabled.
TCK, TDI, TDO, TMS	JTAG Interface Pins. Also includes $\overline{RST}$.
REFOUT	ADC Internal Reference Output

Block Diagram



Detailed Description

The following is an introduction to the primary features of the DS4830A optical microcontroller. More detailed descriptions of the device features can be found in the DS4830A User's Guide.

Core Architecture

The device employs a low-power, low-cost, high-performance, 16-bit RISC microcontroller with on-chip flash memory. It is structured on an advanced, 16 accumulator-based, 16-bit RISC architecture. Fetch and execution operations are completed in one cycle without pipelining, since the instruction contains both the op code and data. The highly efficient core is supported by 16 accumulators and a 32-level hardware stack, enabling fast subroutine calling and task switching. Data can be quickly and efficiently manipulated with three internal data pointers. Multiple data pointers allow more than one function to access data memory without having to save and restore data pointers each time. The data pointers can automatically increment or decrement following an operation, eliminating the need for software intervention.

Module Information

Top-level instruction decoding is extremely simple and based on transfers to and from registers. The registers are organized into functional modules, which are in turn divided into the system register and peripheral register groups.

Peripherals and other features are accessed through peripheral registers. These registers reside in modules 0–5. The following provides information about the specific module that each peripheral resides in:

Module 0: Timer 1, GPIO Ports 0, 1, and 2

Module 1: I2C Master, GPIO Port 6, Supply Voltage Monitor

Module 2: I2C Slave

Module 3: Timer 2, MAC-Related Registers, Software Interrupt and General-Purpose Registers

Module 4: ADC, Sample/Hold, Internal Temperature, 3-Wire Master, SPI Slave, DAC

Module 5: Quick Trips, SPI Master, PWM

Instruction Set

The instruction set is composed of fixed-length, 16-bit instructions that operate on registers and memory locations. The instruction set is highly orthogonal, allowing arithmetic and logical operations to use any register along with the accumulator. Special-function registers control the peripherals and are subdivided into register modules.

Memory Organization

The device incorporates several memory areas:

- 32KWords of flash memory for application program and constant data storage
- 2KWords of SRAM
- 4KWords of utility ROM contain a debugger and program loader
- 32-level stack memory for storage of program return addresses and application use

The memory is implemented with separate address spaces for program memory, data memory and register space which also allows ROM, application code, and data memory into a single contiguous memory map. The device allows data memory to be mapped into program space, permitting code execution from data memory. In addition program memory may be mapped into data space, permitting code constants to be accessed as data memory. Figure 6 shows the DS4830A's memory map when executing from program memory space. Refer to the DS4830A User's Guide for memory map information when executing from data or ROM space.

The incorporation of flash memory allows field upgrade of the firmware. Flash memory can be password protected with a 16-word key, denying access to program memory by unauthorized individuals.

Utility ROM

The utility ROM is a 4KWord block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software, which include the following:

- In-system programming (bootstrap loader) over JTAG or I2C-compatible interfaces
- Callable routines for in-application flash programming

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of application code, or to one of the special routines mentioned. Routines within the utility ROM are firmware-accessible and can be called as subroutines by the application software. More information on the utility ROM contents is contained in the DS4830A User's Guide.

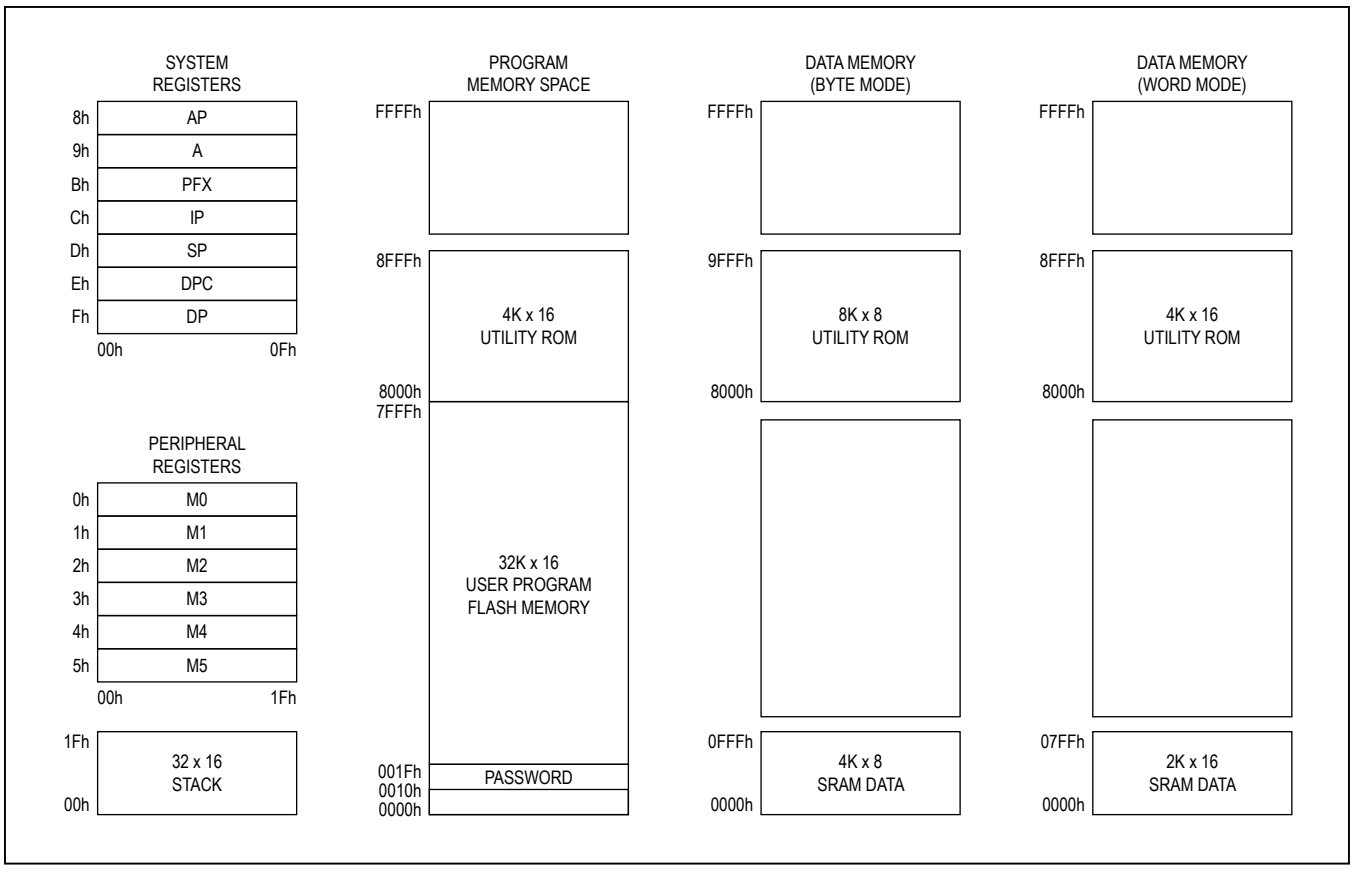


Figure 6. Memory Map When Program Is Executing from Flash Memory

Password

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h–001Fh.

A single password lock (PWL) bit is implemented in the device. When the PWL is set to 1 (power-on reset default) and the contents of the memory at addresses 0010h–001Fh are any value other than all FFh or 00h, the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to 0, these utilities are fully accessible without the password. The password is automatically set to all ones following a mass erase. Mass erase can be performed without password match.

Detailed information regarding the password can be found in the DS4830A User's Guide.

Stack Memory

A 16-bit, 32-level internal stack provides storage for program return addresses. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced. The stack can also be used explicitly to store and retrieve data by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (1Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then decrement SP.

Programming

The microcontroller's flash memory can be programmed by one of two methods: in-system programming and in-application programming. These provide great flexibility in system design as well as reduce the life-cycle cost of the embedded system. Programming can be password protected to prevent unauthorized access to code memory.

In-System Programming

An internal bootstrap loader allows the device to be programmed over the JTAG or I²C compatible interfaces. As a result, system software can be upgraded in-system, eliminating the need for a costly hardware retrofit when software updates are required.

The programming source select (PSS) bits in the ICDF register determine which interface is used for boot loading operation. The device supports JTAG and I²C as an interface corresponding to 00 and 01 bits of PSS, respectively as shown in Figure 7.

In-Application Programming

The in-application programming feature allows the microcontroller to modify its own flash program memory. This allows on-the-fly software updates in mission-critical applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains firmware-accessible flash programming functions that erase and program flash memory. These functions are described in detail in the DS4830A User's Guide.

Register Set

Sets of registers control most device functions. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types: system registers (special purpose registers, or SPRs) and peripheral registers (special function registers, or SFRs). The system registers includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality and the functionality is broken up into discrete modules. Both the system registers and the peripheral registers are described in detail in the DS4830A User's Guide.

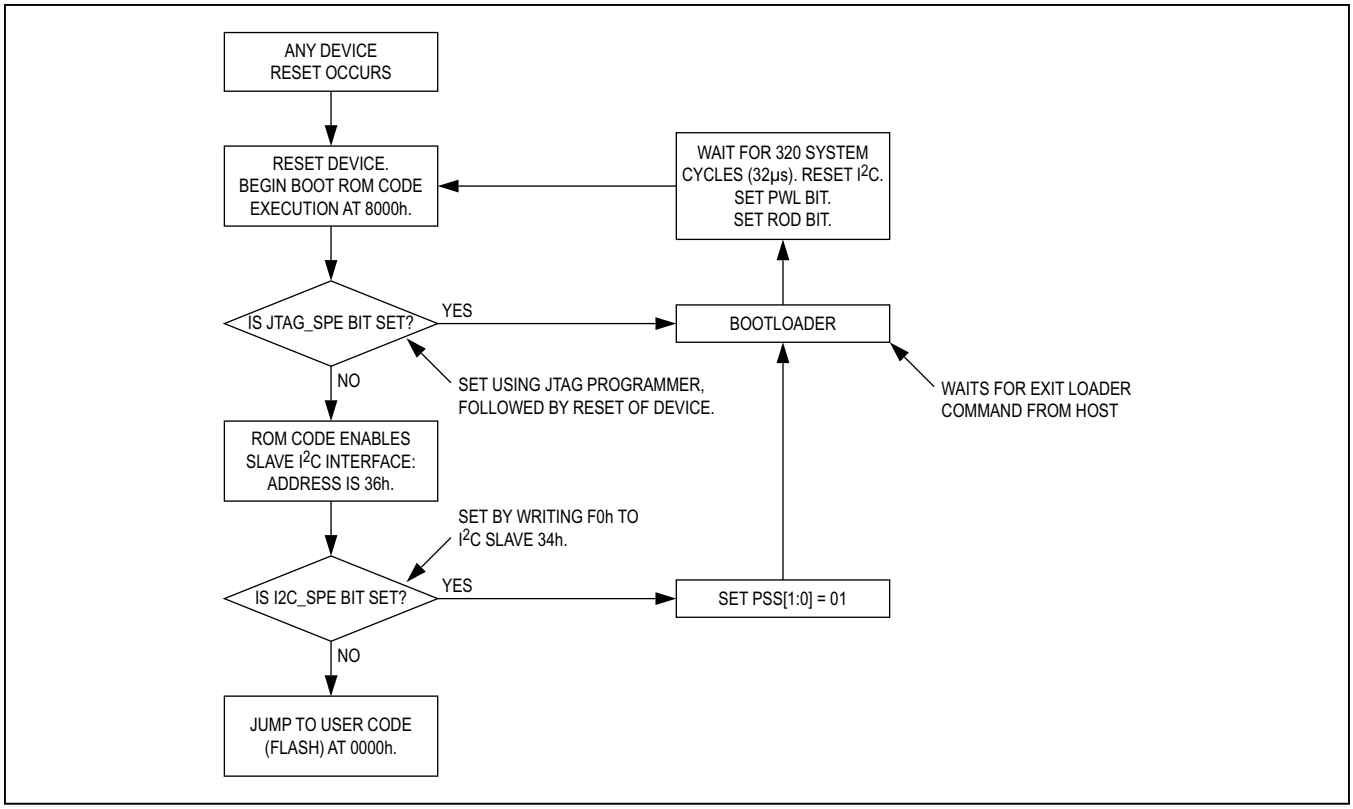


Figure 7. In-System Programming

System Timing

The device generates its 10MHz instruction clock (MOSC) and 20MHz peripheral clock internally. On power-up, oscillator's output (which cannot be accessed externally) is disabled until V_{DD} rises above V_{BO}. Once this threshold is reached, the output is enabled after approximately 1ms ($t_{SU:MOSC}$), clocking the device as shown in Figure 8.

System Reset

The device features several sources that can be used to reset the DS4830A. The DAC and PWM outputs are maintained during execution of all resets except POR.

Power-On Reset

An internal power-on reset (POR) circuit is used to enhance system reliability. This circuit forces the device to perform a POR whenever a rising voltage on V_{DD} climbs above V_{BO}. When this happens the following events occur:

- All registers and circuits enter their reset state.
- The POR flag (WDCN.7) is set to indicate the source of the reset.
- Code execution begins at location 8000h when the reset condition is released.

Brownout Detect/Reset

The device features a brownout detect/reset function. Whenever the power monitor detects a brown-out condition (when $V_{DD} < V_{BO}$), it immediately issues a reset and stays in that state as long as V_{DD} remains below V_{BO}. Once V_{DD} voltage rises above V_{BO}, the device waits for $t_{SU:MOSC}$ before returning to normal operation, also referred to as CPU state. If a brownout occurs during this $t_{SU:MOSC}$, the device again goes back to the brownout state. Otherwise, it enters into CPU state. In CPU state, the brownout detector is also enabled.

On power-up, the device always enters brownout state first and then follows the above sequence. The reset issued by brownout is same as POR. Any action performed after POR also happens on brownout reset. All the registers that are cleared on POR are also cleared on brownout reset.

External Reset

Asserting the $\overline{RST}$ pin low causes the device to enter the reset state. Execution resumes at location 8000h after $\overline{RST}$ is released.

Watchdog Timer Reset

The watchdog timer provides a mechanism to reset the processor in the case of undesirable code execution. The watchdog timer is a hardware timer designed to be periodically reset by the application software. If the software operates correctly, the timer is reset before it reaches its maximum count. However, if undesirable code execution prevents a reset of the watchdog timer, the timer reaches its maximum count and resets the processor.

The watchdog timer is controlled through 2 bits in the WDCN register (WDCN[5:4] : WD[1:0]). Its timeout period can be set to one of the four programmable intervals ranging from 2^{12} to 2^{21} system clock (MOSC) periods (0.410ms to 0.210s). The watchdog interrupt occurs at the end of this timeout period, which is 512 MOSC clock periods, or approximately 50µs, before the reset. The reset generated by the watchdog timer lasts for 4 system clock cycles, which is 0.4µs. Software can determine if a reset is caused by a watchdog timeout by checking the watchdog timer reset flag (WTRF) in the WDCN register. Execution resumes at location 8000h following a watchdog timer reset. The watchdog reset has the same effect as the external reset as far as the reset values of all registers are concerned.

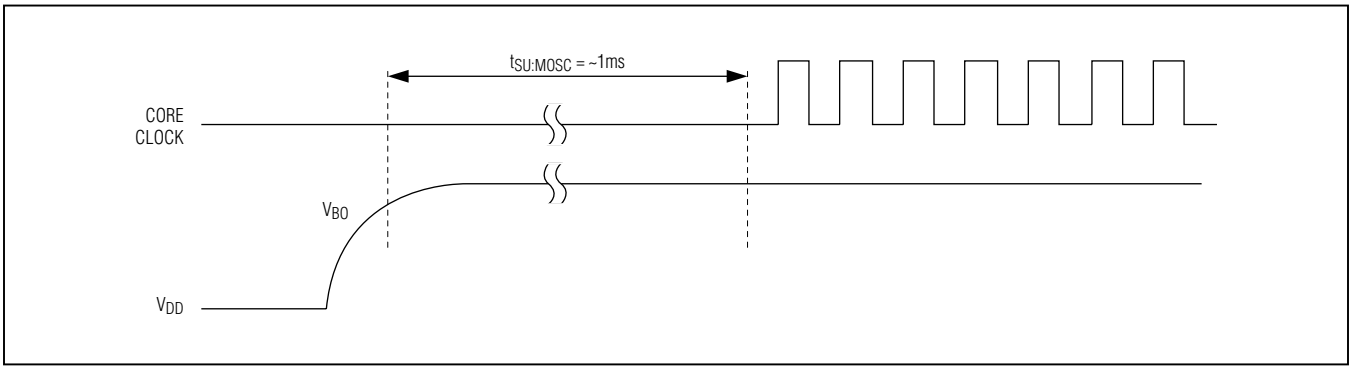


Figure 8. System Timing

Internal System Reset

The host can issue an I²C command (BBh) to reset the communicating device. This reset has the same effect as the external reset as far as the reset values of all registers are concerned. Also, an internal system reset can occur when the in-system programming is done (ROD = 1). This reset has the same effect as the external reset as far as the reset values of all registers are concerned.

Software Reset

The device UROM provides option to soft reset through the application program. The application program can jump to UROM code, which generates the internal system reset. This reset has the same effect as the internal system reset.

Further information regarding various resets can be found in the DS4830A User's Guide.

Programmable Timer

The device features two general-purpose programmable timers. Various timing loops can be implemented using the timers. The timer can be used in two modes: free-running mode and compare mode. The functionality of the timers can be accessed through three SFRs for each of the general purpose timers. GTCN is the general control register, GTV is the timer value register and GTC is the timer compare register.

The timer SFRs are accessed in Module 0 and 3. Detailed information regarding the timer block can be found in the DS4830A User's Guide.

Hardware Multiplier

The hardware multiplier (a multiply-accumulate, or MAC module) is a very powerful tool, especially for applications that require heavy calculations. This multiplier is capable of executing the multiply, multiply-negate, multiply-accumulate, multiply-subtract operation for signed or unsigned operands in a single machine cycle. The MAC module uses 10 SFRs, mapped as register 0h–05h, 07h–09h and 0Eh in Module M3.

System Interrupts

Multiple interrupt sources are available to respond to internal and external events. The microcontroller architecture uses a single interrupt vector (IV) and single interrupt-service routine (ISR) design. For maximum flexibility, interrupts can be enabled globally, individually, or by module. When an interrupt condition occurs, its individual flag is set, even if the interrupt source is disabled at the local, module, or global level. Interrupt flags must be cleared within the firmware-interrupt routine to avoid repeated interrupts from the same source. Application software must ensure a delay between the write to the flag and the RETI instruction to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, execution jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up, so if it is not changed to a different address, application firmware must determine whether a jump to 0000h came from a $\overline{RST}$ or interrupt source.

Once control has been transferred to the ISR, the interrupt identification register (IIR) can be used to determine which module was the source of the interrupt. In addition to IIR, MIIR registers are implemented to indicate which particular function under a peripheral module has caused the interrupt. The device contains six peripheral modules, M0 to M5. An MIIR register is implemented in modules M1, M4, and M5. The MIIRs are 16-bit read only registers and all of them default to all zero on system reset. Once the module that causes the interrupt is singled out, it can then be interrogated for the specific interrupt source and software can take appropriate action. Interrupts are evaluated by application code allowing the definition of a unique interrupt priority scheme for each application. Interrupt sources are available from the watchdog timer, the ADC (including sample/holds and internal temperature), fast comparators, the programmable timers, SVM, the I²C-compatible master and slave interface, 3-wire, master and slave SPI, software interrupts, as well as all GPIO pins.

I/O Port

The device allows for most inputs and outputs to function as general purpose input and/or output pins. There are four ports: P0, P1, P2, and P6. Note that there is no port pin corresponding to P6.7. The 7th bit of port 6 is nonfunctional in all SFRs. Each pin is multiplexed with at least one special function, such as interrupts, ADC, DAC, PWM, or JTAG pins etc.

The GPIO pins have Schmitt trigger receivers and full CMOS output drivers, and can support alternate functions. The ports can be accessed through SFRs (PO[0,1,2,6], PI[0,1,2,6], PD[0,1,2,6], EIE[0,1,2,6], EIF[0,1,2,6], and EIES[0,1,2,6]) in Modules 0 and 1 and each pin can be individually configured. The pin is either high impedance or a weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register.

In addition, each pin can function as an external interrupt with individual enable, flag and active edge selection, when programmed as input.

The GPIO pins also having DAC function are by default high impedance. The I/O port SFRs are accessed in Module 0 and 1. Detailed information regarding the GPIO block can be found in the DS4830A User's Guide.

DAC Outputs

The device provides eight 12-bit DAC outputs with multiple reference options. An internal 2.5V reference is provided. There are also two selectable external references. REFINA pin can be selected as the full-scale reference for DAC0 to DAC3. REFINB pin can be selected as the full-scale reference for DAC4 to DAC7. The external reference can be between 1.0V to 2.5V. The DAC outputs are voltage buffered. Each DAC can be individually disabled and put into a low power power-down mode using DACCFG.

If a DAC output is used during the lifetime of the DS4830A, the DAC must always be enabled to guarantee meeting the INL and offset specifications. If a pin is used for a DAC, it should be used only for the DAC function. The pin's function should not be switched between DAC and PWM or switched between DAC and GPIO.

The DAC SFRs are accessed in Module 4. Detailed information regarding the DAC block can be found in the DS4830A User's Guide.

Analog-to-Digital Converter, Sample/Hold

The analog-to-digital converter (ADC) controller is the digital interface block between the CPU and the ADC. It provides all the necessary controls to the ADC and the CPU interface. The ADC uses a set of SFRs for configuring the ADC in desired mode of operation.

The device contains a 13-bit ADC with an input mux, as shown in Figure 9. The mux selects the ADC input from 16 single-ended or eight differential inputs. Additionally, the channels can be configured to convert internal temperature, V_{DD}, internal reference or REFINA/B. Two channels can be programmed to be sample/hold inputs. The internal channel is used exclusively to measure the die temperature. The SFR registers control the ADC.

ADC

When used in voltage input mode, the voltage applied on the corresponding channel (differential or single-ended) is converted to a digital readout. The ADC can be set up to continuously poll selected input channels (continuous-sequence mode) or run a short burst of conversions and enter a shut down mode to conserve power (single-sequence mode).

In voltage mode there are four full-scale values that can be programmed. These values can be trimmed by modifying the associated gain registers (ADCG1, ADCG2, ADCG3, and ADCG4). By default these are set to 1.2V, 0.6V, 2.4V, and 6.55V full scale.

The ADC clock (ADCCLK) is derived from the system clock with division ratio defined by the ADC control register. The ADC sampling rate is approximately 40ksps for the fastest ADC clock (Core Clk/8). The device provides eight different ADC clock configurations to set different ADC clock setting. Refer to the ADC section of the DS4830A User's Guide for different ADC clock settings. In applications where extending the acquisition time is desired, the sample can be acquired over a prolonged period determined by the ADC control register.

Each ADC channel can have its own configuration, such as differential mode select, data alignment select, acquisition extension enable and ADC gain select, etc. The ADC also has 24 (0 to 23) 16-bit data buffers for conversion result storage. The ADC data available interrupt flag (ADDAI) can be configured to trigger an interrupt following a predetermined number of samples. Once set, ADDAI can be cleared by software or at the start of a conversion process.

The ADC controller provides options to average the ADC results of individual channel. The device provides 1, 4, 8, and 16 samples averaging configurations for each channel independently. The ADC's internal reference can be output at pin GP1.

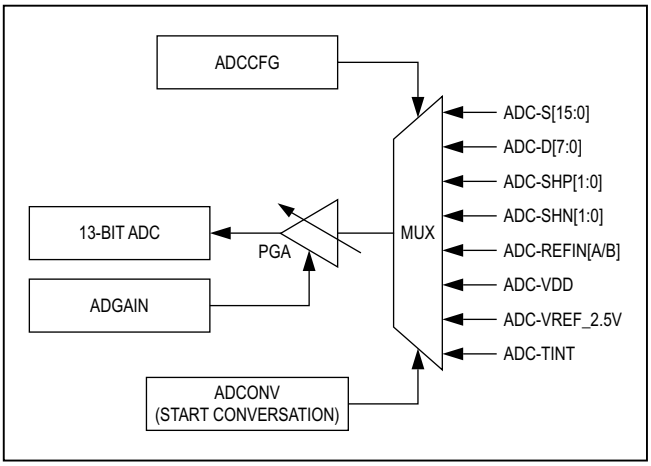


Figure 9. ADC Block Diagram

Sample/Hold

Pin combinations GP2-GP3 and GP12-GP13 can be used for sample/hold conversions if enabled in the SHCN register. These two can be independently enabled or disabled by writing a 1 or 0 to their corresponding bit locations in SHCN register. A data buffer location is reserved for each channel. When a particular channel is enabled, a sample of the input voltage is taken when a signal is issued on the SHEN pin, converted and stored in the corresponding data buffer.

The two sample/hold channels can sample simultaneously on the same SHEN signal or different SHEN signals depending on the SH_DUAL bit in the SHCN SFR.

The sample/hold data available interrupt flag (SHnDAI) can be configured to trigger an interrupt following sample completion. Once set, SHnDAI can be cleared by software.

Each sample/hold circuit consists of a sampling capacitor, charge injection nulling switches, and a buffer. Also included is a discharge circuit used to discharge parasitic capacitance on the input node and the sample capacitor before sampling begins. The negative input pins are used to reduce ground offsets and noise.

The ADC controller provides options to average the sample/hold results of individual channel. The device provides 1, 2, 4, and 8 samples averaging configurations for each channel independently.

The sample/hold inputs can be used for monitoring the burst mode receive power signal in APD biasing and OLT applications using current mirror, as shown Figure 10.

Temperature Measurement

The device provides an internal temperature sensor for die temperature monitoring which can be enabled independently by setting the appropriate bit locations in the TEMPCN register. Whenever a temperature conversion is complete the INTDAI is set. This can be configured to cause an interrupt, and can be cleared by software. The temperature measurement resolution is 0.0625°C.

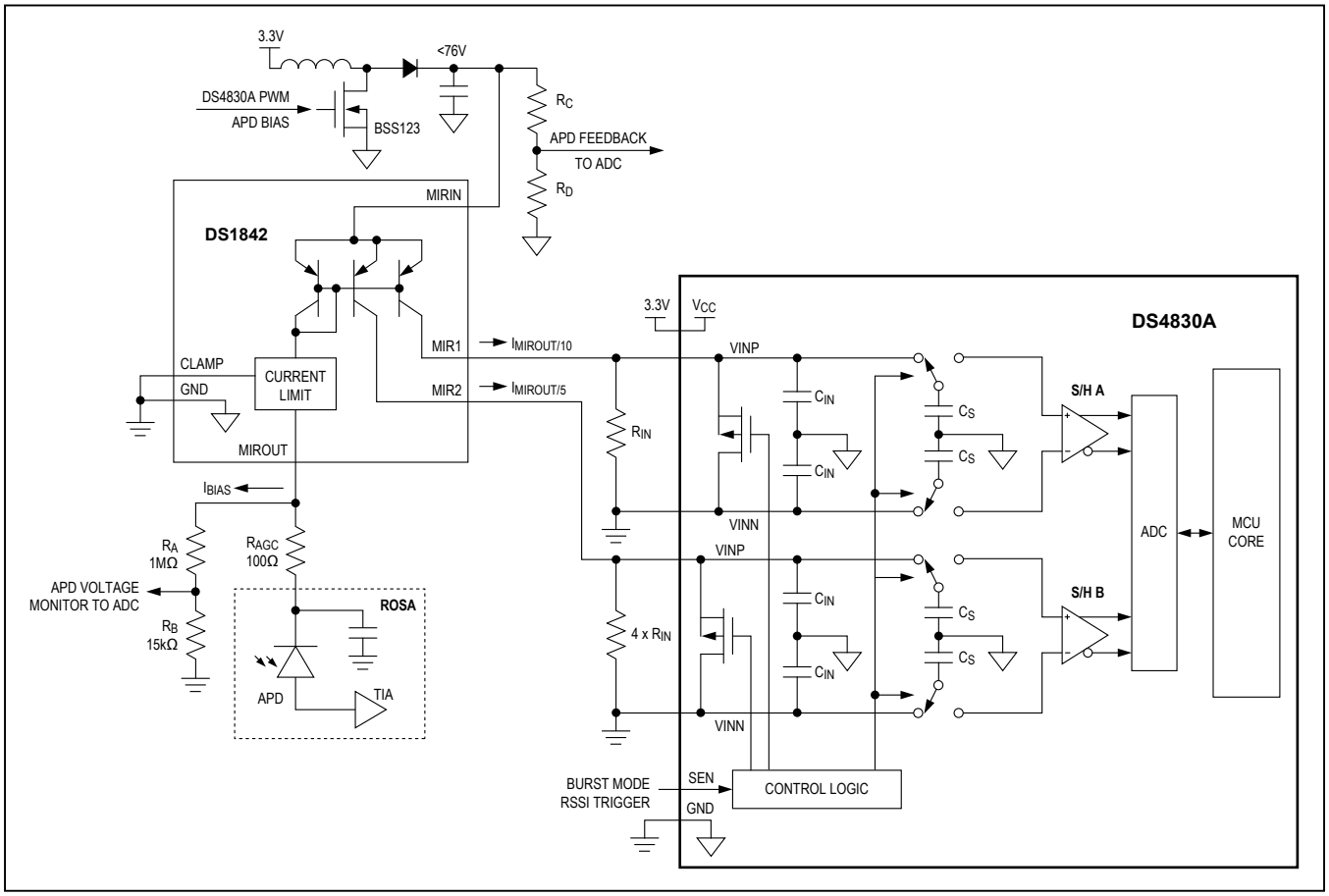


Figure 10. Burst Mode RSSI Monitoring

The ADC controller provides options to average the internal temperature results. The device provides 1, 8, 16, and 32 samples averaging configurations for the internal temperature.

The ADC related SFRs are accessed in Module 1 and Module 4. For further detailed information regarding ADC can be found in the ADC section of the DS4830A User's Guide.

PWM Outputs

The device provides 10 independently configurable PWM outputs. Each PWM output's resolution can be configured from 7-bit to 16-bit independently. The PWM outputs are configured using three SFRs: PWMCN, PWMDATA, and PWNSYNC. Using PWMCN and PWMDATA, individual PWM channels can be programmed for unique Duty Cycles (DCYCn), configurations (PWMCFGn) and delays (PWMDLYn) where n represents the PWM channel number.

The PWM clock can be obtained from the core clock, peripheral clock or an external clock depending on CLK_SEL bits programmed in individual PWMCFG registers. The PWMCFGn register also enables/disables the corresponding PWM output and selects the PWM polarity. The user can set the duty cycle and the frequency of each PWM output individually by configuring the corresponding DCYCn register and the PWMCFGn register.

The device allows delta sigma dithering for each PWM channel. The PWM outputs can be configured to be output on an alternate location using the configuration register. PWMDLY is a 16-bit register for providing starting delay on different PWM channels, and can be used to create multiphase PWM operation.

Different channels can be synchronized using the PWMSYNC register. Doing so effectively brings the channels in phase by restarting the channels that are to be synchronized. The PWM SFRs are accessed in Module 5. Detailed information regarding the PWM block can be found in the DS4830A User's Guide.

Figure 11 shows how the PWM outputs can be used to control a TEC. Refer to Application Note AN5424: *Thermoelectric Cooler Control Using the DS4830 Optical Microcontroller* for further detailed information.

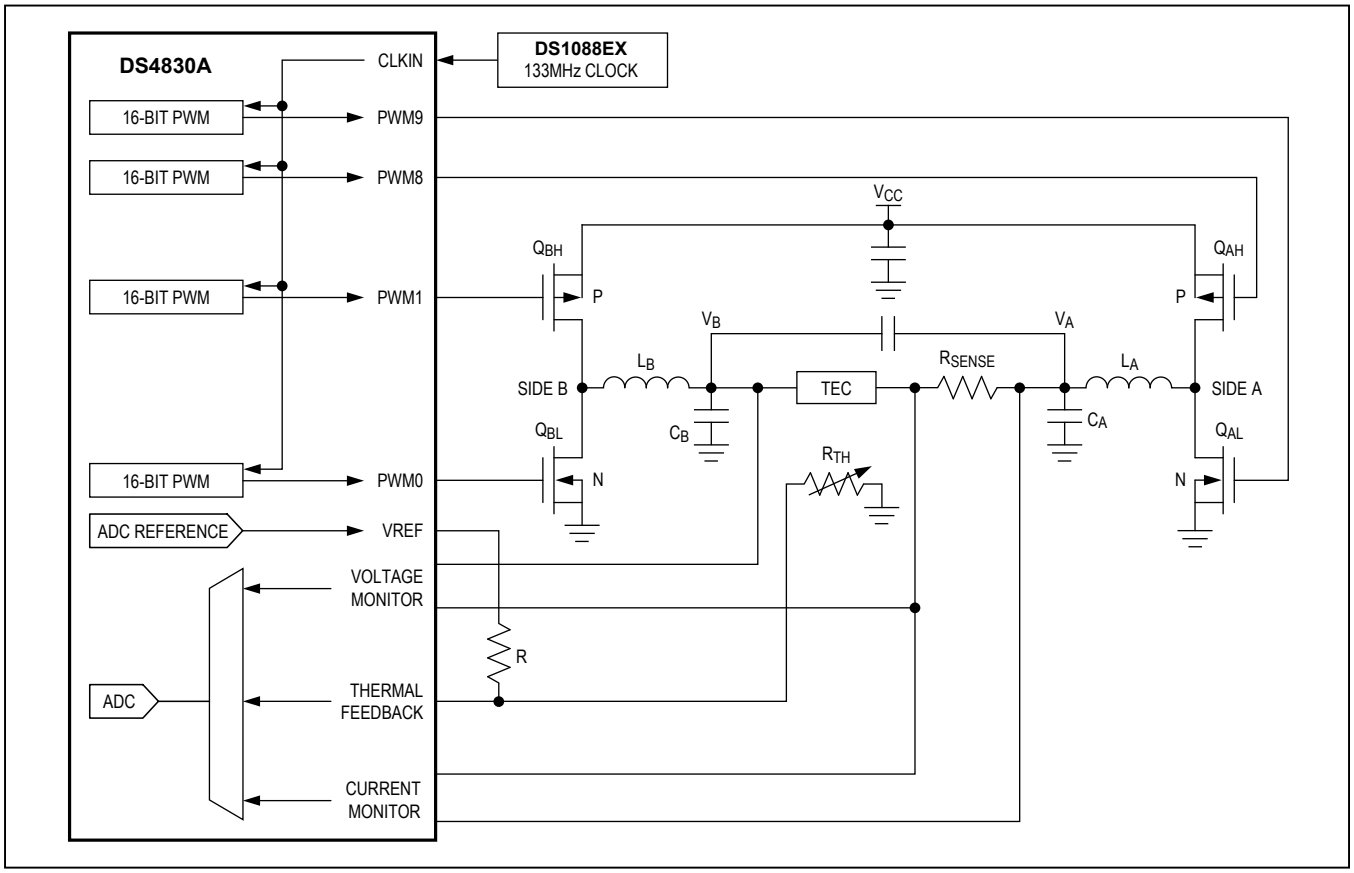


Figure 11. TEC Application

Fast Comparator/Quick Trips

The device supports 10-bit quick trip comparison functionality. The quick trips may be used to continuously monitor user defined channels in a round robin sequence. The quick trip controller allows the user to control the list of channels to monitor in the round-robin sequence.

The quick trip (analog) performs two comparisons on any selected channel.

1) Comparison with a high threshold value.
2) Comparison with a low threshold value.

Any comparison above the high threshold value or below the low threshold value causes a bit to set in the corresponding register. This bit can be used to trigger an interrupt. The threshold values are stored in 32 internal register (16 for low threshold settings and 16 for high threshold settings). The quick trip controller provides user defined threshold values for the quick trips. Because the quick trips and the ADC use the same input pins, the controller ensures that no collision takes place.

The quick-trip-related SFRs are accessed in Module 5. Refer to the quick trip section of the DS4830A User's Guide for more information.

I²C-Compatible Interface Modules

The device provides two independent I²C-compatible interfaces, one is a master and another is a slave.

I²C-Compatible Master Interface

The device features an internal I²C-compatible master interface for communication with a wide variety of external I²C devices. The I²C-compatible master bus is a bidirectional bus using two bus lines, the serial data line (MSDA) and the serial clock line (MSCL). For the I²C-compatible master, the device has ownership of the I²C bus and drives the clock and generates the START and STOP signals. This allows the device to send data to a slave or receive data from a slave.

The device has a configuration bit in the I2CCN_M register that allows the user to configure I²C master MSDA and MSCL pins to two different set of pins.

PIN	I2CCN_M.I2CM_ALT = 0	I2CCN_M.I2CM_ALT = 1
MSDA	P1.0	P1.6
MSCL	P1.1	P1.7

Details can be found in the I²C master section of the DS4830A User's Guide.

I²C-Compatible Slave Interface

The device also features an internal I²C-compatible slave interface for communication with a host. Furthermore, the device can be in system programmed (bootloaded) through the I²C-compatible slave interface. The two interface signals used by the I²C slave interface are SCL and SDA. For the I²C-compatible slave interface, the device relies on an externally generated clock to drive SCL and responds to data and commands only when requested by the I²C master device. The I²C-compatible slave interface is open-drain and requires external pull up resistors. The device supports four slave addresses. Each slave address has dedicated 8-byte transmit page and all slave addresses share common 8-byte receive FIFO.

SMBus Timeout

Both the I²C-compatible slave interfaces can work in SMBus-compatible mode for communication with other SMBus devices. To achieve this, a 30ms timer has been implemented on the I²C-compatible slave interface to make the interface SMBus-compatible. The purpose of this timer is to issue a timeout interrupt and thus the firmware can reset the I²C-compatible slave interface when the SCL is held low for longer than 30ms. The timer only starts when **none** of the following conditions is true:

1) The I²C-compatible slave interface is in the idle state and there is no communication on the bus.
2) The I²C-compatible slave interface is not working in SMBus-compatible mode.
3) The SCL logic level is high.
4) The I²C-compatible slave interface is disabled.

When a timeout occurs, the timeout bit is set and an interrupt is generated, if enabled. The I²C master related SFRs are accessed in Module 1. The I²C slave related SFRs are accessed in Module 2. Details can be found in the I²C master and slave section of the DS4830A User's Guide.

Serial Peripheral Interface Module

The device supports master and slave SPI interfaces. The SPI provides an independent serial communication channel to communicate synchronously with peripheral devices in a multiple master or multiple slave system. The interface allows access to a four-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time. The maximum data rate of the SPI is 1/4 the system reference clock frequency for slave mode and 1/2 the system clock frequency for master mode.

The SPI uses the following four interface signals:

- **Master In-Slave Out.** This signal is an output from a slave device, SSPIDO, and an input to the master device, MSPIDI. It is used to serially transfer data from the slave to the master. Data is transferred most significant bit (MSB) first. The slave device places this pin in an input state with a weak pullup when it is not selected.
- **Master Out-Slave In.** This signal is an output from a master device, MSPIDO, and an input to the slave devices, SSPIDI. It is used to serially transfer data from the master to the slave. Data is transferred MSB first.
- **SPI Clock.** This serial clock is an output from the master device, MSPICK, and an input to the slave devices, SSPICK. It is used to synchronize the transfer of data between the master and the slave on the data bus.
- **Slave Select.** The slave-select signal is an input to enable the SPI module in slave mode, SSPICS, by a master device. The SPI module supports configuration of an active SSPICS state through the slave-active select. Normally, this signal has no function in master mode and its port pin can be used as a general-purpose I/O. However, the SSEL can optionally be used as mode fault detection in master mode.

SPI Master Interface

The master mode is used when the device's SPI controls the data transmission rates and data format. The SPI is placed in master mode by setting the master mode bit (MSTM). Only an SPI master device can initiate a data transfer. Writing a data character to the SPI data buffer (SPIB), when in master mode, starts a data transfer. The SPI master immediately shifts out the data serially on MSPIDO, MSB first, while providing the serial clock on the MSPICK output. New data is simultaneously gated in on MSPIDI into the least significant bit (LSB) of the shift register. At the end of a transfer, the received data is loaded into the data buffer for reading, and the SPI transfer complete flag (SPIC) is set. If SPIC is set, an interrupt request is generated to the interrupt handler, if enabled.

SPI Slave Interface

Slave mode is used when the SPI is controlled by another peripheral device. The SPI is in slave mode when an internal bit (MSTM) is cleared to logic 0. In slave mode, the SPI is dependent on the SPICK sourced from the master to control the data transfer. The SPICK input frequency should not be greater than the system clock frequency of the slave device divided by 4. The SPI master transfers data to a slave on the SSPIDI, MSB first, the selected slave device simultaneously transfers the contents of its shift register to the master on the SSPIDO, also MSB first. Data received from the master replaces data in the slave's shift register at the completion of a transfer. Just like in the master mode, received data is loaded into the read buffer and the SPIC is set at the end of the transfer. Setting the SPIC flag may cause an interrupt if enabled.

The SPI master-related SFRs are accessed in Module 5. The SPI slave-related SFRs are accessed in Module 4. Details can be found in the SPI section of the DS4830A User's Guide.

3-Wire Interface Module

The device controls 3-wire slave devices like the MAX3798 and MAX3799 over a proprietary 3-wire interface. The device acts as the 3-wire master, initiating communication with and generating the clock for the 3-wire slave. It is a 3-pin interface consisting of MSDIO (a bidirectional data line), an MSCL clock signal, and an MCS chip-select output (active high).

The 3-wire master-related SFRs are accessed in Module 4. Detailed information regarding the 3-wire interface block can be found in the DS4830A User's Guide.

In-Circuit Debug

Embedded debugging capability is available through the JTAG-compatible test access port (TAP). Embedded debug hardware and embedded ROM firmware provide in-circuit debugging capability to the user application, eliminating the need for an expensive in-circuit emulator. Figure 12 shows a block diagram of the in-circuit debugger. The in-circuit debug features include the following:

- Hardware debug engine
- Set of registers able to set breakpoints on register, code, or data accesses (ICDA, ICDB, ICDC, ICDD, ICDF, ICDT0, and ICDT1)
- Set of debug service routines stored in the utility ROM

The embedded hardware debug engine is an independent hardware block in the microcontroller. The debug engine can monitor internal activities and interact with selected internal registers while the CPU is executing user code. Collectively, the hardware and software features allow two basic modes of in-circuit debugging:

- Background mode allows the host to configure and set up the in-circuit debugger while the CPU continues to execute the application software at full speed. Debug mode can be invoked from background mode.
- Debug mode allows the debug engine to take control of the CPU, providing read/write access to internal registers and memory, and single-step trace operation.

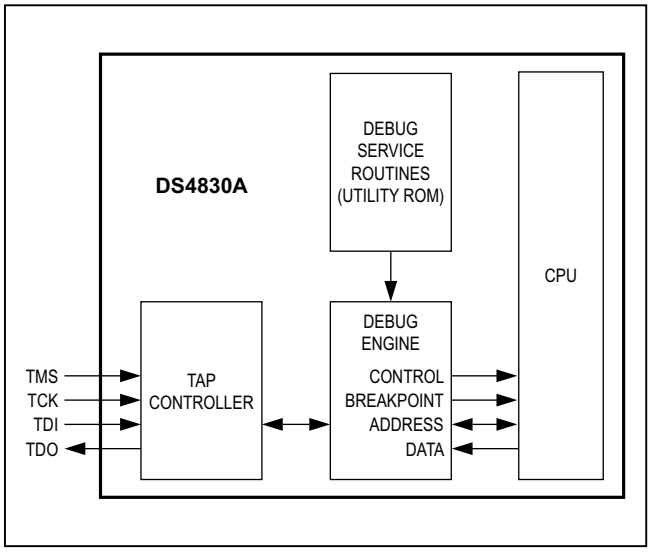


Figure 12. In-Circuit Debugger

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS4830A, decouple the V_{DD} power supply with a 0.1µF X5R capacitor. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Decouple the REG274 and REG18 pins using 1µF X5R and 10nF capacitors (one each/per output). **Note: Do not use either of these pins for external circuitry.**

Additional Documentation

Designers must have three documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. User guides offer detailed information about device features and operation. The following documents can be downloaded from **www.maximintegrated.com/DS4830A**.

- The DS4830A data sheet, which contains electrical/timing specifications, package information, and pin descriptions.
- The DS4830A revision-specific errata sheet, if applicable.
- The DS4830A User's Guide, which contains detailed information and programming guidelines for core features and peripherals.

Development and Technical Support

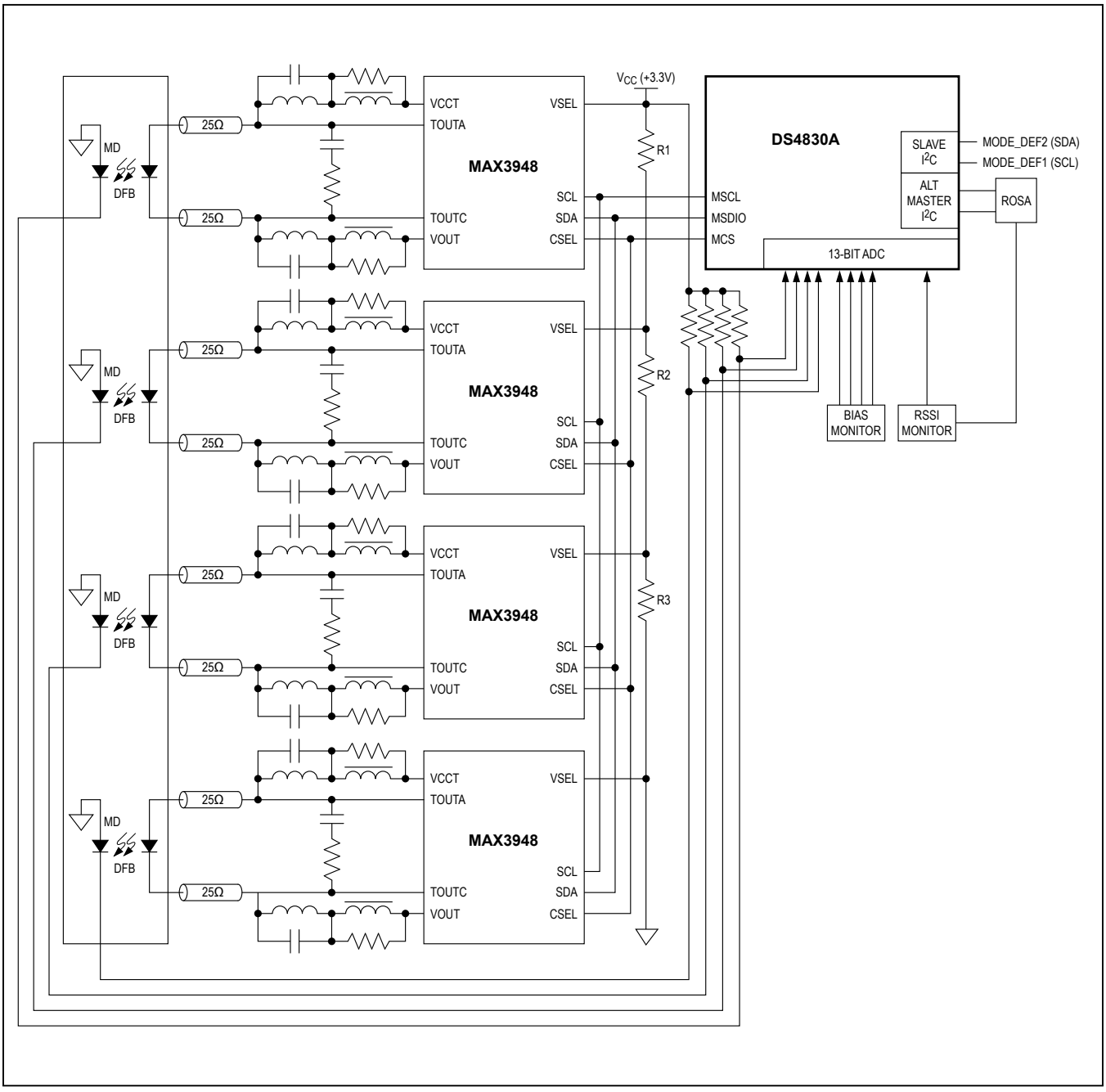
Maxim Integrated and third party suppliers provide a variety of highly versatile, affordably priced development tools for this microcontroller, including the following:

- Compilers (C and assembly)
- In-circuit debugger
- Integrated development environments (IDEs)
- Serial-to-JTAG converters for programming and debugging
- USB-to-JTAG converters for programming and debugging

A partial list of development tool vendors can be found at **www.maximintegrated.com/MAXQ_tools**.

Go to **www.maximintegrated.com/support** for additional technical support.

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS4830AT+	-40°C to +85°C	40 TQFN-EP*
DS4830AT+T	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/13	Initial release	—
1	1/17	Updated *DAC Outputs* section and *Package Information* table	2, 24

