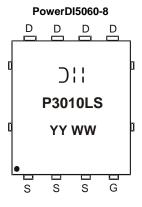


### **Marking Information**



□!! = Manufacturer's Marking P3010LS = Product Type Marking Code YYWW = Date Code Marking YY = Year (ex: 15 = 2015)WW = Week (01 - 53)

# Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V <sub>DSS</sub>	-30	V
Gate-Source Voltage			V <sub>GSS</sub>	±20	V
Continuous Drain Current (Note 8) V <sub>GS</sub> = 10V	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I <sub>D</sub>	-36 -29	А
Continuous Drain Current (Note 8) V <sub>GS</sub> = 4.5V	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I <sub>D</sub>	-31 -25	А
Continuous Drain Current (Note 7) V <sub>GS</sub> = 10V	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I <sub>D</sub>	-14.5 -11.5	А
Pulsed Drain Current (Notes 7 & 10)			I <sub>DM</sub>	-100	Α
Avalanche Current (Notes 11 & 12)			I <sub>AS</sub>	-17.5	Α
Avalanche Energy (Notes 11 & 12) L = 1mH			E <sub>AS</sub>	153	mJ

### **Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 6)	P <sub>D</sub>	1.26	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 6)	R <sub>θJA</sub>	97	°C/W
Power Dissipation (Note 7)	$P_{D}$	2.18	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 7)	$R_{\theta JA}$	55	°C/W
Power Dissipation (Note 8)	P <sub>D</sub>	14.37	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 8)	$R_{\theta JA}$	8.7	°C/W
Power Dissipation (Notes 8 & 9)	P <sub>D</sub>	58.7	W
Thermal Resistance, Junction to Case @T <sub>C</sub> = +25°C (Notes 8 & 9)	$R_{ heta JC}$	2.13	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

Notes:

- 6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  7. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
- 8. Device mounted on FR-4 PCB with infinite heatsink.
- 9.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.
- 10. Repetitive rating, pulse width limited by junction temperature, 10µs pulse, duty cycle = 1%.
- 11.  $I_{AS}$  and  $E_{AS}$  rating are based on low frequency and duty cycles to keep  $T_J = +25$ °C.



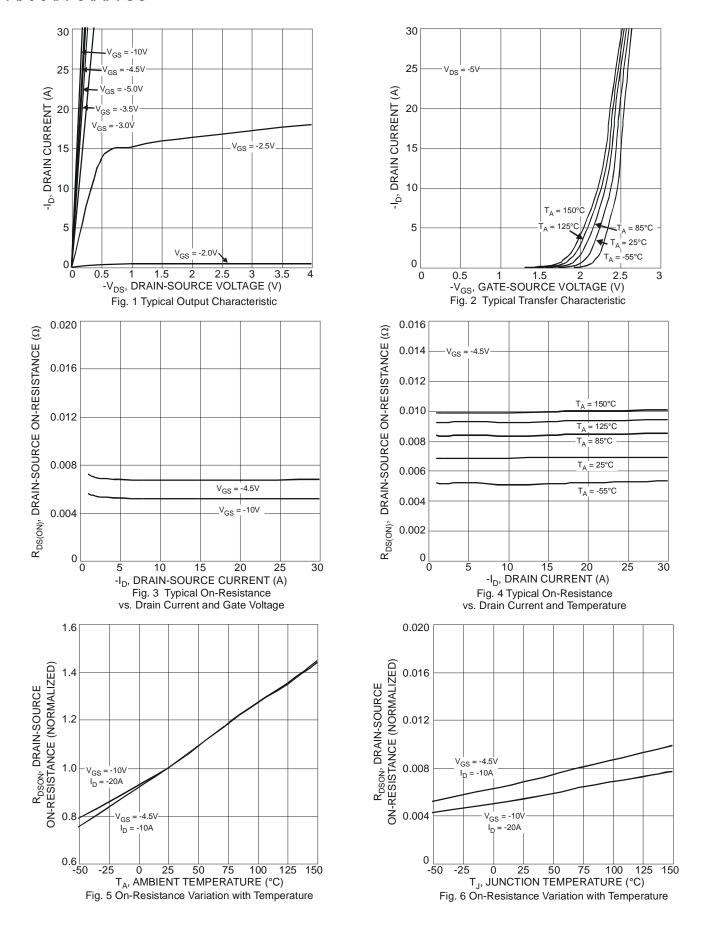
### Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 12)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-30	_	_	V	$V_{GS} = 0V, I_{D} = -250\mu A$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	-1	μΑ	$V_{DS} = -30V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 12)							
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1.1	-1.6	-2.1	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
Static Drain-Source On-Resistance	D	l	5.7	7.5	mΩ	$V_{GS} = -10V, I_D = -10A$	
Static Diain-Source On-Nesistance	R <sub>DS(ON)</sub>	-	7.2	10		$V_{GS} = -4.5V, I_D = -10A$	
Forward Transfer Admittance	Y <sub>fs</sub>	1	30	_	S	$V_{DS} = -15V, I_{D} = -10A$	
Diode Forward Voltage	$V_{SD}$	_	-0.65	-1	V	$V_{GS} = 0V, I_{S} = -1A$	
DYNAMIC CHARACTERISTICS (Note 13)							
Input Capacitance	Ciss	1	6,234	1	pF	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1MHz	
Output Capacitance	Coss	-	1,500	-	pF		
Reverse Transfer Capacitance	C <sub>rss</sub>	I	774	l	pF		
Gate Resistance	$R_g$	_	1.28	_	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge (V <sub>GS</sub> = -10V)	$Q_g$	_	126.2	_	nC	$V_{DS} = -15V, I_{D} = -10A$	
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Qg	_	59.2	_	nC	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -10A	
Gate-Source Charge	Q <sub>gs</sub>	_	16.1	_	nC		
Gate-Drain Charge	Q <sub>gd</sub>		15.7		nC		
Turn-On Delay Time	t <sub>D(on)</sub>	_	11.4		ns	$V_{DS} = -15V$ , $V_{GEN} = -10V$ , $R_G = 6\Omega$ , $I_D = -1A$	
Turn-On Rise Time	t <sub>r</sub>	I	9.4	l	ns		
Turn-Off Delay Time	t <sub>D(off)</sub>	1	260.7	1	ns		
Turn-Off Fall Time	t <sub>f</sub>	_	99.3	_	ns		

Notes:

- 12. Short duration pulse test used to minimize self-heating effect.13. Guaranteed by design. Not subject to product testing.







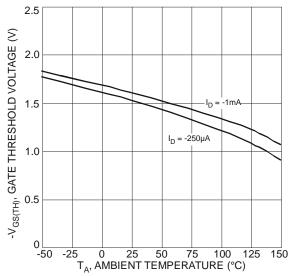
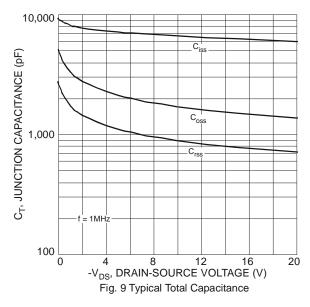
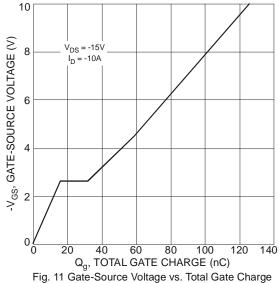
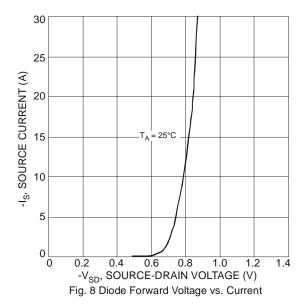


Fig. 7 Gate Threshold Variation vs. Ambient Temperature







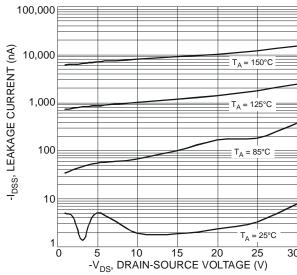
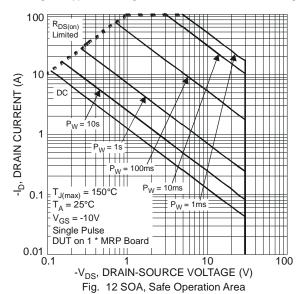
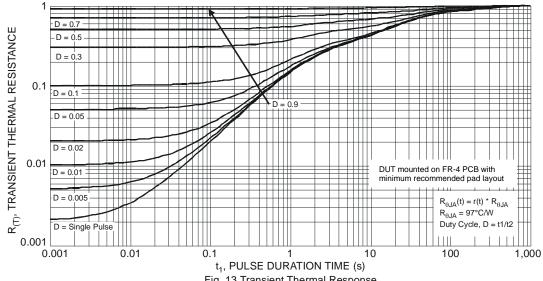


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage





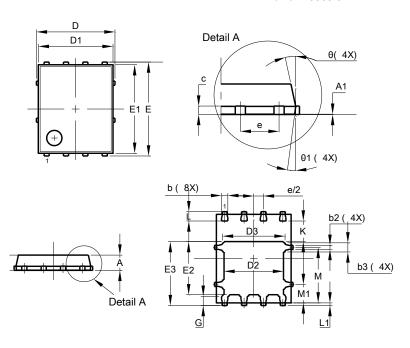




### **Package Outline Dimensions**

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

#### PowerDI5060-8

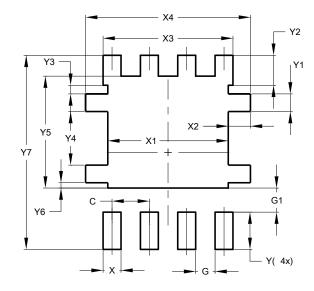


		.=			
PowerDI5060-8					
Dim	Min	Max	Тур		
Α	0.90	1.10	1.00		
A1	0.00	0.05	-		
b	0.33	0.51	0.41		
b2	0.200	0.350	0.273		
b3	0.40	0.80	0.60		
C D	0.230	0.330	0.277		
D	5.15 BSC				
D1	4.70	5.10	4.90		
D2	3.70	4.10	3.90		
D3	3.90	4.30	4.10		
Е	6.15 BSC				
E1	5.60	6.00	5.80		
E2	3.28	3.68	3.48		
E3	3.99	4.39	4.19		
е	1.27 BSC				
G	0.51	0.71	0.61		
K	0.51	-	_		
L	0.51	0.71	0.61		
L1	0.100	0.200	0.175		
M	3.235	4.035	3.635		
M1	1.00	1.40	1.21		
Θ	10°	12°	11°		
Θ1	6°	8°	7°		
All Dimensions in mm					

## **Suggested Pad Layout**

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

#### PowerDI5060-8



Dimensions	Value (in mm)
С	1.270
G	0.660
G1	0.820
Х	0.610
X1	4.100
X2	0.755
Х3	4.420
X4	5.610
Υ	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610



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