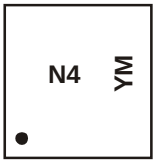
Marking Information

Site 1



N4 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: H = 2020)
M = Month (ex: 9 = September)

Date Code Key

Year	2011	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	Y	…	H	I	J	K	L	M	N	O	P	R

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Site 2

N4 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 0 = 2020)
W = Week (ex: a = Week 27; z Represents Week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2011	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	1	…	0	1	2	3	4	5	6	7	8	9

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	±12	V
Continuous Drain Current (Note 6) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	10.5 8.5	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	12.5 10.0	A
Continuous Drain Current (Note 6) V_{GS} = 2.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	9.4 7.5	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	11.2 8.8	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	80	A
Maximum Body Diode Continuous Current			I_S	2.5	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	0.66	W
	T_A = +70°C		0.42	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	189	°C/W
	t<10s		132	
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	2.03	W
	T_A = +70°C		1.31	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	61	°C/W
	t<10s		43	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	9.3	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1	µA	V_{DS} = 16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±12V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.5	—	1.1	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	9.3	11.6	mΩ	V_{GS} = 4.5V, I_D = 8.5A
			11.4	15		V_{GS} = 2.5V, I_D = 8.5A
			17	30		V_{GS} = 1.8V, I_D = 5A
			24	50		V_{GS} = 1.5V, I_D = 3A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	11.3	—	s	V_{DS} = 10V, I_D = 8.5A
Diode Forward Voltage	V_{SD}	—	—	1.2	V	V_{GS} = 0V, I_S = 8.5A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	1779	—	pF	V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	175	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	154	—	pF	
Gate Resistance	R_g	—	0.94	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	19.7	—	nC	V_{DS} = 10V, I_D = 8.5A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	45.6	—	nC	
Gate-Source Charge	Q_{gs}	—	2.9	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.8	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	7.4	—	ns	V_{DS} = 10V, I_D = 8.5A V_{GS} = 4.5V, R_G = 1.8Ω
Turn-On Rise Time	t_r	—	16.8	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	43.6	—	ns	
Turn-Off Fall Time	t_f	—	10.9	—	ns	
Reverse Recovery Time	T_{rr}	—	8.6	—	ns	I_F = 8.5A, di/dt = 210A/µs
Reverse Recovery Charge	Q_{rr}	—	3.7	—	nC	

Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

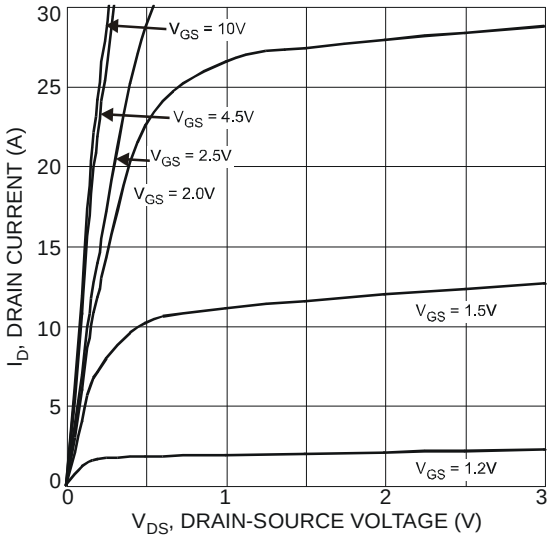


Fig.1 Typical Output Characteristic

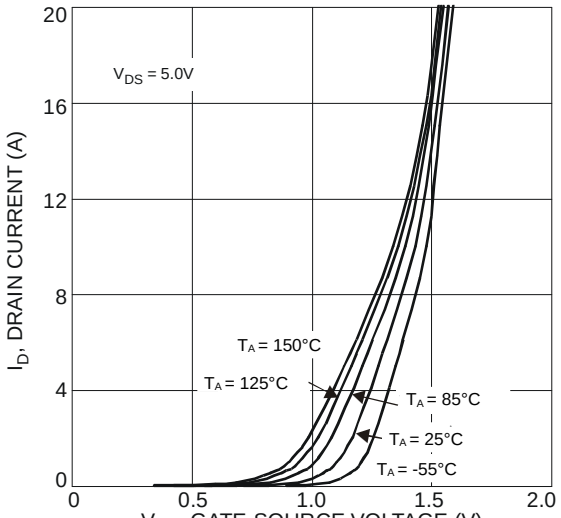


Fig. 2 Typical Transfer Characteristics

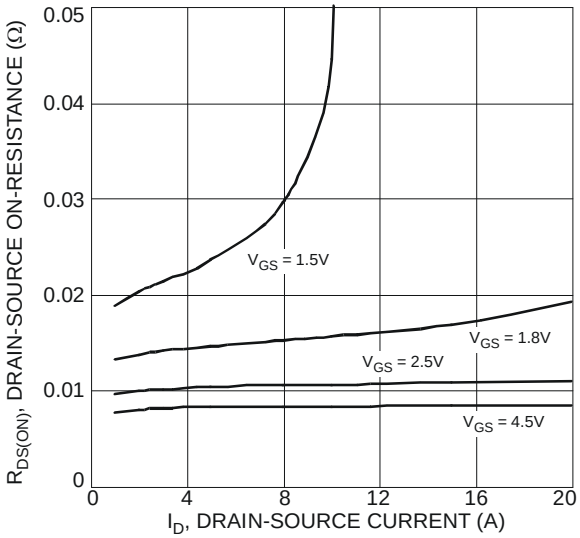


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

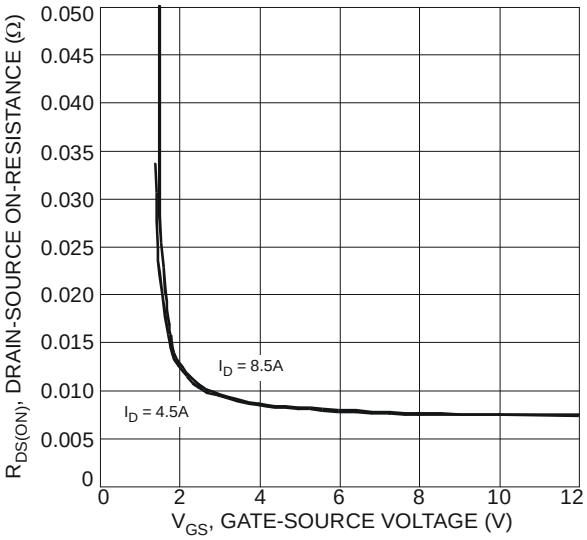


Fig. 4 Typical Drain-Source On-Resistance vs. Gate-Source Voltage

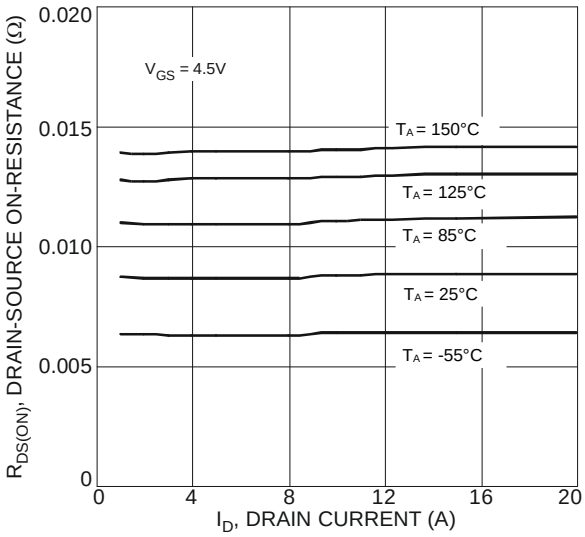


Fig. 5 Typical On-Resistance vs. Drain Current and Temperature

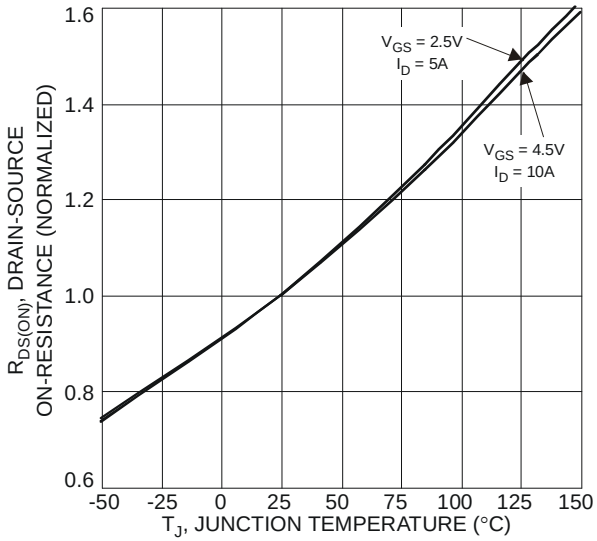


Fig. 6 On-Resistance Variation with Temperature

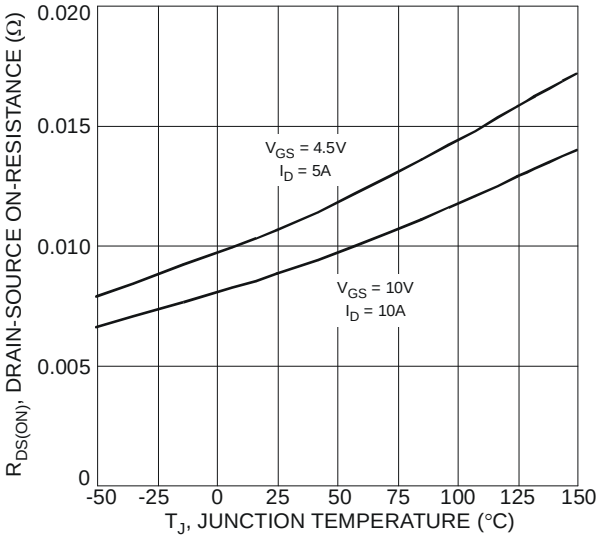


Fig. 7 On-Resistance Variation with Temperature

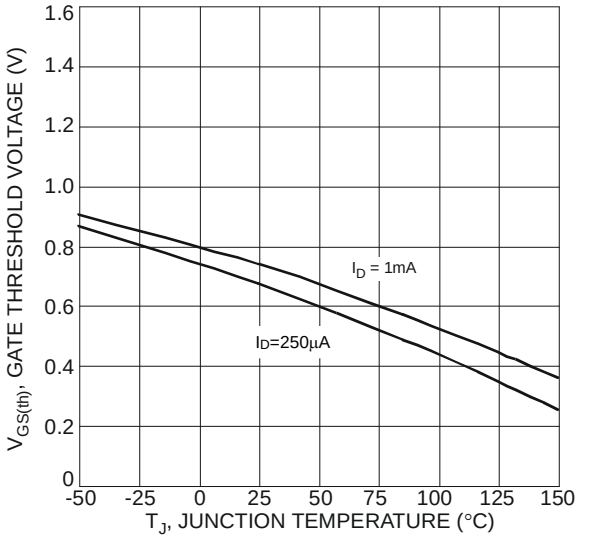


Fig. 8 Gate Threshold Variation vs. Junction Temperature

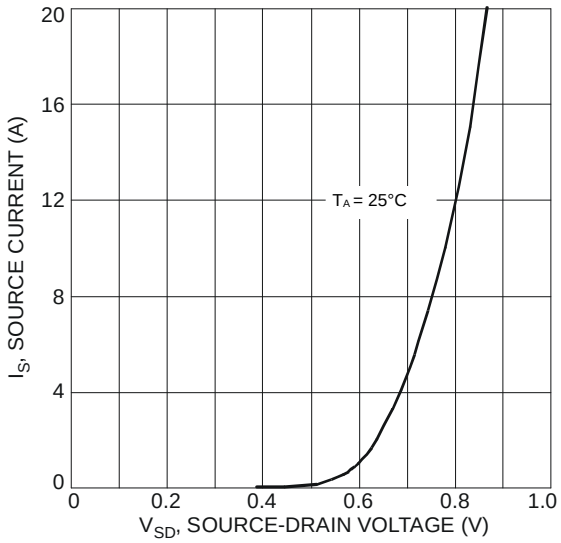


Fig. 9 Diode Forward Voltage vs. Current

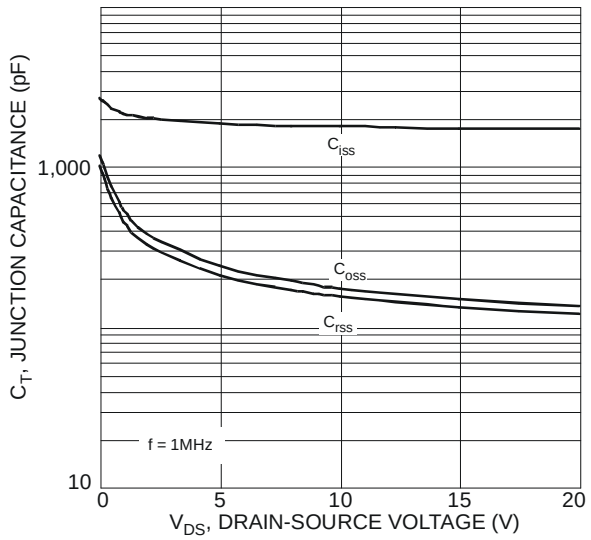


Fig. 10 Typical Junction Capacitance

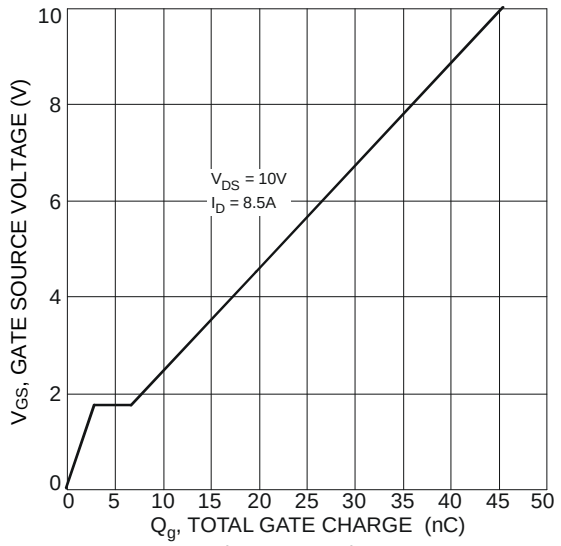


Fig. 11 Gate Charge

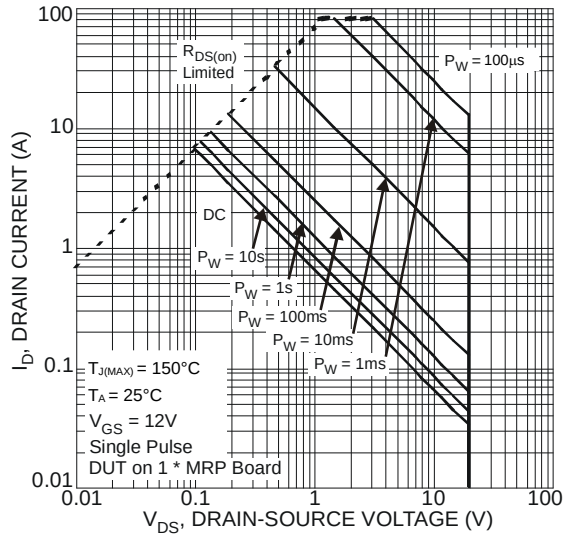


Fig. 12 SOA, Safe Operation Area

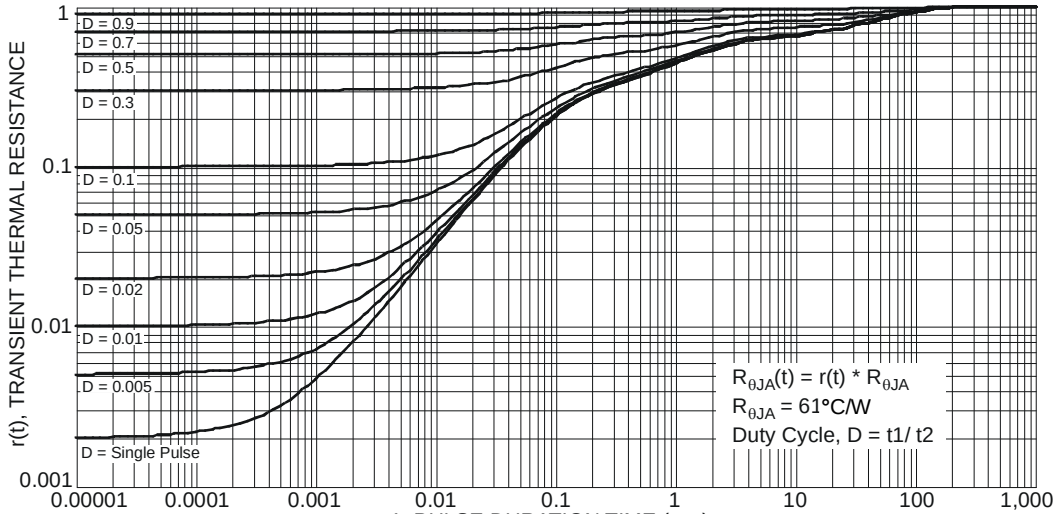
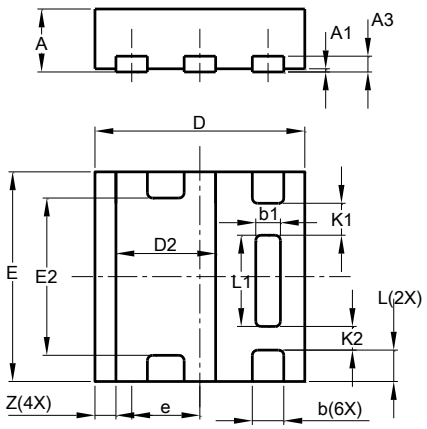


Fig. 13 Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type E)

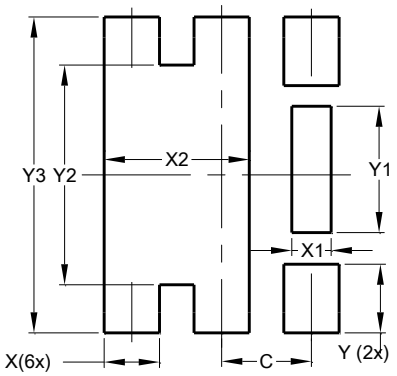


U-DFN2020-6 Type E			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	–	–	0.15
b	0.25	0.35	0.30
b1	0.185	0.285	0.235
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
E	1.95	2.05	2.00
E2	1.40	1.60	1.50
e	–	–	0.65
L	0.25	0.35	0.30
L1	0.82	0.92	0.87
K1	–	–	0.305
K2	–	–	0.225
Z	–	–	0.20
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type E)



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.285
X2	1.050
Y	0.500
Y1	0.920
Y2	1.600
Y3	2.300

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