Vishay Siliconix



ABSOLUTE MAXIMUM RATINGS						
Parameter		Limit	Unit			
Referenced V+ to GND		- 0.3 to + 4	V			
IN, COM, NC, NO ^a	- 0.3 to (V+ + 0.3)]				
Continuous Current (NO, NC and COM Pins)		± 200	m A			
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 300	mA mA			
Storage Temperature (D Suffix)		- 65 to 150	°C			
Power Dissipation (Packages) ^b	6-Pin SO70 ^c	250	mW			

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings. b. All leads welded or soldered to PC Board.
- c. Derate 3.1 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 1.8 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 1.8 V, ± 10 %, V _{IN} = 0.4 or 1.1 V ^e	Temp ^a	Limits - 40 to 85 °C			
				Min ^b	Typ ^c	Max ^b	Unit
Analog Switch							•
Analog Signal Range ^d	$V_{NO}, V_{NC} V_{COM}$		Full	0		V+	V
On-Resistance	r _{ON}	$V+ = 1.8 \text{ V}, V_{COM} = 0.2 \text{ V}/0.9 \text{ V}$ $I_{NO}, I_{NC} = 10 \text{ mA}$	Room Full ^d		1.8	3.0 4.5	Ω
r _{ON} Flatness ^d	r _{ON} Flatness	$V+ = 1.8 \text{ V}, V_{COM} = 0 \text{ to V+, } I_{NO}, I_{NC} = 10 \text{ mA}$	Room			2	
r _{ON} Match ^d	Δr _{ON}		Room			0.06	
Switch Off Leakage Current ^f	I _{NO(off)} I _{NC(off)}	V+ = 2.2 V V _{NO} , V _{NC} = 0.2 V/2.0 V, V _{COM} = 2.0 V/0.2 V	Room Full ^d	- 1 - 10		1 10	nA
	I _{COM(off)}		Room Full ^d	- 1 - 10		1 10	
Channel-On Leakage Current ^f	I _{COM(on)}	$V_{+} = 2.2 \text{ V}, V_{NO}, V_{NC} = V_{COM} = 0.2 \text{ V}/2.0 \text{ V}$	Room Full ^d	- 1 - 10		1 10	
Digital Control							•
Input High Voltage	V _{INH}		Full	1.1			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance ^d	C _{in}		Full		3.5		pF
Input Current ^f	I _{INL} or I _{INH}	$V_{IN} = 0$ or V+	Full	- 1		1	μΑ
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 300 Ω , C_L = 35 pF Figures 1 and 2	Room Full ^d		55	75 89	ns
Turn-Off Time ^d	t _{OFF}		Room Full ^d		19	39 40	
Break-Before-Make Time ^d	t _d		Room	3			
Charge Injection ^d	Q _{INJ}	$C_L = 1 \text{ nF, } V_{GEN} = 0 \text{ V, } R_{GEN} = 0 \Omega, \text{ Figure 3}$	Room		13		рC
Off-Isolation ^d	OIRR	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$	Room		- 64		dB
Crosstalk ^d	X _{TALK}		Room		- 64		
NO, NC Off Capacitance ^d	$C_{NO(off)} \ C_{NC(off)}$	V _{IN} = 0 or V+, f = 1 MHz	Room		32		pF
Channel-On Capacitance ^d	C _{ON}		Room		78		

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SPECIFICATIONS (V		Test Conditions		Limits			
Parameter		Otherwise Unless Specified		-	40 to 85 °	C	Unit
	Symbol	$V+ = 3 V, \pm 10 \%, V_{IN} = 0.5 \text{ or } 1.5 V^{e}$	Temp ^a	Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	r _{ON}	$V+ = 2.7 \text{ V}, V_{COM} = 0.2 \text{ V}/1.5 \text{ V}$ $I_{NO}, I_{NC} = 100 \text{ mA}$	Room Full		0.85	1.2 1.3	
r _{ON} Flatness	r _{ON} Flatness	$V+ = 2.7 \text{ V}, V_{COM} = 0 \text{ to V+}, I_{NO}, I_{NC} = 100 \text{ mA}$	Room			0.2	Ω
r _{ON} MatchFlat	Δr_{ON}		Room			0.06	
Switch Off Leakage Current	I _{NO(off)} I _{NC(off)}	V+ = 3.3 V	Room Full	- 1 - 10		1 10	
Switch On Leakage Guirent	V_{NO} , $V_{NC} = 0.3 \text{ V/3 V}$, $V_{COM} = 3 \text{ V/10.3 V}$	Room Full	- 1 - 10		1 10	nA	
Channel-On Leakage Current	I _{COM(on)}	$V+ = 3.3 \text{ V}, V_{NO}, V_{NC} = V_{COM} = 0.3 \text{ V/3 V}$	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.5			V
Input Low Voltage	V_{INL}		Full			0.5	•
Input Capacitance ^d	C _{in}		Full		3.3		pF
Input Current ^f	I _{INL} or I _{INH}	$V_{IN} = 0$ or $V+$	Full	- 1		1	μΑ
Dynamic Characteristics							
Turn-On Time	t _{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω , C_L = 35 pF Figures 1 and 2	Room Full		28	51 55	ns
Turn-Off Time	t _{OFF}		Room Full		12	33 34	113
Break-Before-Make Time	t _d		Room	1			
Charge Injection ^d	Q _{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω , Figure 3	Room		9		рС
Off-Isolation ^d	OIRR	$R_1 = 50 \Omega$, $C_1 = 5 pF$, $f = 1 MHz$	Room		- 64		dB
Crosstalk ^d	X _{TALK}	$H_L = 50.14$, $O_L = 5$ pr, $T = 1$ MHZ	Room		- 64		
NO, NC Off Capacitance ^d	$C_{NO(off)} \ C_{NC(off)}$	V _{IN} = 0 or V+, f = 1 MHz	Room		30		pF
Channel-On Capacitance ^d	C _{ON}		Room		77		
Power Supply							
Power Supply Range	V+			1.5		3.6	V
Power Supply Current	I+	$V+ = 3.6 V$, $V_{IN} = 0 \text{ or } V+$			0.01	1.0	μΑ

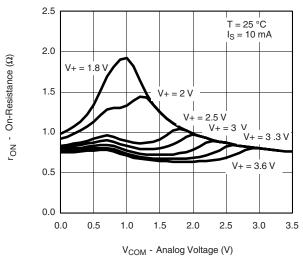
Notes:

- a. Room = 25 $^{\circ}$ C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Guaranteed by 3 V leakage testing, not production tested.

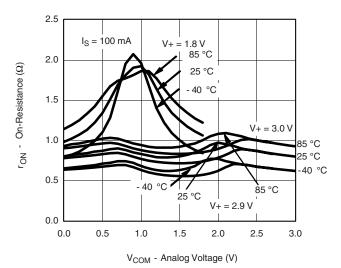
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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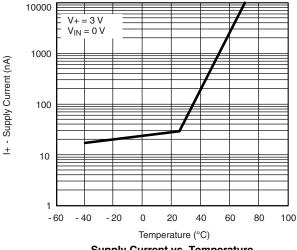
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



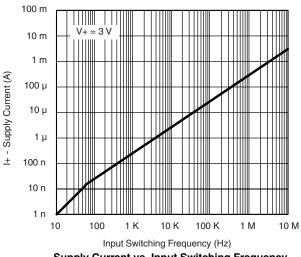
 r_{ON} vs. V_{COM} and Single Supply Voltage



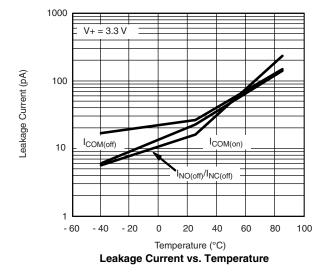
 $r_{\mbox{\scriptsize ON}}$ vs. Analog Voltage and Temperature

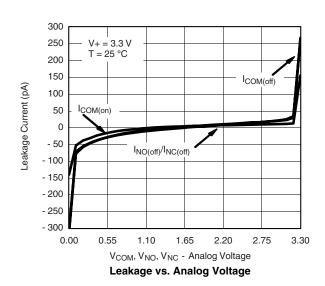


Supply Current vs. Temperature



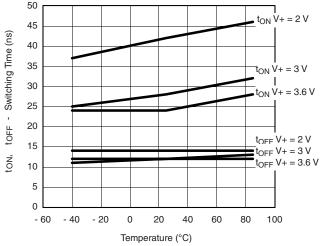
Supply Current vs. Input Switching Frequency



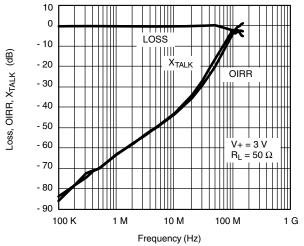




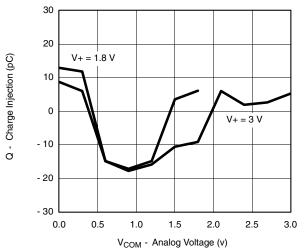
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







Insertion Loss, Off-Isolation Crosstalk vs. Frequency

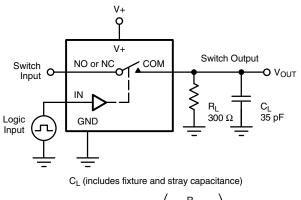


Charge Injection vs. Analog Voltage

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TEST CIRCUITS



 V_{INH} V_{INL} 0 V $t_r < 5 \text{ ns}$ $t_f < 5 \text{ ns}$ t_{OFF}

Logic "1" = Switch On Logic input waveforms inverted for switches that have the opposite logic sense.

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Figure 1. Switching Time

Logic

Input

Switch

Output

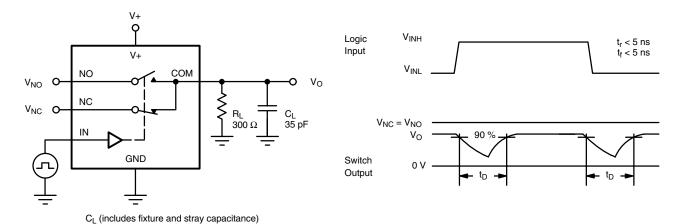


Figure 2. Break-Before-Make Interval

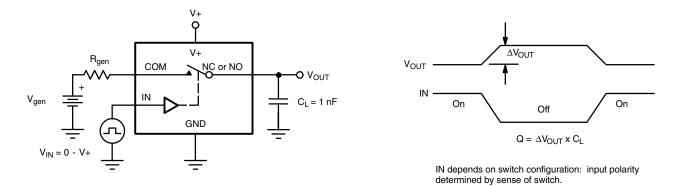


Figure 3. Charge Injection



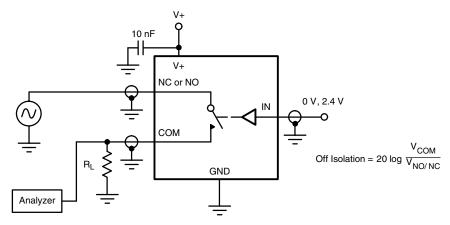


Figure 4. Off-Isolation

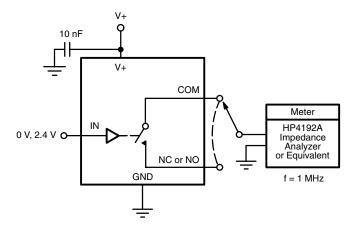


Figure 5. Channel Off/On Capacitance

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