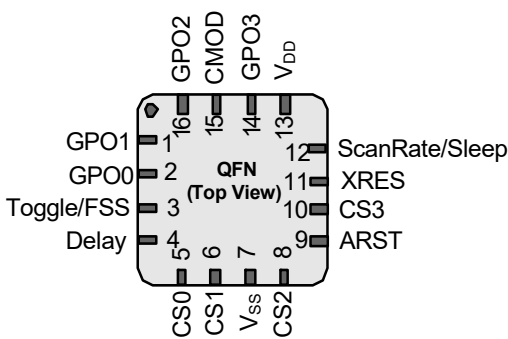


## Contents

<b>Pinout</b> .....	<b>3</b>	Recommended Via Hole Placement .....	16
<b>Typical Circuits</b> .....	<b>4</b>	Example PCB Layout Design with Four	
Schematic 1: 4-Buttons, 4-LEDs		CapSense Buttons and Four LEDs .....	17
with Auto Reset Enabled .....	4	<b>Electrical Specifications</b> .....	<b>18</b>
Schematic 2: 3-Buttons, 3-LEDs, 2-Outputs		Absolute Maximum Ratings .....	18
to Master, and Advanced Features Enabled .....	5	Operating Temperature .....	18
<b>Configuring the CY8CMBR2044</b> .....	<b>6</b>	DC Electrical Characteristics .....	19
<b>Device Features</b> .....	<b>6</b>	AC Electrical Specifications .....	21
CapSense Buttons .....	6	CapSense Specifications .....	21
SmartSense Auto Tuning .....	6	<b>Ordering Information</b> .....	<b>22</b>
General Purpose Outputs .....	6	Ordering Code Definitions .....	22
Toggle ON/OFF .....	7	<b>Package Diagram</b> .....	<b>23</b>
Flanking Sensor Suppression (FSS) .....	7	Package Information .....	23
LED ON Time .....	7	<b>Appendix</b> .....	<b>24</b>
Button Auto Reset .....	8	<b>Acronyms</b> .....	<b>26</b>
System Diagnostics .....	9	<b>Document Conventions</b> .....	<b>26</b>
Serial Debug Data .....	10	Units of Measure .....	26
Power Consumption and Device Operating		<b>Document History Page</b> .....	<b>27</b>
Modes .....	12	<b>Sales, Solutions, and Legal Information</b> .....	<b>29</b>
Additional Components to Enable Advanced		Worldwide Sales and Design Support .....	29
Features .....	14	Products .....	29
Response Time .....	14	PSoC® Solutions .....	29
<b>Layout Guidelines and Best Practices</b> .....	<b>15</b>	Cypress Developer Community .....	29
CapSense Button Shapes .....	16	Technical Support .....	29
Button Layout Design .....	16		

## Pinout

**Table 1. Pin Diagram and Definitions – CY8CMBR2044**

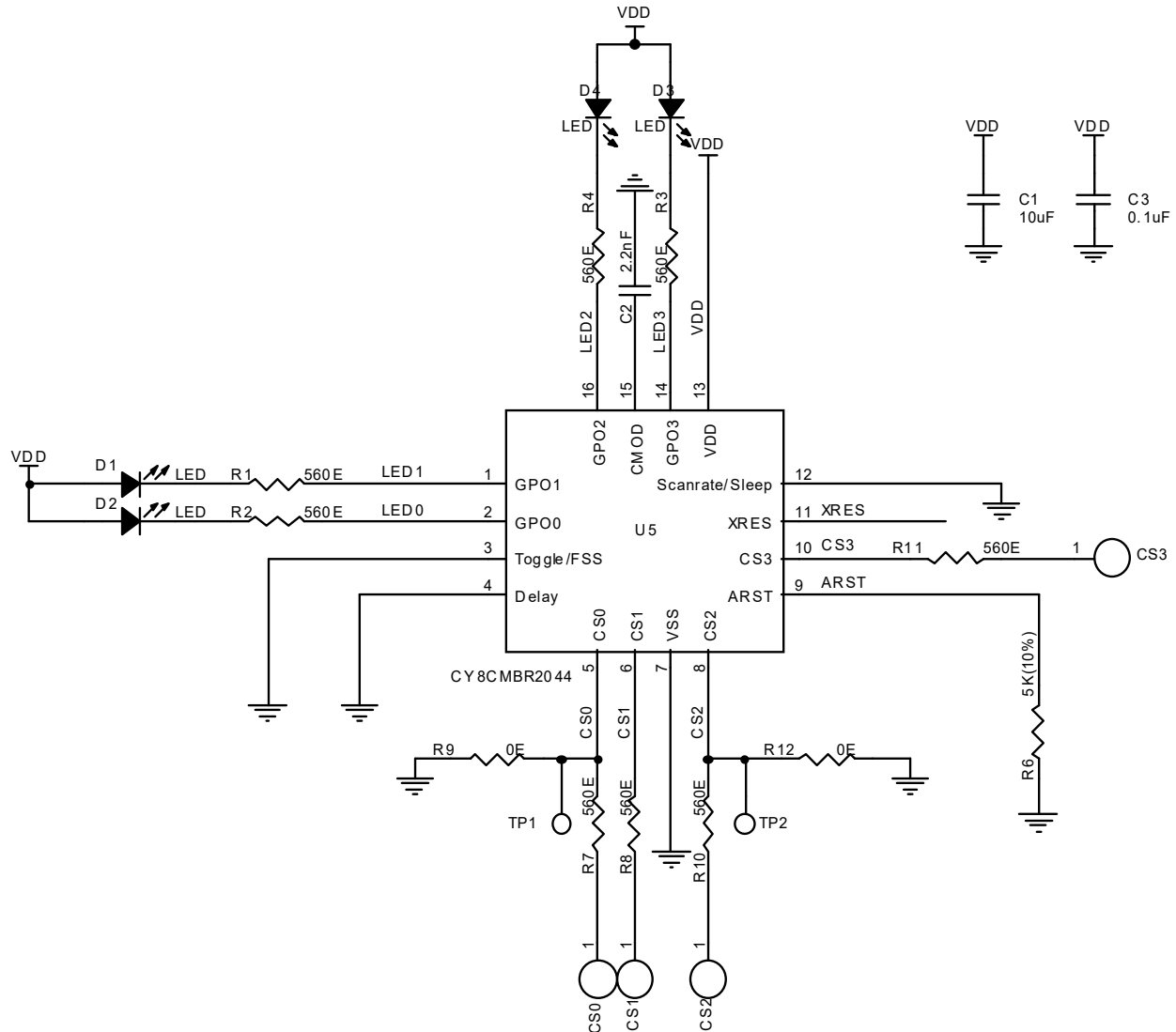
Pin	Label	Type <sup>[2]</sup>	Description	If Unused	
1	GPO1	DO	GPO activated by CS1	Leave open	
2	GPO0	DO	GPO activated by CS0	Leave open	
3	Toggle/ FSS	AI	Controls FSS and Toggle ON/OFF features	Ground	
4	Delay	AI	Controls LED ON Time. For details refer to <a href="#">Table 2 on page 6</a>	Ground	
5	CS0	AIO	CapSense input, controls GPO0 or serial debug data out	Ground	
6	CS1	AIO	CapSense input, controls GPO1 or serial debug data out	Ground	
7	V <sub>SS</sub>	P	Ground		
8	CS2	AIO	CapSense input, controls GPO2 or serial debug data out	Ground	
9	ARST	AIDO	Controls Button Auto Reset	Leave open	
10	CS3	AIO	CapSense input, controls GPO3 or serial debug data out	Ground	
11	XRES	DI	Device reset, active high, with internal pull down	Leave open	
12	ScanRate / Sleep	AI	Controls scan rate and deep sleep	Ground	
13	V <sub>DD</sub>	P	Power		
14	GPO3	DO	GPO activated by CS3	Leave open	
15	C <sub>MOD</sub>	AI	External modulator capacitor, connect a 2.2 nF (±10%) to ground		
16	GPO2	DO	GPO activated by CS2	Leave open	

**Note**

2. AI – Analog Input, AIO – Analog Input / Output, AIDO – Analog Input / Digital Output, DI – Digital Input, DO – Digital Output, P – Power

## Typical Circuits

### Schematic 1: 4-Buttons, 4-LEDs with Auto Reset Enabled



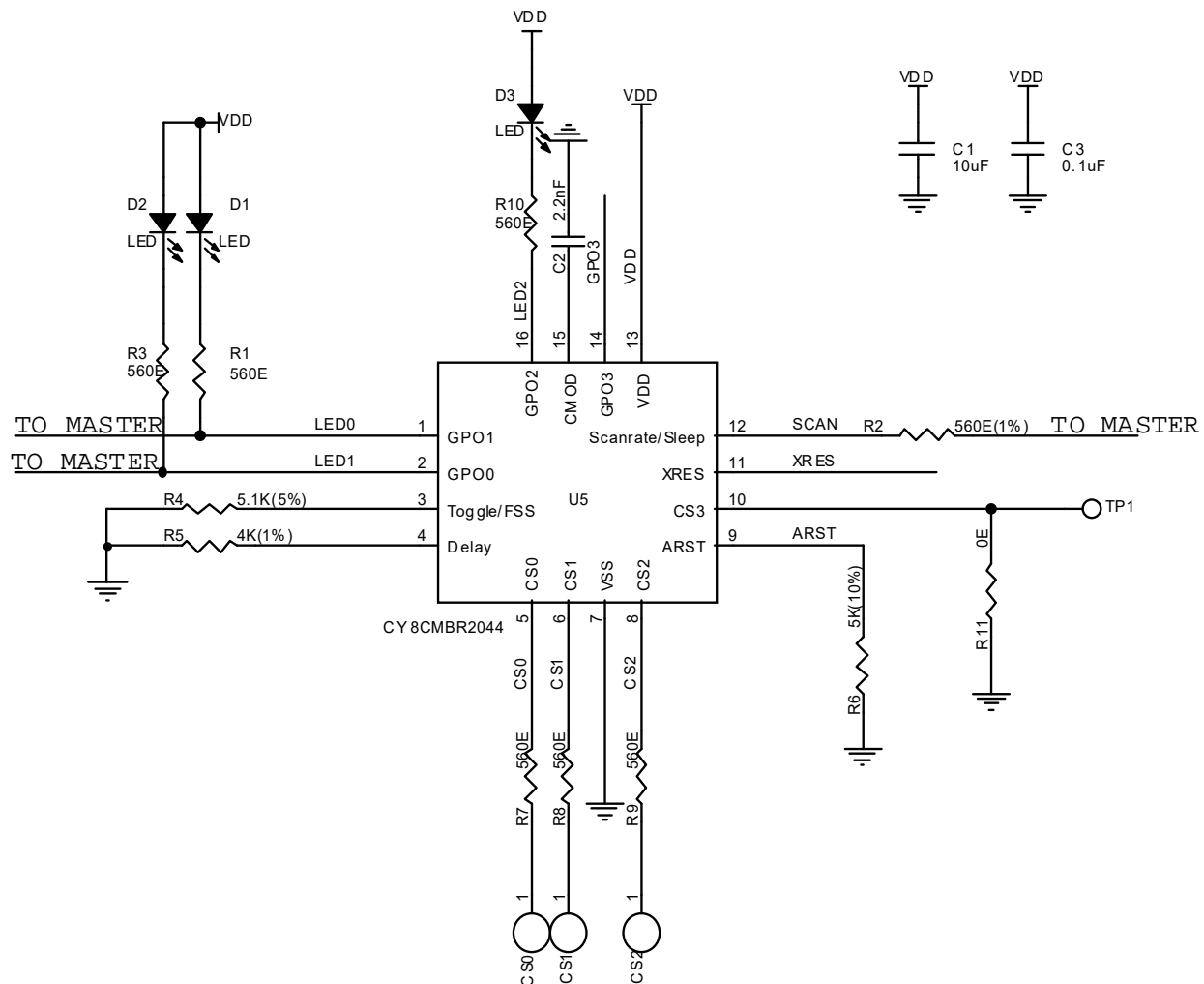
In the above schematic, the device is configured to support:

- CS0–CS3 pins: 560-Ω to CapSense button
  - Four CapSense buttons (CS0–CS3)
- GPO0–GPO3 pins: LED and 560-Ω to  $V_{DD}$ 
  - CapSense buttons driving 4 LEDs (GPO0–GPO3)
- $C_{MOD}$  pin: 2.2 nF to ground
  - Modulator capacitor
- XRES pin: Floating
  - For external reset

- Toggle/FSS pin: Ground
  - Toggle ON/OFF disabled
  - FSS disabled
- ARST pin: 5 kΩ to Ground
  - Button Auto Reset enabled, 20 second time
- Delay pin: Ground
  - LED ON Time disabled
- ScanRate/Sleep pin: Ground
  - User configured scan rate = 20 ms

To enable Serial Debug Data output, connect a 5.6 kΩ resistor on R9 or R12.

### Schematic 2: 3-Buttons, 3-LEDs, 2-Outputs to Master, and Advanced Features Enabled



In the above schematic the device is configured to support:

- CS0–CS2 pins: 560-Ω to CapSense buttons; CS3 pin: Ground
  - Three CapSense buttons (CS0–CS2)
  - CS3 not used in design
- GPO0–GPO2 pins: LED and 560-Ω to VDD; GPO3 floating; GPO0–GPO1 pins interfaced to Master
  - CapSense buttons driving 3 LEDs (GPO0–GPO2)
  - GPO0, GPO1 interfaced to master for direct status read
- C<sub>MOD</sub> pin: 2.2 nF to ground
  - Modulator capacitor
- XRES pin: Floating
  - For external reset

- Toggle/FSS pin: 5.1 k $\Omega$  to Ground
    - Toggle ON/OFF disabled
    - FSS enabled
  - ARST pin: 5 k $\Omega$  to Ground
    - Button Auto Reset enabled, Auto Reset period = 20 seconds
  - Delay pin: 4 k $\Omega$  to Ground
    - LED ON Time of 1000 ms
  - ScanRate/Sleep pin: 560  $\Omega$  to Master
    - User configured scan rate = 30 ms
    - Master to control device operating mode
- To enable Serial Debug Data output, connect a 5.6 k $\Omega$  resistor on R11.

## Configuring the CY8CMBR2044

The CY8CMBR2044 device features are configured using external resistors.

The resistors on the hardware configurable pins are determined by the device upon power-on.

The [Appendix](#) gives the matrix of features enabled using different external resistor configurations.

To know more about the required settings for your design, refer to the [CY8CMBR2044 Design Guide](#).

## Device Features

### CapSense Buttons

- Device supports up to four CapSense buttons
- Ground the CSx pin to disable CapSense input
- A 2.2-nF ( $\pm 10\%$ ) capacitor must be connected on the C<sub>MOD</sub> pin for proper CapSense operation
- The parasitic Capacitance (C<sub>P</sub>) of each button must be less than 40 pF for proper CapSense operation

### SmartSense Auto Tuning

- Device supports auto tuning of CapSense parameters
- No manual tuning required; all parameters are automatically tuned by the device
- Compensates printed circuit board (PCB) variations, device process variations, and PCB vendor changes
- Ensures portability of the user interface design

## General Purpose Outputs

- The GPOx is controlled by the corresponding CSx
- GPOx pins output are in strong drive mode <sup>[3]</sup>
- Active low output – supports sinking configuration
- If CSx is disabled (grounded), then the corresponding GPOx must be left floating
- A 5-ms active LOW pulse is sent after 175 ms after device power-up, on a GPOx after that it is set to Logic HIGH, if the CSx fails the System Diagnostics.
- GPOx pin outputs are in strong drive mode at logic level HIGH in Deep sleep power mode.
- GPOx pins output are in strong drive mode and retain the logic level same as before entering into low power sleep mode based on feature like (Toggle ,etc).
- All GPO pins are placed in a High-impedance state during reset i.e. XRES,POR.

**Table 2. Advanced Features supported by CY8CMBR2044**

Feature	Benefits
<a href="#">Toggle ON/OFF</a>	Button retains state on touch (ON/OFF)
<a href="#">Flanking Sensor Suppression (FSS)</a>	Helps in distinguishing closely spaced buttons
<a href="#">LED ON Time</a>	Gives an LED effect on button release
<a href="#">Button Auto Reset</a>	Disables false output trigger due to conducting object placed close to button
<a href="#">System Diagnostics</a>	Support for production testing and debugging
<a href="#">Serial Debug Data</a>	Support for production testing and validating design
<a href="#">Low Power Sleep Mode and Deep Sleep Mode</a>	Low power consumption

### Note

3. When a pin in in strong drive mode, it is pulled up to V<sub>DD</sub> when the output is HIGH and pulled down to Ground when the output is LOW. The output cannot be floating.

### Toggle ON/OFF

- Toggles the GPO state at each button touch.
- Used for mechanical button replacement. For example, wall switch.

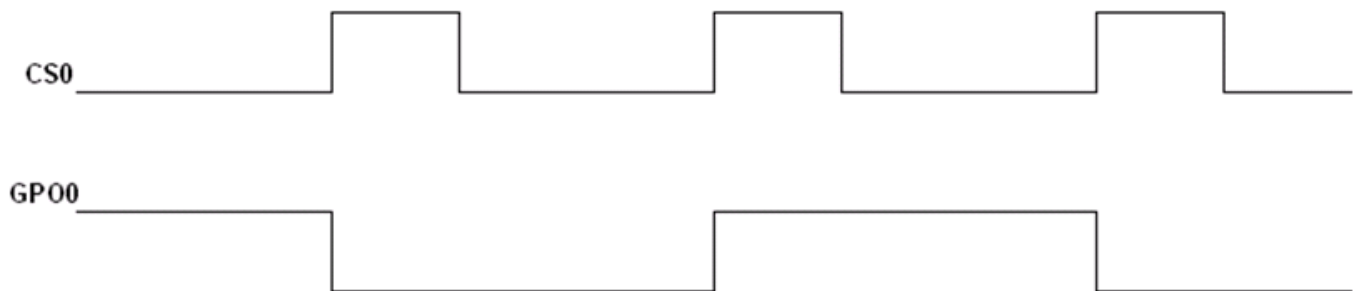
### Flanking Sensor Suppression (FSS)

- Helps to distinguish closely spaced buttons.
- Also used in situations when a button can produce opposite effects. For example, an interface with two buttons for brightness control (UP or DOWN).
- FSS action can be explained for the following different scenarios:
  - When only one button is touched, it is reported as ON.
  - When more than one button is detected as ON and previously one of those buttons was touched, then the previously touched button is reported as ON.

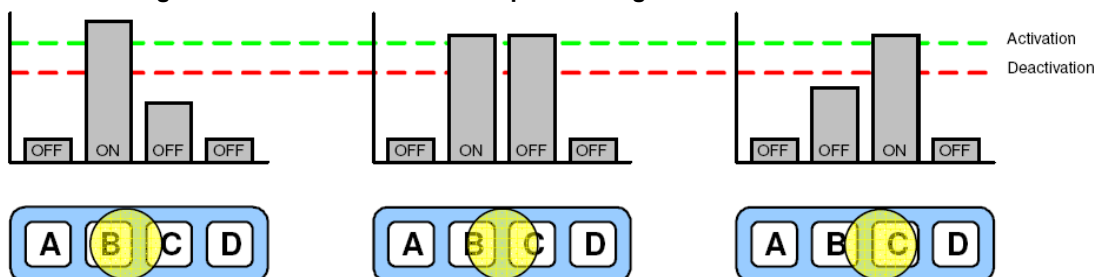
### LED ON Time

- Provides better visual feedback when a button is released and improves the design's aesthetic value.
- The GPOx is driven low for a specified interval after the corresponding CSx button is released.
- When a button gets reset, LED ON Time is not applied on the corresponding GPO.
- In [Figure 3 on page 7](#), GPO0 goes high prematurely (prior to LED ON Time) because CS1 button is released. Therefore, the LED ON Time counter is reset. Now, GPO1 remains LOW for LED ON Time after releasing CS1.
- LED ON Time can range from 0–2000 ms.
- LED ON Time resolution is 20 ms.

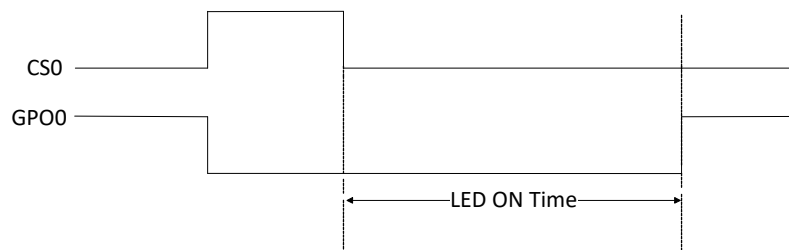
**Figure 1. Example of Toggle Feature on GPO**



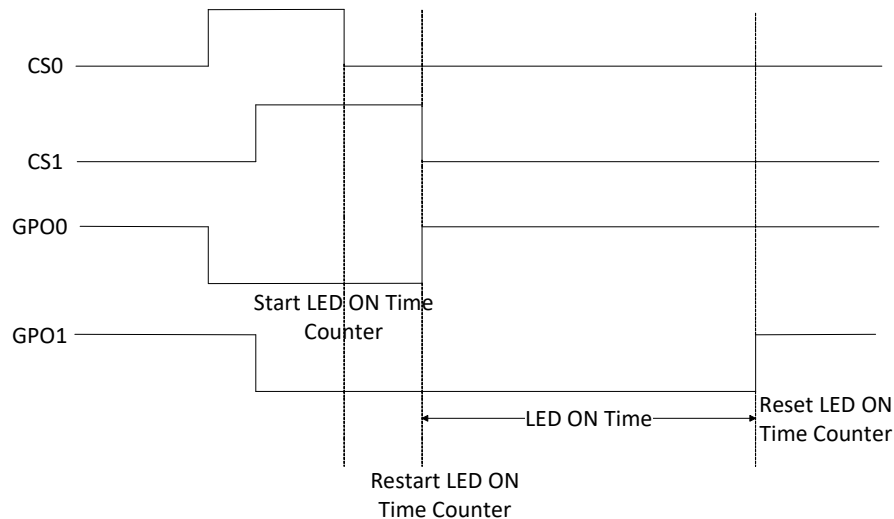
**Figure 2. Button Status with Respect to Finger Touch when FSS is Enabled**



**Figure 3. Example LED ON timing diagram on GPO0**



**Figure 4. Example LED ON timing diagram on multiple GPO0 and GPO1**



### Button Auto Reset

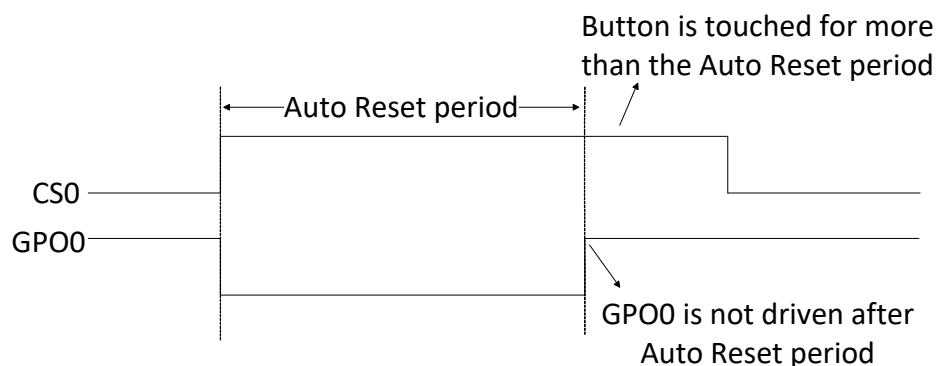
- Prevents button stuck, due to metal object placed close to a button.
- Useful when GPO output to be kept ON only for a specific time.
- If enabled, the GPOx is driven for a maximum of Button Auto Reset period when CSx is continuously touched. See [Figure 5 on page 8](#).

- Button Auto Reset period can be set to 5 or 20 seconds.
- After the Button Auto Reset has been triggered, the CSx hold time of that button after the button has been released is given in [Table 3](#). The hardware configuration is shown in [Table 18](#) in [Appendix](#).

**Table 3. Button Hold Time After Auto Reset**

Button Press Time after Button Auto Reset	Button Hold Time (ms)
< 2 sec	220
> 2 sec	ScanRate + 200

**Figure 5. Example of Button Auto Reset on GP0**



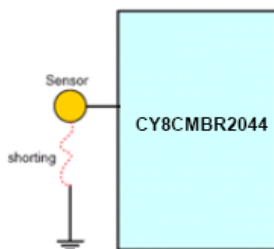
## System Diagnostics

- A built-in Power-on Self Test (POST) mechanism performs some tests at Power-on Reset (POR), which can be useful in production testing.
- If any button fails these tests, a 5 ms pulse is sent out on the corresponding GPO withing 175 ms after POR.
- Following tests are performed on all the buttons -

### *Button Shorted to Ground*

If any button is found to be shorted to ground, it is disabled. See [Figure 6](#).

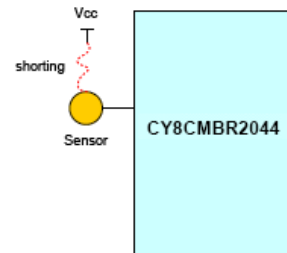
**Figure 6. Button Shorted to Ground**



### *Button Shorted to V<sub>DD</sub>*

If any button is found to be shorted to V<sub>DD</sub>, it is disabled. See [Figure 7](#).

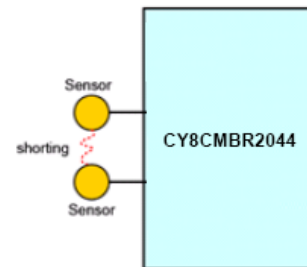
**Figure 7. Button Shorted to VDD**



### *Button to Button Short*

If two or more buttons are found to be shorted to each other, all of these buttons are disabled. See [Figure 8](#).

**Figure 8. Button to Button Short**



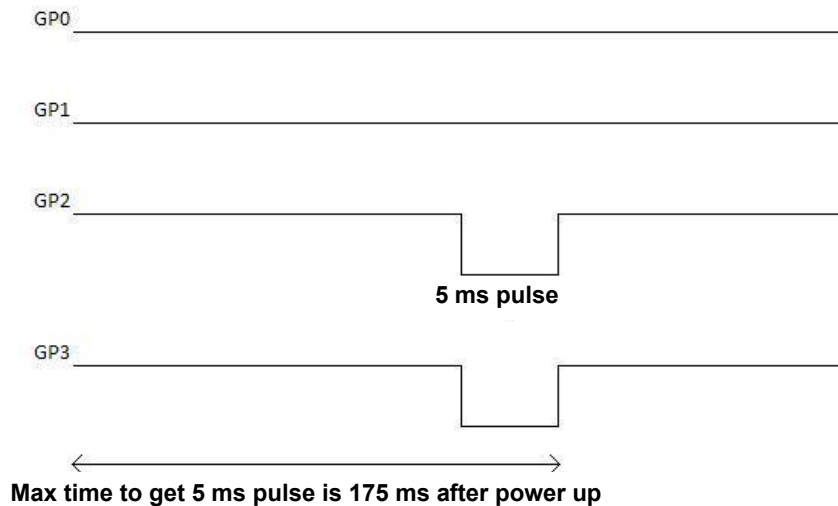
### *Improper Value of C<sub>MOD</sub>*

- Recommended value of C<sub>MOD</sub> is 2 nF to 2.4 nF.
- If the value of C<sub>MOD</sub> is found to be less than 1 nF or greater than 4 nF, all the buttons are disabled.

### *Button C<sub>P</sub> > 40 pF*

If the parasitic capacitance (C<sub>P</sub>) of any button is found to be more than 40 pF, that button is disabled.



**Figure 9. Example Showing CS0 and CS1 Passing the POST and CS2 and CS3 Failing**


In [Figure 9](#), CS0 and CS1 buttons are enabled; CS2 and CS3 buttons are disabled because they failed the Power-on Self Test. A 5 ms pulse is observed on GPO2 and GPO3.

#### Serial Debug Data

- Used to see CapSense data for debug purposes
- If enabled, debug data is transmitted using UART communication protocol.
- To enable this feature pull down any one of the CapSense pins with a 5.6 kΩ resistor to ground. Data is sent out on the same CapSense pin
- If more than one CapSense pin is pulled down, debug data is sent out only on one CapSense pin and the priority is CS0 > CS1 > CS2 > CS3
- The Cypress MultiChart tool can be used to view the data as a graph.
- Serial data is sent out with ~115,200 baud rate (refer to [AN2397](#), chapter 6. Enabling UART-to-USB Bridge Using CY3240-I2USB Bridge, to enable reading debug data from this device).

- Firmware revision, CapSense status, GPO status, raw count, baseline, difference count, and parasitic capacitance of all sensors are sent out

- For designs having a maximum of three CapSense buttons, Cypress recommends to take the debug data on a CapSense button that is not used in design

- For designs with four CapSense buttons, Cypress recommends taking debug data on two CapSense buttons. For example, pull down CS0 with a 5.6 kΩ resistor and read data of CS1, CS2, and CS3. Next, pull down CS1 with a 5.6 kΩ resistor and read data of CS0, CS2, and CS3

For more information on Raw Count, Baseline, Difference Count and Parasitic Capacitance, refer to [Getting Started with CapSense](#), section 2. For more information on MultiChart tool, refer to [AN2397](#) CapSense Data Viewing Tools, Method 2.

- MultiChart tool arranges the data in the format as shown in [Table 4](#).

- The Serial Debug Data is sent by the device in the order as per [Table 5](#).

**Table 4. Serial Debug Data arranged in MultiChart**

S.No.	Raw Count Array		Baseline Array		Signal Array	
	MSB	LSB	MSB	LSB	MSB	LSB
0	0x00	FW_Revision	CS_Status	GPO_Status	0x00	CS2_Cp
1	0x00	CS0_Cp	0x00	CS1_Cp	0x00	CS3_Cp
2	CS0_RawCount		CS0_Baseline		CS0_DiffCount	
3	CS1_RawCount		CS1_Baseline		CS1_DiffCount	
4	CS2_RawCount		CS2_Baseline		CS2_DiffCount	
5	CS3_RawCount		CS3_Baseline		CS3_DiffCount	

**Table 5. Serial Data Output sent by CY8CMBR2044**

Byte	Data	Notes
0	0x0D	Dummy data for multi chart
1	0x0A	
2	0x00	
3	FW_Revision	–
4	0x00	–
5	CS0_Cp	CS0 parasitic capacitance in Hex
6	CS0_RawCount_MSB	Unsigned 16-bit integer
7	CS0_RawCount_LSB	–
8	CS1_RawCount_MSB	Unsigned 16-bit integer
9	CS1_RawCount_LSB	–
10	CS2_RawCount_MSB	Unsigned 16-bit integer
11	CS2_RawCount_LSB	–
12	CS3_RawCount_MSB	Unsigned 16-bit integer
13	CS3_RawCount_LSB	–
14	CS_Status	Gives CapSense button status, least significant bit (LSB) contains CS0 status
15	GPO_Status	Gives GPO status, LSB contains GPO0 status
16	0x00	–
17	CS1_Cp	CS1 parasitic capacitance in Hex
18	CS0_Baseline_MSB	Unsigned 16-bit integer
19	CS0_Baseline_LSB	–
20	CS1_Baseline_MSB	Unsigned 16-bit integer
21	CS1_Baseline_LSB	–
22	CS2_Baseline_MSB	Unsigned 16-bit integer
23	CS2_Baseline_LSB	–
24	CS3_Baseline_MSB	Unsigned 16-bit integer
25	CS3_Baseline_LSB	–
26	0x00	–
27	CS2_Cp	CS2 parasitic capacitance in Hex
28	0x00	–
29	CS3_Cp	CS3 parasitic capacitance in Hex
30	CS0_DiffCount_MSB	Unsigned 16-bit integer
31	CS0_DiffCount_LSB	–
32	CS1_DiffCount_MSB	Unsigned 16-bit integer
33	CS1_DiffCount_LSB	–
34	CS2_DiffCount_MSB	Unsigned 16-bit integer
35	CS2_DiffCount_LSB	–
36	CS3_DiffCount_MSB	Unsigned 16-bit integer
37	CS3_DiffCount_LSB	–
38	0x00	Dummy data for multi chart
39	0xFF	
40	0xFF	

## Power Consumption and Device Operating Modes

The CY8CMBR2044 is designed to meet the low power requirements of battery powered applications. To design for the lowest operating current -

- Ground all unused CapSense inputs
- Minimize  $C_p$  using the design guidelines in [Getting Started with CapSense](#), section 3.7.1.
- Lower the supply voltage.
- Use a higher Button Scan Rate or Deep Sleep operating mode.

To know more about the steps to reduce power consumption, refer to [CY8CMBR2044 Design Guide](#), section 5.

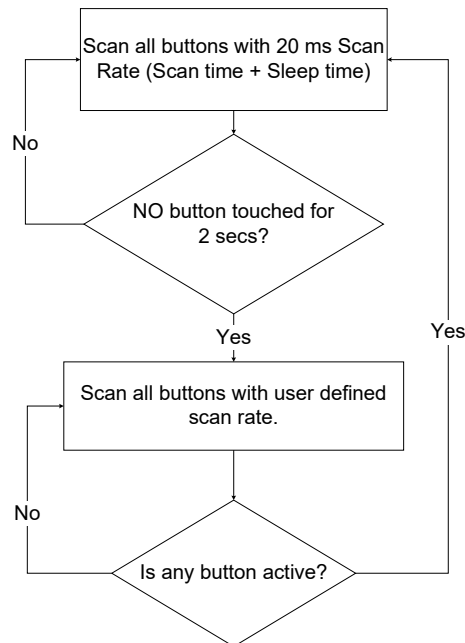
There are two device operating modes:

- Low power sleep mode
- Deep sleep mode

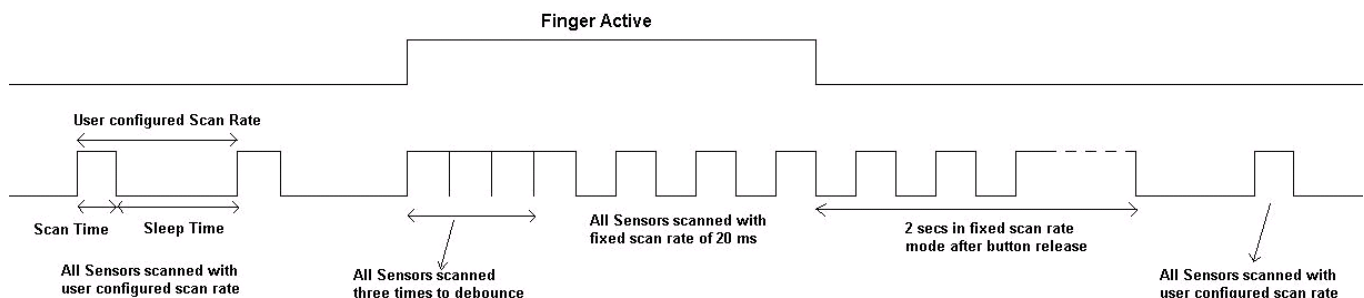
### Low Power Sleep Mode

The following flow chart describes the low power sleep mode operation.

**Figure 10. Low Power Sleep Mode Operation**

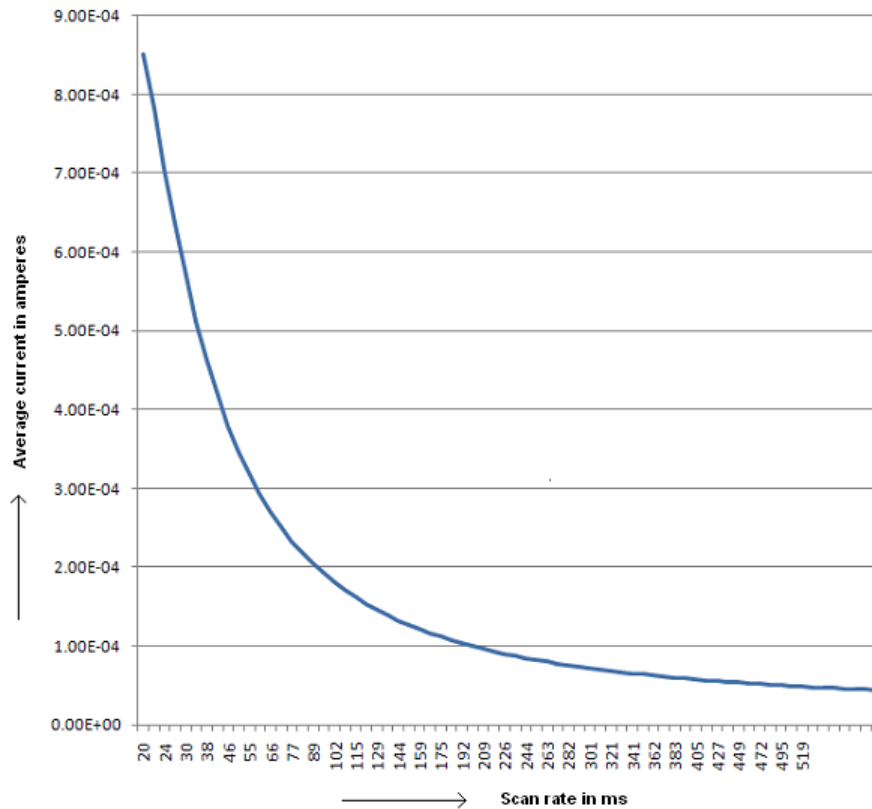


**Figure 11. Low Power Sleep Mode Implementation**



- To enable low power sleep mode, the hardware configurable pin ScanRate/Sleep should be pulled down to ground with resistor 'R' (1%). The scan rate values for different resistor values are given in Table 18 in Appendix.
- If the ScanRate/Sleep pin is pulled to ground without any resistor, the Button Scan Rate is set to 20 ms. The device operates in low power sleep mode, unless a button is touched.
- The range of scan rate is 20 to 530 ms.

**Figure 12. Average Current vs Scan Rate** <sup>[4]</sup>

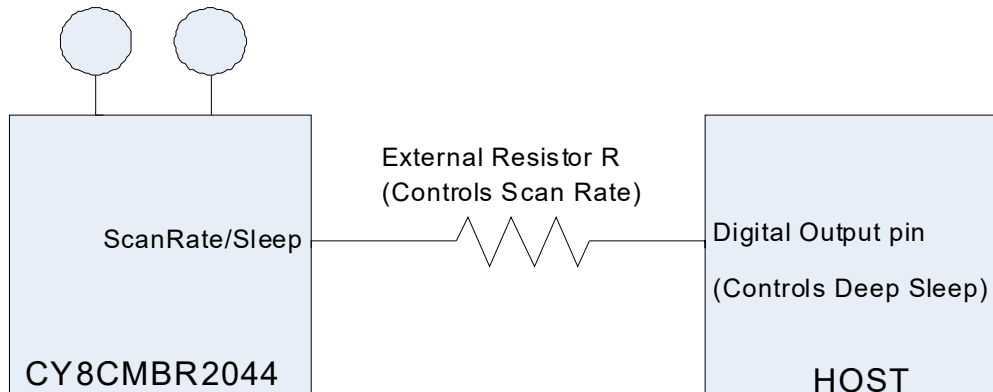


**Note**

4. Number of sensors = 3,  $C_p < 19$  pF, 0% touch time,  $V_{DD} = 3$  V.

### Deep Sleep Mode

**Figure 13. ScanRate/Sleep Pin Connection to Enable Deep Sleep Mode**



- To enable the deep sleep mode, the hardware configuration pin ScanRate/Sleep should be connected to the master device as shown in [Figure 13](#).
- Host controller should pull the pin to  $V_{DD}$  for the device to go into deep sleep.
- The Host controller output pin should be in Strong drive mode, so that the ScanRate/Sleep pin is not left floating.
- In deep sleep mode, all blocks are turned off and the device current consumption is approximately 0.1  $\mu A$ .
- There is no CapSense scanning in deep sleep mode.
- ScanRate/Sleep pin should be pulled low for the device to wake up from deep sleep.
- When device comes out of deep sleep mode, the CapSense system is reinitialized. Typical time for reinitialization is 8 ms. Any button touch within this time is not reported.
- After the device comes out of deep sleep, the device operates in low power sleep mode.
- If the ScanRate/Sleep pin is pulled high at power on, then the device does not go to deep sleep immediately. The device goes to deep sleep after initializing all internal blocks and scanning all buttons once.
- If the ScanRate/Sleep pin is pulled high at power on, then the button scan rate is calculated when the device is taken out of Deep Sleep by the master.

### Additional Components to Enable Advanced Features

S.No.	Feature	Resistors required	Notes
1	Low power sleep and deep sleep	1	Deep sleep is controlled by a master device. When the device comes out of deep sleep, it enters into low power sleep mode based on settings. Resistor is not required if both features are not used.
2	Toggle/FSS	1	To enable both the features only one resistor is required. Resistor is not required if both features are not used.
3	LED ON time	1	Resistor is not required if the feature is not used.
4	Sensor auto reset	1	Resistor is not required if the feature is not used.

### Response Time

Response time is the minimum amount of time the button should be touched for the device to detect as valid button press.

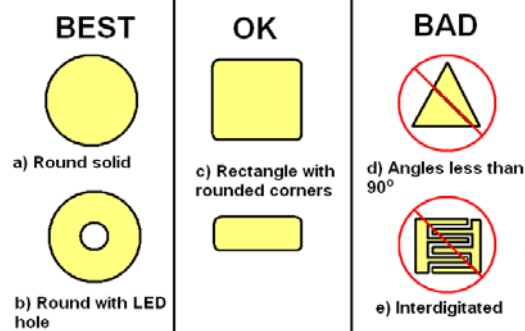
Condition	Response time (in ms)
First button press	Button Scan rate value + 20. For button scan rate value, see <a href="#">Table 18</a> in <a href="#">Appendix</a> .
Consecutive button press after first button press	80

## Layout Guidelines and Best Practices

S.No.	Category	Min	Max	Recommendations / Remarks
1	Button shape	–	–	Solid round pattern, round with LED hole, rectangle with round corners
2	Button size	5 mm	15 mm	Refer <a href="#">Design Toolbox</a>
3	Button-button spacing	Equal to Button Ground Clearance	–	8 mm (Y dimension in <a href="#">Button Layout Design on page 16</a> )
4	Button ground clearance	0.5 mm	2 mm	Refer <a href="#">Design Toolbox</a> (X dimension in <a href="#">Button Layout Design on page 16</a> )
5	Ground flood – top layer	–	–	Hatched ground 7 mil trace and 45 mil grid (15% filling)
6	Ground flood – bottom layer	–	–	Hatched ground 7 mil trace and 70 mil grid (10% filling)
7	Trace length from button pad to CapSense controller pins	–	450 mm	Refer <a href="#">Design Toolbox</a>
8	Trace width	0.17 mm	0.20 mm	0.17 mm (7 mil)
9	Trace routing	–	–	Traces should be routed on the non button side. If any non CapSense trace crosses CapSense trace, ensure that intersection is orthogonal
10	Via position for the buttons	–	–	Via should be placed near the edge of the button to reduce trace length thereby increasing sensitivity
11	Via hole size for button traces	–	–	10 mil
12	No. of via on button trace	1	2	1
13	Distance of CapSense series resistor from button pin	–	10 mm	Place CapSense series resistors close to the device for noise suppression. CapSense resistors have highest priority; place them first
14	Distance between any CapSense trace to ground flood	10 mil	20 mil	20 mil
15	Device placement	–	–	Mount the device on the layer opposite to button. The CapSense trace length between the device and buttons should be minimum (see trace length above)
16	Placement of components in two layer PCB	–	–	Top layer – buttons and bottom layer – device, other components and traces
17	Placement of components in four layer PCB	–	–	Top layer – buttons, second layer – CapSense traces and V <sub>DD</sub> (avoid V <sub>DD</sub> traces below the buttons), third layer – hatched ground, bottom layer – CapSense IC or device, other components, and non CapSense traces
18	Overlay thickness	0 mm	5 mm	Refer <a href="#">Design Toolbox</a>
19	Overlay material	–	–	Should be non-conductive material. Glass, ABS plastic, formica, wood, and so on. There should be no air gap between PCB and overlay. Use adhesive to stick the PCB and overlay
20	Overlay adhesives	–	–	Adhesive should be non conductive and dielectrically homogenous. 467MP and 468MP adhesives made by 3M are recommended
21	LED back lighting	–	–	Cut a hole in the button pad and use rear mountable LEDs. Refer to <a href="#">Example PCB Layout Design with Four CapSense Buttons and Four LEDs on page 17</a>
22	Board thickness	–	–	Standard board thickness for CapSense FR4 based designs is 1.6 mm.

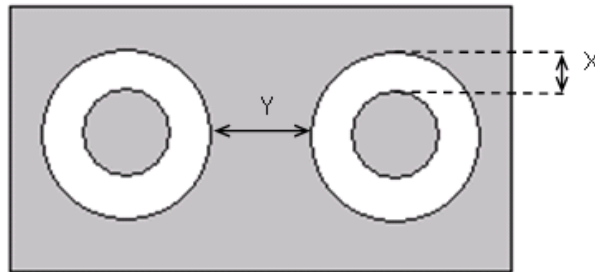
## CapSense Button Shapes

**Figure 14. CapSense Button Shapes**



## Button Layout Design

**Figure 15. Button Layout Design**

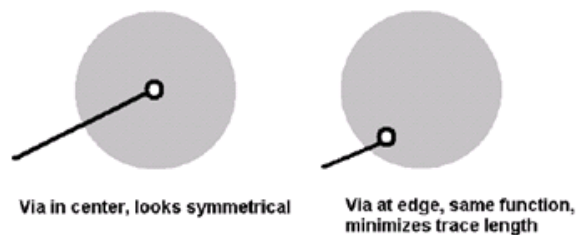


X: Button to ground clearance (Refer to [Layout Guidelines and Best Practices on page 15](#))

Y: Button to button clearance (Refer to [Layout Guidelines and Best Practices on page 15](#))

## Recommended Via Hole Placement

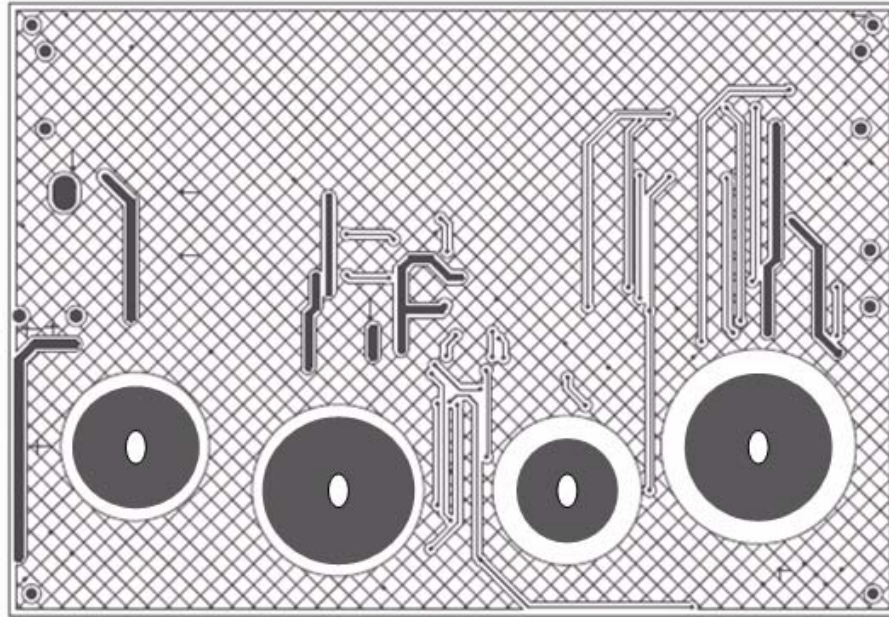
**Figure 16. Recommended Via Hole Placement**



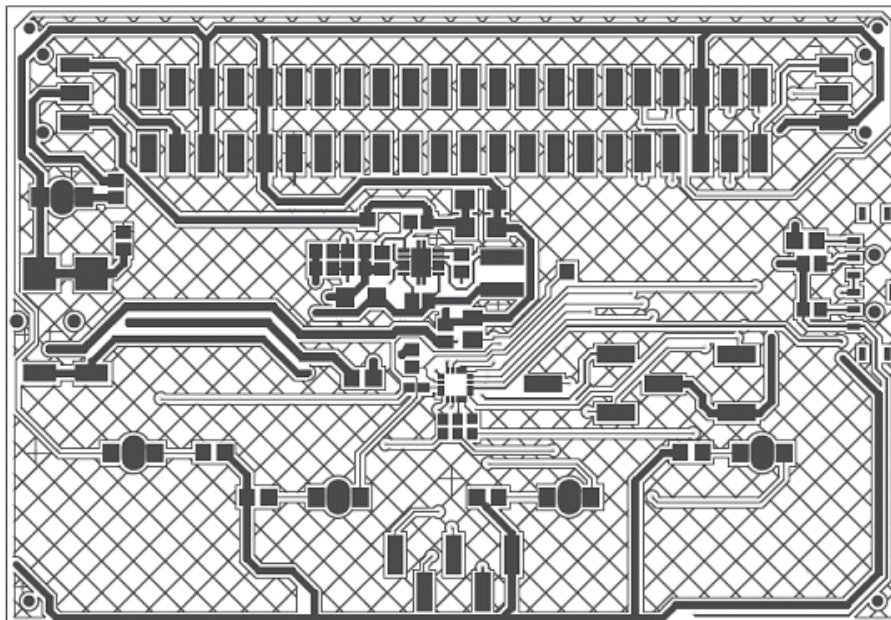


**Example PCB Layout Design with Four CapSense Buttons and Four LEDs**

**Figure 17. Top Layer**



**Figure 18. Bottom Layer**





## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CMBR2044 device.

### Absolute Maximum Ratings

**Table 6. Absolute Maximum Ratings**

Parameter	Description	Min	Typ	Max	Unit	Notes
T <sub>STG</sub>	Storage temperature	–55	25	+125	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.
V <sub>DD</sub>	Supply voltage relative to V <sub>SS</sub>	–0.5	–	+6.0	V	
V <sub>IO</sub>	DC voltage on CapSense inputs and digital output pins	V <sub>SS</sub> – 0.5	–	V <sub>DD</sub> + 0.5	V	
I <sub>MIG</sub>	Maximum current into any GPO output pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	In accordance with JESD78 standard

### Operating Temperature

**Table 7. Operating Temperature**

Parameter	Description	Min	Typ	Max	Unit	Notes
T <sub>A</sub>	Ambient temperature	–40	–	+85	°C	
T <sub>J</sub>	Operational die temperature	–40	–	+100	°C	

## DC Electrical Characteristics

### DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 8. DC Chip Level Specifications**

Parameter	Description	Min	Typ	Max	Unit	Notes
$V_{DD}$ [5, 6, 7]	Supply voltage	1.71	—	5.5	V	
$I_{DD}$	Supply current	—	2.88	4.0	mA	Conditions are $V_{DD} = 3.0$ V, $T_A = 25$ °C
$I_{DA}$	Active current	—	2.88	4.0	mA	Conditions are $V_{DD} = 3.0$ V, $T_A = 25$ °C, continuous sensor scan
$I_{DS}$	Deep sleep current	—	0.1	0.5	μA	Conditions are $V_{DD} = 3.0$ V, $T_A = 25$ °C
$I_{AV1}$	Average current	—	40	—	μA	Conditions are $V_{DD} = 3.0$ V, $T_A = 25$ °C, 4 – buttons used, 0% touch time, $C_P$ of all sensors < 19 pF and scan rate = 530 ms
$I_{AV2}$	Average current	—	63	—	μA	Conditions are $V_{DD} = 3.0$ V, $T_A = 25$ °C, 4 – buttons used, 0% touch time, $C_P$ of all sensors > 19 pF and scan rate = 530 ms
$I_{AV3}$	Average current	—	1	—	mA	Conditions are $V_{DD} = 3.0$ V, $T_A = 25$ °C, 4 – buttons used, 100% touch time, $C_P$ of all sensors < 19 pF and scan rate = 20 ms
$I_{AV4}$	Average current	—	1.6	—	mA	Conditions are $V_{DD} = 3.0$ V, $T_A = 25$ °C, 4 – buttons used, 100% touch time, $C_P$ of all sensors > 19 pF and < 40 pF, scan rate = 20 ms

#### Notes

- When  $V_{DD}$  remains in the range from 1.75 V to 1.9 V for more than 50 μs, the slew rate when moving from the 1.75 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μs. This helps to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the  $SR_{POWER\_UP}$  parameter.
- After power down, ensure that  $V_{DD}$  falls below 100 mV before powering backup.
- For proper CapSense block functionality, if the drop in  $V_{DD}$  exceeds 5% of the base  $V_{DD}$ , the rate at which  $V_{DD}$  drops should not exceed 200 mV/s. Base  $V_{DD}$  can be between 1.8 V and 5.5 V

### DC General Purpose I/O Specifications

These tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 9. 3.0 V to 5 V DC General Purpose I/O Specifications**

Parameter <sup>[8]</sup>	Description	Min	Typ	Max	Unit	Notes
V <sub>OH1</sub>	High output voltage on GP0, GP1, GP2, GP3	V <sub>DD</sub> – 0.2	–	–	V	I <sub>OH</sub> < 10 µA, maximum of 40 µA source current in all I/Os
V <sub>OH2</sub>	High output voltage on GP0, GP1	V <sub>DD</sub> – 0.9	–	–	V	I <sub>OH</sub> = 1 mA, maximum of 2 mA source current in all I/Os
V <sub>OH3</sub>	High output voltage on GP2, GP3	V <sub>DD</sub> – 0.9	–	–	V	I <sub>OH</sub> = 5 mA, maximum of 10 mA source current in all I/Os
V <sub>OL</sub>	Low output voltage	–	–	0.75	V	I <sub>OL</sub> = 25 mA/pin, V <sub>DD</sub> > 3.30, maximum of 60 mA sink current on GP00, GP01, GP02, GP03
R <sub>PD</sub>	XRES internal pull-down	3.7	4.8	6.2	kΩ	–

**Table 10. 2.4 V to 3.0 V DC General Purpose I/O Specifications**

Parameter <sup>[8]</sup>	Description	Min	Typ	Max	Unit	Notes
V <sub>OH1</sub>	High output voltage on GP0, GP1, GP2, GP3	V <sub>DD</sub> – 0.2	–	–	V	I <sub>OH</sub> < 10 µA, maximum of 40 µA source current in all I/Os
V <sub>OH2</sub>	High output voltage on GP0, GP1	V <sub>DD</sub> – 0.4	–	–	V	I <sub>OH</sub> = 0.2 mA, maximum of 0.4 mA source current in all I/Os
V <sub>OH3</sub>	High output voltage on GP2, GP3	V <sub>DD</sub> – 0.5	–	–	V	I <sub>OH</sub> = 2 mA, maximum of 4 mA source current in all I/Os
V <sub>OL</sub>	Low output voltage	–	–	0.72	V	I <sub>OL</sub> = 10 mA/pin, maximum of 30 mA sink current on GP00, GP01, GP02, GP03

**Table 11. 1.71 V to 2.4 V DC General Purpose I/O Specifications**

Parameter <sup>[8]</sup>	Description	Min	Typ	Max	Unit	Notes
V <sub>OH1</sub>	High output voltage on GP0,GP1	V <sub>DD</sub> – 0.2	–	–	V	I <sub>OH</sub> = 10 µA, maximum of 20 µA source current in all I/Os
V <sub>OH2</sub>	High output voltage on GP0,GP1	V <sub>DD</sub> – 0.5	–	–	V	I <sub>OH</sub> = 0.5 mA, maximum of 1 mA source current in all I/Os
V <sub>OH3</sub>	High output voltage on GP2,GP3	V <sub>DD</sub> – 0.2	–	–	V	I <sub>OH</sub> = 100 µA, maximum of 200 µA source current in all I/Os
V <sub>OH4</sub>	High output voltage on GP2,GP3	V <sub>DD</sub> – 0.5	–	–	V	I <sub>OH</sub> = 2 mA, maximum of 4 mA source current in all I/Os
V <sub>OL</sub>	Low output voltage	–	–	0.4	V	I <sub>OL</sub> = 5 mA/pin, maximum of 20 mA sink current on GP00, GP01, GP02, GP03

#### Note

8. XRES pin input voltage ranges at various DC Specifications (VDD) listed below:  
 Minimum Input voltage for reset is 2V at 3.0 V to 5.5 V.  
 Minimum Input voltage for reset is 1.4V at 2.4 V to 3.0 V.  
 Minimum Input voltage for reset is 0.65 × VDD at 1.71 V to 2.4 V.

## AC Electrical Specifications

### AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 12. AC Chip-Level Specifications**

Parameter	Description	Min	Max	Unit	Notes
SR <sub>POWER_UP</sub>	Power supply slew rate	–	250	V/ms	V <sub>DD</sub> slew rate during power up
T <sub>XRST</sub>	External reset pulse width at power up	1	–	ms	After supply voltage is valid
T <sub>XRST2</sub>	External reset pulse width after power-up	10	–	μs	Applies after part has booted

### AC General Purpose I/O Specifications

**Table 13. AC General Purpose I/O Specifications**

Parameter	Description	Min	Typ	Max	Unit	Notes
TRise1	Rise time on GPO0 and GPO1, Cload = 50 pF	15	–	80	ns	V <sub>DD</sub> = 3.0 to 3.6 V, 10%–90%
TRise2	Rise time on GPO2 and GPO3, Cload = 50 pF	10	–	50	ns	V <sub>DD</sub> = 3.0 to 3.6 V, 10%–90%
TRise3	Rise time on GPO0 and GPO1, Cload = 50 pF	15	–	80	ns	V <sub>DD</sub> = 1.71 to 3.0V, 10%–90%
TRise2	Rise time on GPO2 and GPO3, Cload = 50 pF	10	–	80	ns	V <sub>DD</sub> = 1.71 to 3.0 V, 10%–90%
TRise4	Fall time, Cload = 50 pF all GPO outputs	10	–	50	ns	V <sub>DD</sub> = 3.0 to 3.6 V, 90%–10%
TFall2	Fall time, Cload = 50 pF all GPO outputs	10	–	70	ns	V <sub>DD</sub> = 1.71 to 3.0 V, 90%–10%

## CapSense Specifications

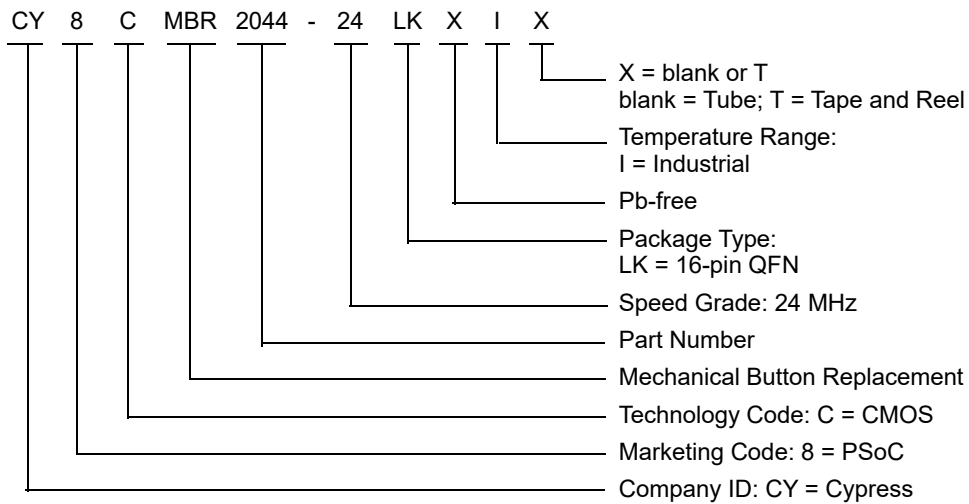
**Table 14. CapSense Specifications**

Parameter	Description	Min	Typ	Max	Unit	Notes
C <sub>P</sub>	Parasitic capacitance	5.0	–	(C <sub>P</sub> +C <sub>F</sub> ) < 40	pF	C <sub>P</sub> is the total capacitance seen by the pin when no finger is present. C <sub>P</sub> is sum of C <sub>BUTTON</sub> , C <sub>TRACE</sub> , and Capacitance of the vias and C <sub>PIN</sub>
C <sub>F</sub>	Finger capacitance	0.25	–	(C <sub>P</sub> +C <sub>F</sub> ) < 40	pF	C <sub>F</sub> is the capacitance added by the finger touch
C <sub>PIN</sub>	Capacitive load on pins as input	0.5	1.7	7	pF	
C <sub>MOD</sub>	External modulator capacitor	2	2.2	2.4	nF	Mandatory for CapSense to work
R <sub>s</sub>	Series resistor between pin and the sensor	–	560	616	Ω	Reduces the RF noise
T <sub>SCAN</sub>	Time which the device takes from the power applied to start of scanning	–	180	–	ms	

## Ordering Information

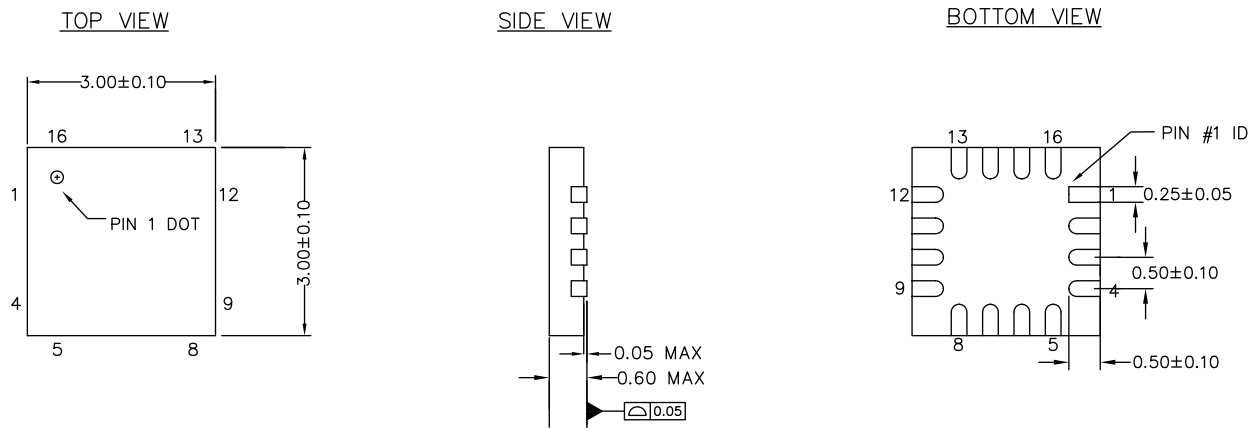
Ordering Code	Package Type	Operating Temperature	CapSense Inputs	GPOs	XRES Pin
CY8CMBR2044-24LKXI	16-pin QFN (3 × 3 × 0.6 mm)	Industrial	4	4	Yes
CY8CMBR2044-24LKXIT	16-pin QFN (3 × 3 × 0.6 mm) (Tape and Reel)	Industrial	4	4	Yes

## Ordering Code Definitions



## Package Diagram

**Figure 19. 16-pin Chip On Lead (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116**



### NOTES

1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 \*J

## Package Information

**Table 15. Thermal Impedances by Package**

Package	Typical $\theta_{JA}$ <sup>[9]</sup>
16-pin QFN	32.7 °C/W

**Table 16. Solder Reflow Peak Temperature**

Package	Minimum Peak Temperature <sup>[10]</sup>	Maximum Peak Temperature
16-pin QFN	240 °C	260 °C

### Notes

9.  $T_J = T_A + \text{Power} \times \theta_{JA}$

10. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

## Appendix

**Table 17. Device Features vs. Resistor Configuration Matrix**

Features	Comments		Pin Configuration	Device Pin Name
Button Auto Reset	Enabled, Auto Reset Period = 5 sec		Ground / Floating	ARST
	Enabled, Auto Reset Period = 20 sec		5.1 k $\Omega$ ( $\pm 5\%$ ) to ground	
	Disabled		VDD	
LED ON Time	0 ms		Ground	Delay
	20 ms		120 $\Omega$ ( $\pm 1\%$ ) to ground	
	40 ms		200 $\Omega$ ( $\pm 1\%$ ) to ground	
	60 ms		280 $\Omega$ ( $\pm 1\%$ ) to ground	
	.....		.....	
	1980 ms		7060 $\Omega$ ( $\pm 1\%$ ) to ground	
	2000 ms		8040 $\Omega$ ( $\pm 1\%$ ) to ground	
	2000 ms		> 8040 $\Omega$ ( $\pm 1\%$ ) to ground	
	2000 ms		VDD / Floating	
Toggle ON/OFF / Flanking Sensor Suppression (FSS)	<b>Toggle ON/OFF</b>	<b>FSS</b>		Toggle/FSS
	Disabled	Disabled	Ground / Floating	
	Enabled	Disabled	1.5 k $\Omega$ ( $\pm 5\%$ ) to ground	
	Disabled	Enabled	5.1 k $\Omega$ ( $\pm 5\%$ ) to ground	
	Enabled	Enabled	VDD	

**Table 18. ScanRate/Sleep Pin Hardware Configuration**

Resistor R (1%) in ohms	Approximate ScanRate (in ms)	Resistor R (1%) in ohms	Approximate ScanRate (in ms)
60	20	4060	209
185	22	4185	217
310	24	4310	226
435	27	4435	235
560	30	4560	244
685	34	4685	253
810	38	4810	263
935	42	4935	272
1060	46	5060	282
1185	51	5185	291
1310	55	5310	301
1435	61	5435	311
1560	66	5560	321
1685	71	5685	331
1810	77	5810	341
1935	83	5935	352
2060	89	6060	362
2185	96	6185	373
2310	102	6310	383
2435	107	6435	394
2560	115	6560	405
2685	122	6685	416
2810	129	6810	427
2935	137	6935	438
3060	144	7060	449
3185	152	7185	461
3310	159	7310	472
3435	167	7435	484
3560	175	7560	495
3685	183	7685	507
3810	192	7810	519
3935	200	7935	531



## Acronyms

Acronym	Description
AC	Alternating Current
AI	Analog Input
AIO	Analog Input/Output
AIDO	Analog Input/Digital Output
DO	Digital Output
P	Power pins
C <sub>F</sub>	Finger Capacitance
C <sub>P</sub>	Parasitic Capacitance
CS	CapSense
FSS	Flanking Sensor Suppression
GPO	General Purpose Output
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed Circuit Board
POR	Power On Reset
POST	Power On Self Test
RF	Radio Frequency

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
μA	microampere
μs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
Ω	ohm
pF	picofarad
V	volt

### Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or '0x' are decimal.

## Document History Page

Document Title: CY8CMBR2044, Four Button CapSense® Controller Document Number: 001-57451				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2807997	SLAN	12/03/2009	New data sheet.
*A	2949368	SLAN	06/10/2010	Updated <a href="#">Features</a> . Updated <a href="#">Functional Description</a> . Updated <a href="#">Pinout</a> . Updated <a href="#">Typical Circuits</a> (Updated <a href="#">Schematic 1: 4-Buttons, 4-LEDs with Auto Reset Enabled</a> and <a href="#">Schematic 2: 3-Buttons, 3-LEDs, 2-Outputs to Master, and Advanced Features Enabled</a> ). Updated <a href="#">Device Features</a> (Added <a href="#">Table 2</a> , updated Hardware Configuration (description), updated <a href="#">Flanking Sensor Suppression (FSS)</a> (Added <a href="#">Figure 2</a> ), updated <a href="#">System Diagnostics</a> (Added <a href="#">Figure 6</a> , and <a href="#">Figure 8</a> ), added <a href="#">Serial Debug Data</a> ). Updated <a href="#">Power Consumption and Device Operating Modes</a> (Updated <a href="#">Deep Sleep Mode</a> (description)). Updated <a href="#">Layout Guidelines and Best Practices</a> (Updated <a href="#">CapSense Button Shapes</a> , updated <a href="#">Example PCB Layout Design with Four CapSense Buttons and Four LEDs</a> ). Updated <a href="#">Electrical Specifications</a> . Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Units of Measure</a> .
*B	2975370	SLAN	07/09/2010	Updated <a href="#">Features</a> . Updated <a href="#">Pinout</a> . Updated <a href="#">Typical Circuits</a> . Updated <a href="#">Device Features</a> (Updated <a href="#">LED ON Time</a> (Updated <a href="#">Figure 4</a> ), updated <a href="#">System Diagnostics</a> (Updated <a href="#">Figure 6</a> , and <a href="#">Figure 8</a> ), updated <a href="#">Serial Debug Data</a> (description)). Updated <a href="#">Power Consumption and Device Operating Modes</a> (Updated <a href="#">Deep Sleep Mode</a> (description)).
*C	2996393	SLAN	07/29/2010	Updated <a href="#">Features</a> .
*D	3036873	ARVM	09/23/2010	Updated <a href="#">Typical Circuits</a> (Updated <a href="#">Schematic 1: 4-Buttons, 4-LEDs with Auto Reset Enabled</a> and <a href="#">Schematic 2: 3-Buttons, 3-LEDs, 2-Outputs to Master, and Advanced Features Enabled</a> ). Updated <a href="#">Layout Guidelines and Best Practices</a> (Updated <a href="#">Example PCB Layout Design with Four CapSense Buttons and Four LEDs</a> (Updated <a href="#">Figure 17</a> )).

**Document History Page** (continued)

Document Title: CY8CMBR2044, Four Button CapSense® Controller Document Number: 001-57451				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*E	3624224	UDYG / SLAN	05/22/2012	Updated Title to read as “Four Button CapSense® Controller”. Updated <a href="#">Features</a> . Updated <a href="#">Functional Description</a> . Updated <a href="#">Pinout</a> (Updated <a href="#">Table 1</a> ). Updated <a href="#">Typical Circuits</a> (Updated <a href="#">Schematic 1: 4-Buttons, 4-LEDs with Auto Reset Enabled</a> and <a href="#">Schematic 2: 3-Buttons, 3-LEDs, 2-Outputs to Master, and Advanced Features Enabled</a> ). Updated <a href="#">Device Features</a> (Updated <a href="#">Table 2</a> , updated <a href="#">CapSense Buttons</a> , updated <a href="#">SmartSense Auto Tuning</a> , updated <a href="#">General Purpose Outputs</a> , removed <a href="#">Hardware Configuration</a> , updated <a href="#">Toggle ON/OFF</a> , updated <a href="#">Flanking Sensor Suppression (FSS)</a> , removed <a href="#">Delay Off</a> , added <a href="#">LED ON Time</a> , updated <a href="#">Button Auto Reset</a> , renamed <a href="#">Failure Mode Analysis</a> as <a href="#">System Diagnostics</a> and updated the same section, renamed <a href="#">Debug Data</a> as <a href="#">Serial Debug Data</a> and updated the same section, renamed <a href="#">Device Operating Modes</a> as <a href="#">Power Consumption and Device Operating Modes</a> ). Updated <a href="#">Layout Guidelines and Best Practices</a> . Updated <a href="#">Electrical Specifications</a> (Updated <a href="#">DC Electrical Characteristics</a> (Updated <a href="#">DC Chip Level Specifications</a> (Updated <a href="#">Note 6</a> )), updated <a href="#">DC General Purpose I/O Specifications</a> ). Updated <a href="#">CapSense Specifications</a> . Updated <a href="#">Ordering Information</a> (Removed <a href="#">CapSense Block</a> column). Updated <a href="#">Package Diagram</a> . Added <a href="#">Appendix</a> . Replaced all instances of sensor with button across the document. Updated to new template.
*F	3907113	SEEE	02/19/2013	Updated <a href="#">Device Features</a> (Updated <a href="#">General Purpose Outputs</a> ). Updated <a href="#">Electrical Specifications</a> (Updated <a href="#">DC Electrical Characteristics</a> (Updated <a href="#">DC General Purpose I/O Specifications</a> (Added <a href="#">Note 8</a> and referred the same note in parameter column in <a href="#">Table 9</a> , <a href="#">Table 10</a> , <a href="#">Table 11</a> ))). Updated <a href="#">Package Diagram</a> : spec 001-09116 – Changed revision from *F to *G.
*G	4062936	VAIR	07/15/2013	Replaced “CS_Status” with “CS_Status” in all instances across the document. Updated <a href="#">Package Diagram</a> : spec 001-09116 – Changed revision from *G to *H. Updated to new template.
*H	5166555	SLAN	03/08/2016	Updated <a href="#">Device Features</a> : Updated <a href="#">Additional Components to Enable Advanced Features</a> : Replaced “Delay Off” with “LED ON time” in “Feature”. Updated <a href="#">Electrical Specifications</a> : Updated <a href="#">CapSense Specifications</a> : Added T <sub>SCAN</sub> parameter and its details. Updated <a href="#">Package Diagram</a> : spec 001-09116 – Changed revision from *H to *J. Updated <a href="#">Appendix</a> : Updated <a href="#">Table 17</a> : Replaced “5 ms” with “5 sec” and “20 ms” with “20 sec” in “Comments” column corresponding to “Button Auto Reset” feature. Updated to new template. Completing Sunset Review.
*I	5747736	AESATMP9	05/24/2017	Updated logo and copyright.
*J	6489930	JOBI	03/04/2019	Updated <a href="#">Serial Debug Data</a> . Updated <a href="#">Table 9</a> . Corrected the <a href="#">CY8CMBR2044 Design Guide</a> link. Updated Copyright information.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Arm® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless Connectivity	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

### Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2009-2019. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.