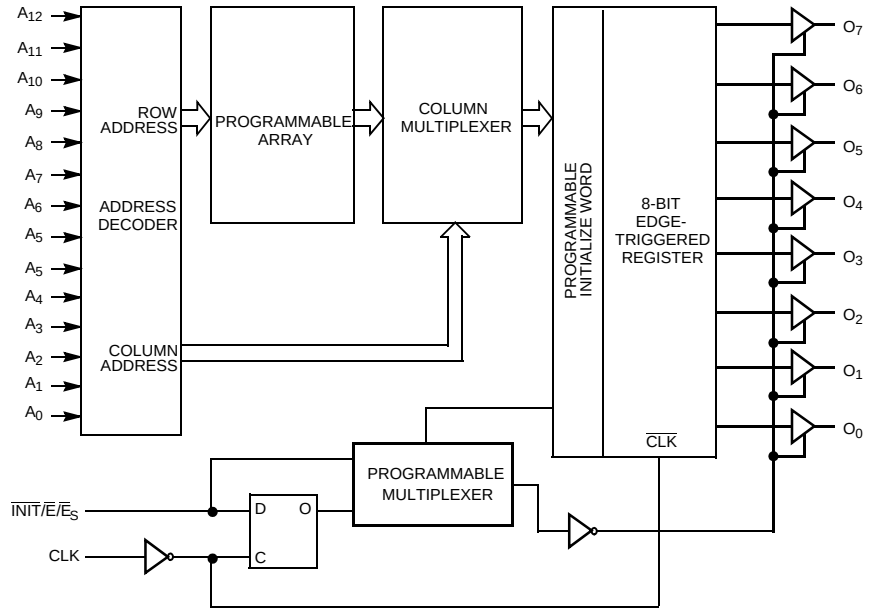
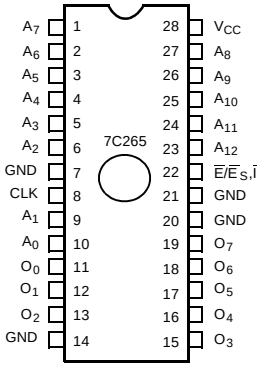
Logic Block Diagram

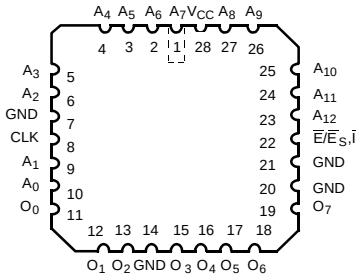


Pin Configurations

DIP/Flatpack Top View



LCC/PLCC (Opaque Only) Top View



Selection Guides

		7C265-15	7C265-25	7C265-40	7C265-50	Unit
Minimum Address Set-Up Time		15	25	40	50	ns
Maximum Clock to Output		12	15	20	25	ns
Maximum Operating Current	Com'l	120	120	100		mA
	Mil				120	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage..... –3.0V to +7.0V

DC Program Voltage..... 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	–55°C to +125°C	5V ±10%

Note
1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C265-15, 25		7C265-40		7C265-50		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4						V
		V_{CC} = Min., I_{OH} = –4.0 mA				2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4					V
		V_{CC} = Min., I_{OL} = 12.0 mA					0.4		0.4	
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil		0.4					
		V_{CC} = Min., I_{OL} = 8.0 mA							0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–40	+40	–40	+40	–40	+40	µA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		100			mA
			Mil						120	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

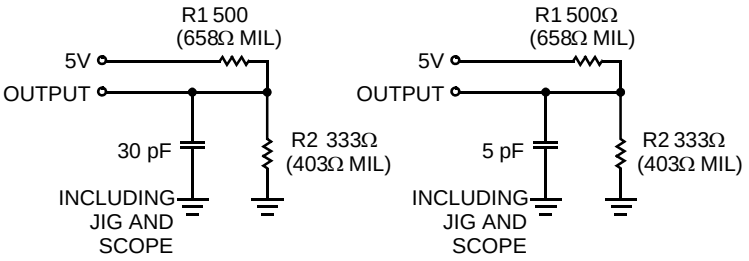
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

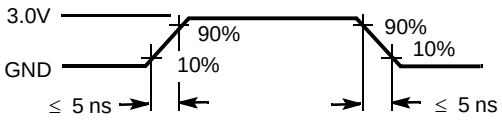
Notes
2. See the last page of this specification for Group A subgroup testing information.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms

Test Load for -15 through -25 speeds

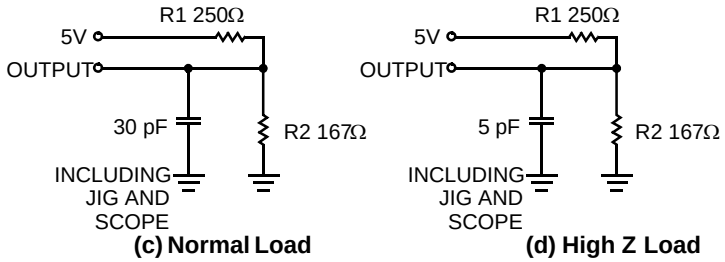


(a) Normal Load **(b) High Z Load**



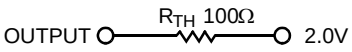
Equivalent to: THÉVENIN EQUIVALENT

Test Load for -40 through -50 speeds



(c) Normal Load **(d) High Z Load**

Equivalent to: THÉVENIN EQUIVALENT



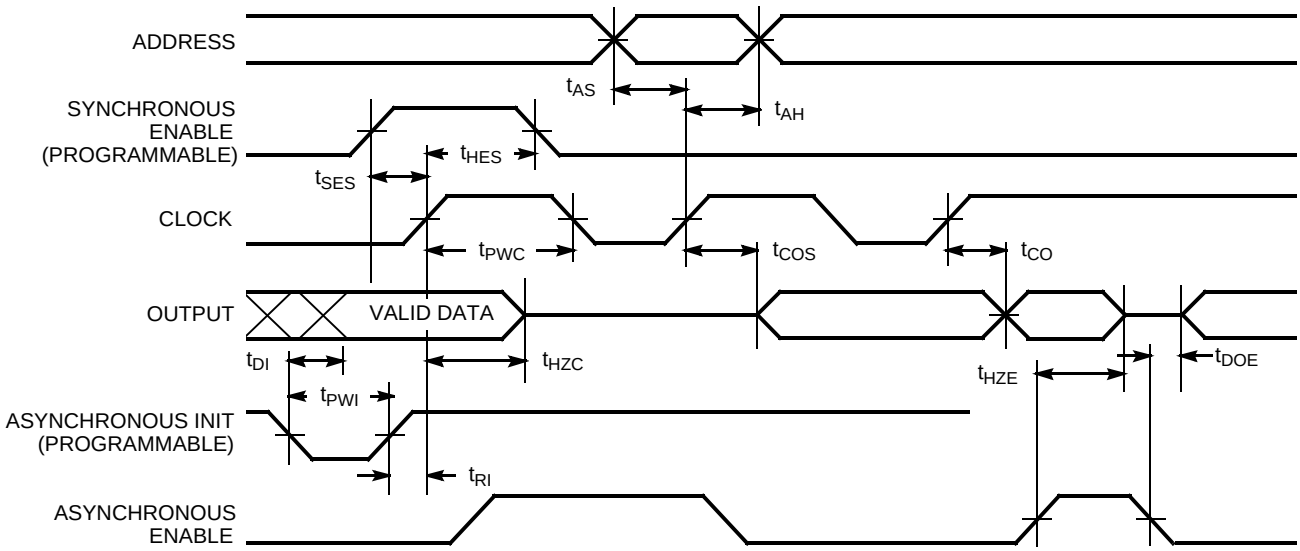
Switching Characteristics Over the Operating Range[2, 4]

Parameter	Description	7C265-15		7C265-25		7C265-40		7C265-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	15		25		40		50		ns
t_{HA}	Address Hold from Clock	0		0		0		0		ns
t_{CO}	Clock to Output Valid		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	12		15		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync. Enable Only)	12		15		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		5		ns
t_{DI}	$\overline{INIT}$ to Output Valid		15		18		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	12		15		20		25		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	12		15		25		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		12		15		20		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		12		15		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Async. Mode)		12		15		20		25	ns

Switching Characteristics Over the Operating Range[2, 4] (continued)

Parameter	Description	7C265-15		7C265-25		7C265-40		7C265-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		12		15		20		25	ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C265 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity • exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C265 needs to be within one inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Bit Map Data

Programmer Address (Hex.)		RAM Data
Decimal	Hex	Contents

Bit Map Data

0	0	Data
.	.	.
.	.	.
8191	1FFF	Data
8192	2000	INIT Byte
8193	2001	Control Byte

Control Byte

- 00 Asynchronous output enable (default condition)
- 01 Synchronous output enable
- 02 Asynchronous initialize

Programming Modes

The 7C265 offers a limited selection of programmed architectures. Programming these features should be done with a single 10-ms-wide pulse in place of the intelligent algorithm, mainly because these features are verified operationally, not with the $\overline{VFY}$ pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C265 architecture, VPP is applied to pins 3, 9, and 22. The choice of a particular mode depends on the states of the other pins during programming, so it is important that the condition of the other pins be met as set forth in the mode table. The considerations that apply with

respect to power-up and power-down during intelligent programming also apply during architecture programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling PGM from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

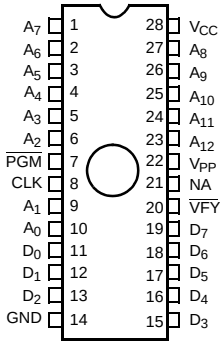
Table 1. Mode Selection

Mode	Read or Output Disable / Other	Pin Function						
	Read or Output Disable	A_{12}	A_{11}	A_{10}–A_7	A_6	A_5	A_4–A_3	A_2
	Other	A_{12}	A_{11}	A_{10}–A_7	A_6	A_5	A_4–A_3	A_2
Asynchronous Enable Read		A_{12}	A_{11}	A_{10}–A_7	A_6	A_5	A_4–A_3	A_2
Synchronous Enable Read		A_{12}	A_{11}	A_{10}–A_7	A_6	A_5	A_4–A_3	A_2
Asynchronous Initialization Read		A_{12}	A_{11}	A_{10}–A_7	A_6	A_5	A_4–A_3	A_2
Program Memory		A_{12}	A_{11}	A_{10}–A_7	A_6	A_5	A_4–A_3	A_2
Program Verify		A_{12}	A_{11}	A_{10}–A_7	A_6	A_5	A_4–A_3	A_2
Program Inhibit		A_{12}	A_{11}	A_{10}–A_7	A_6	A_5	A_4–A_3	A_2
Program Synchronous Enable		V_{IHP}	V_{IHP}	A_{10}–A_7	V_{IHP}	V_{PP}	A_4–A_3	V_{IHP}
Program Initialize		V_{ILP}	V_{IHP}	A_{10}–A_7	V_{IHP}	V_{PP}	A_4–A_3	V_{ILP}
Program Initial Byte		A_{12}	V_{ILP}	A_{10} – A_7	V_{IHP}	V_{PP}	A_4–A_3	V_{ILP}

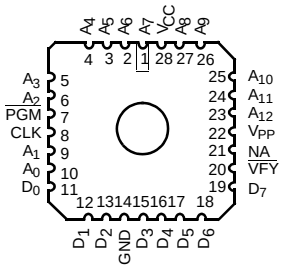
Mode	Read or Output Disable / Other	Pin Function						
	Read or Output Disable	A_1	A_0	GND	CLK	GND	$\overline{E}$, $\overline{I}$	O_7–O_0
	Other	A_1	A_0	$\overline{PGM}$	CLK	$\overline{VFY}$	V_{PP}	D_7–D_0
Asynchronous Enable Read		A_1	A_0	GND	V_{IL}	GND	V_{IL}	O_7–O_0
Synchronous Enable Read		A_1	A_0	GND	V_{IL}/V_{IH}	GND	V_{IL}	O_7–O_0
Asynchronous Initialization Read		A_1	A_0	GND	V_{IL}	GND	V_{IL}	O_7–O_0
Program Memory		A_1	A_0	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Program Verify		A_1	A_0	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	O_7–O_0
Program Inhibit		A_1	A_0	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Program Synchronous Enable		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Program Initialize		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Program Initial Byte		V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0

Figure 1. Programming Pinout

DIP/Flatpack



LCC/PLCC (Opaque Only)

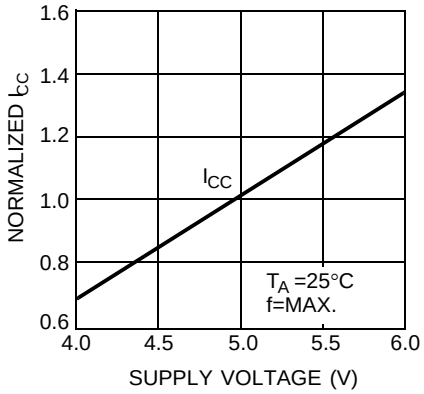


Programming Information

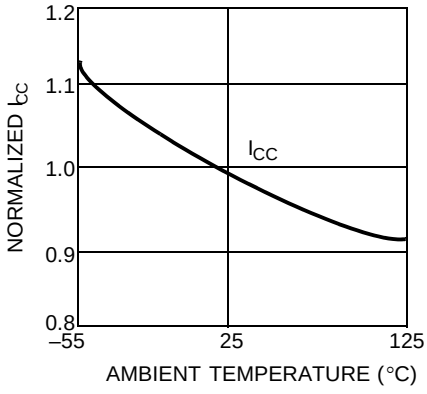
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Typical DC and AC Characteristics

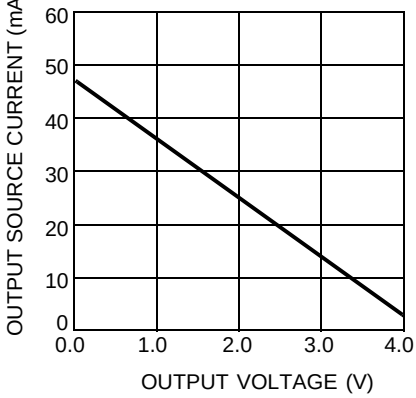
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



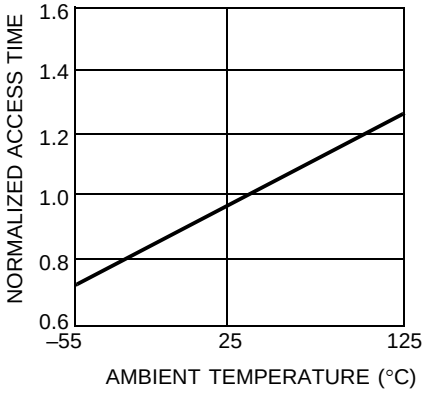
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



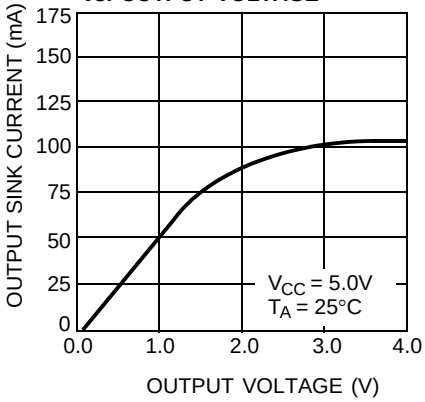
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



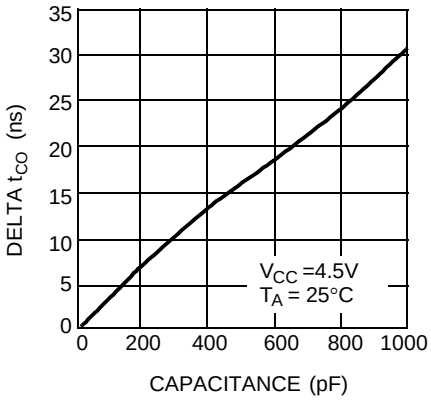
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



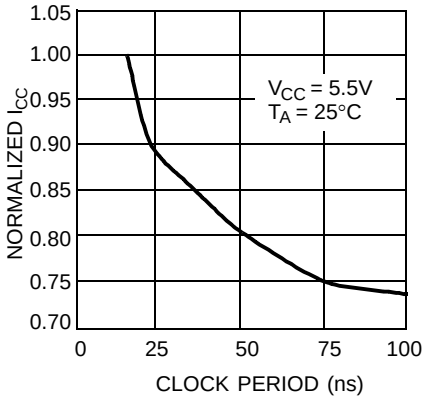
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	120	CY7C265-15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265-15WC	W22	28-Lead (300-Mil) Windowed CerDIP	
25	120	CY7C265-25WC	W22	28-Lead (300-Mil) Windowed CerDIP	Commercial
40	100	CY7C265-40PC	P21	28-Lead (300-Mil) Molded DIP	Commercial

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{PW}	7, 8, 9, 10, 11
t_{SES}	7, 8, 9, 10, 11
t_{HES}	7, 8, 9, 10, 11
t_{COS}	7, 8, 9, 10, 11

Package Diagrams

Figure 2. 28-Lead (300-Mil) CerDIP D22

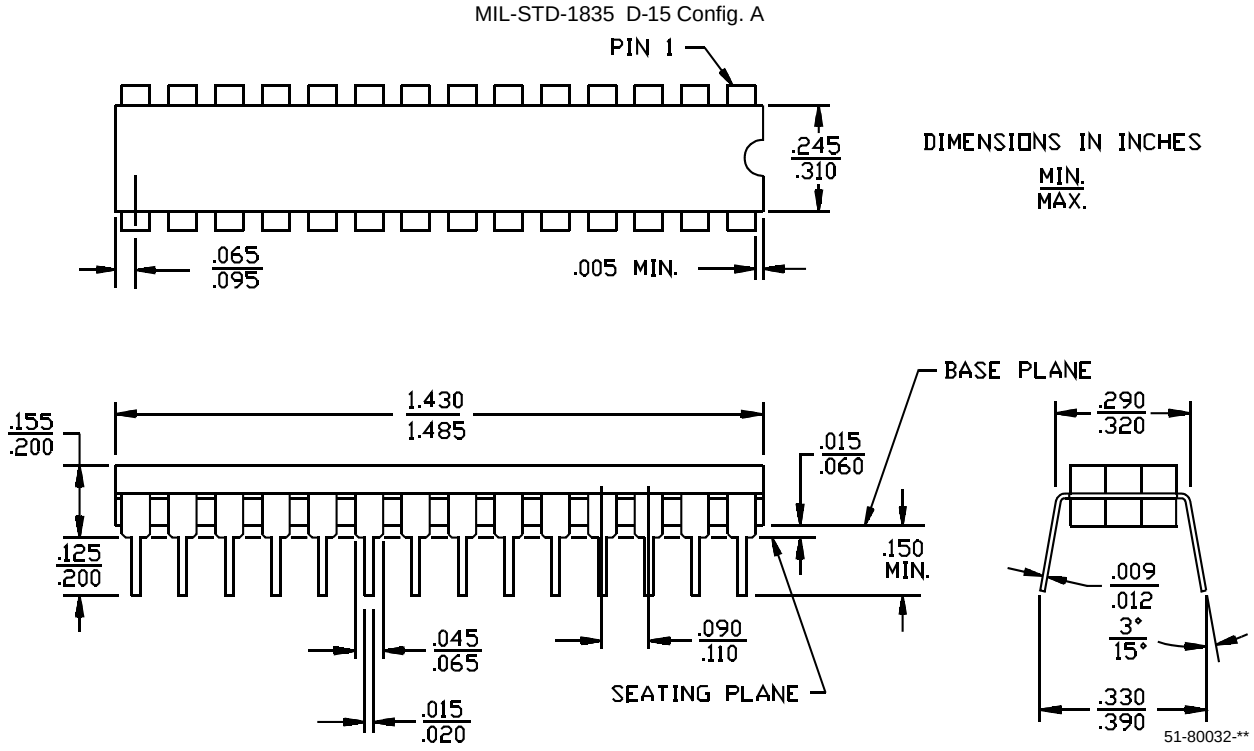
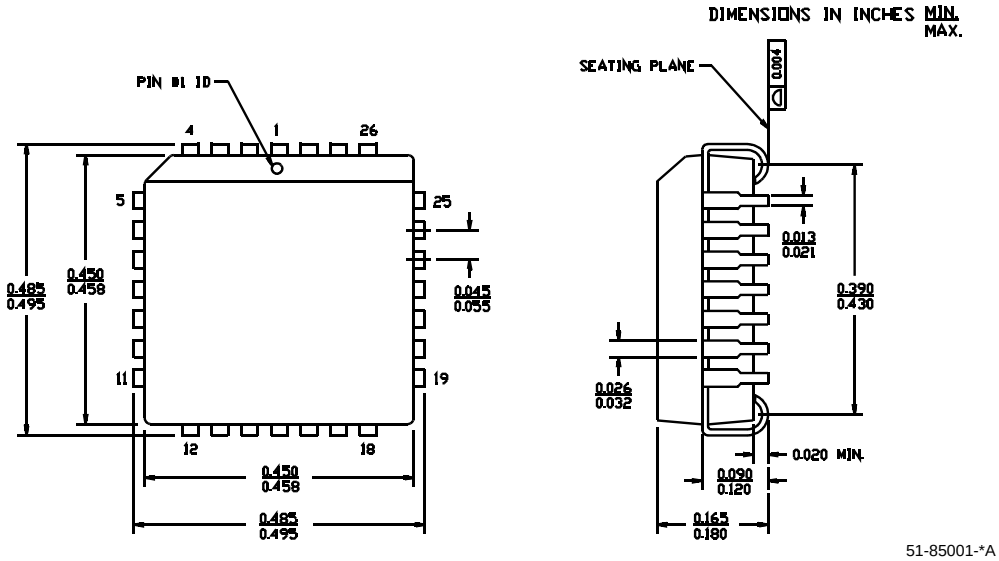
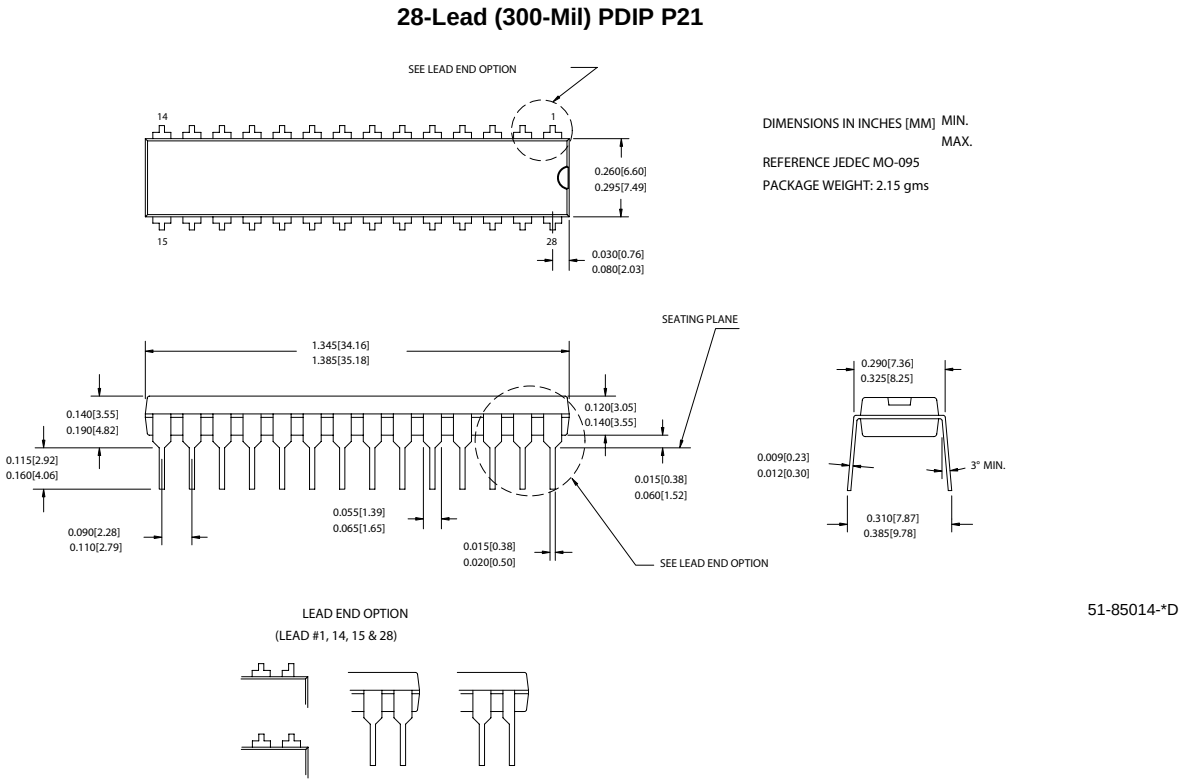


Figure 3. 28-Lead Plastic Leaded Chip Carrier J64



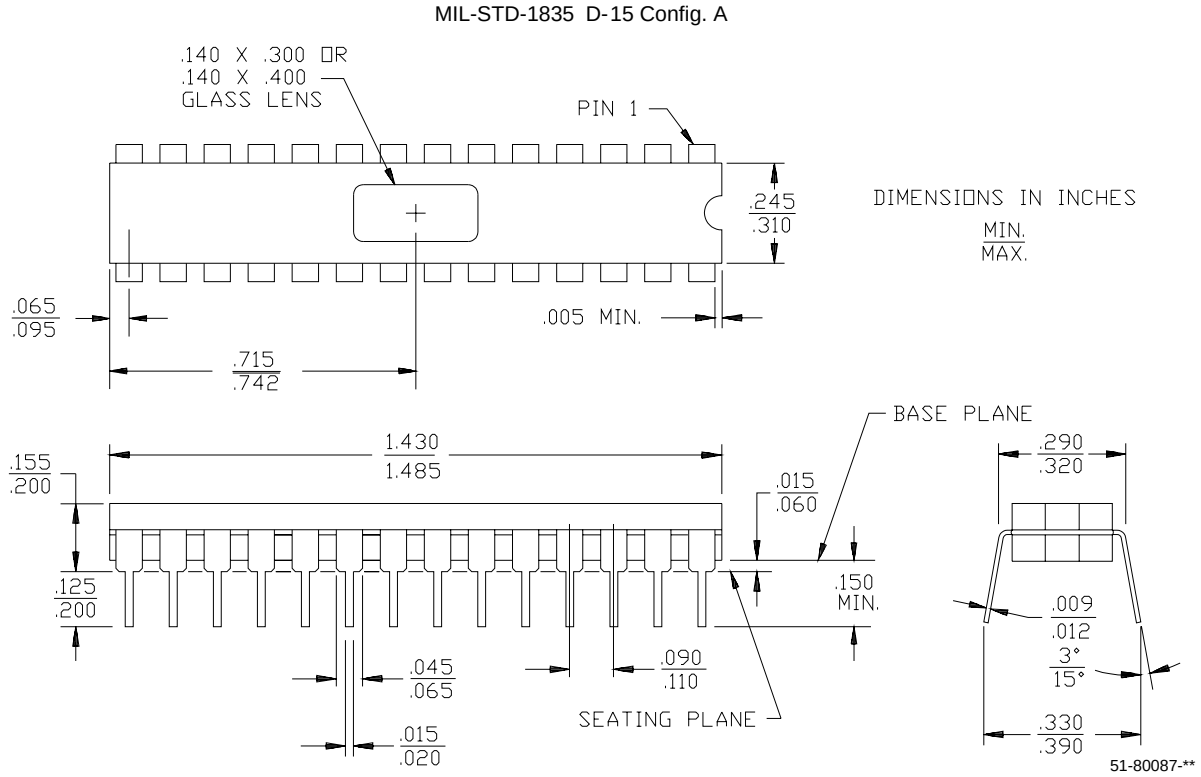
Package Diagrams (continued)

Figure 4. 28-Lead (300-Mil) Molded DIP P21



Package Diagrams (continued)

Figure 5. 28-Lead (300-Mil) Windowed CerDIP W22



Document History Page

Document Title: CY7C265 8K x 8 Registered PROM Document Number: 38-04012				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	114139	03/18/02	DSG	Changed from Spec number: 38-00084 to 38-04012
*A	118896	10/09/02	GBI	Updated ordering information
*B	499562	See ECN	PCI	Updated ordering information