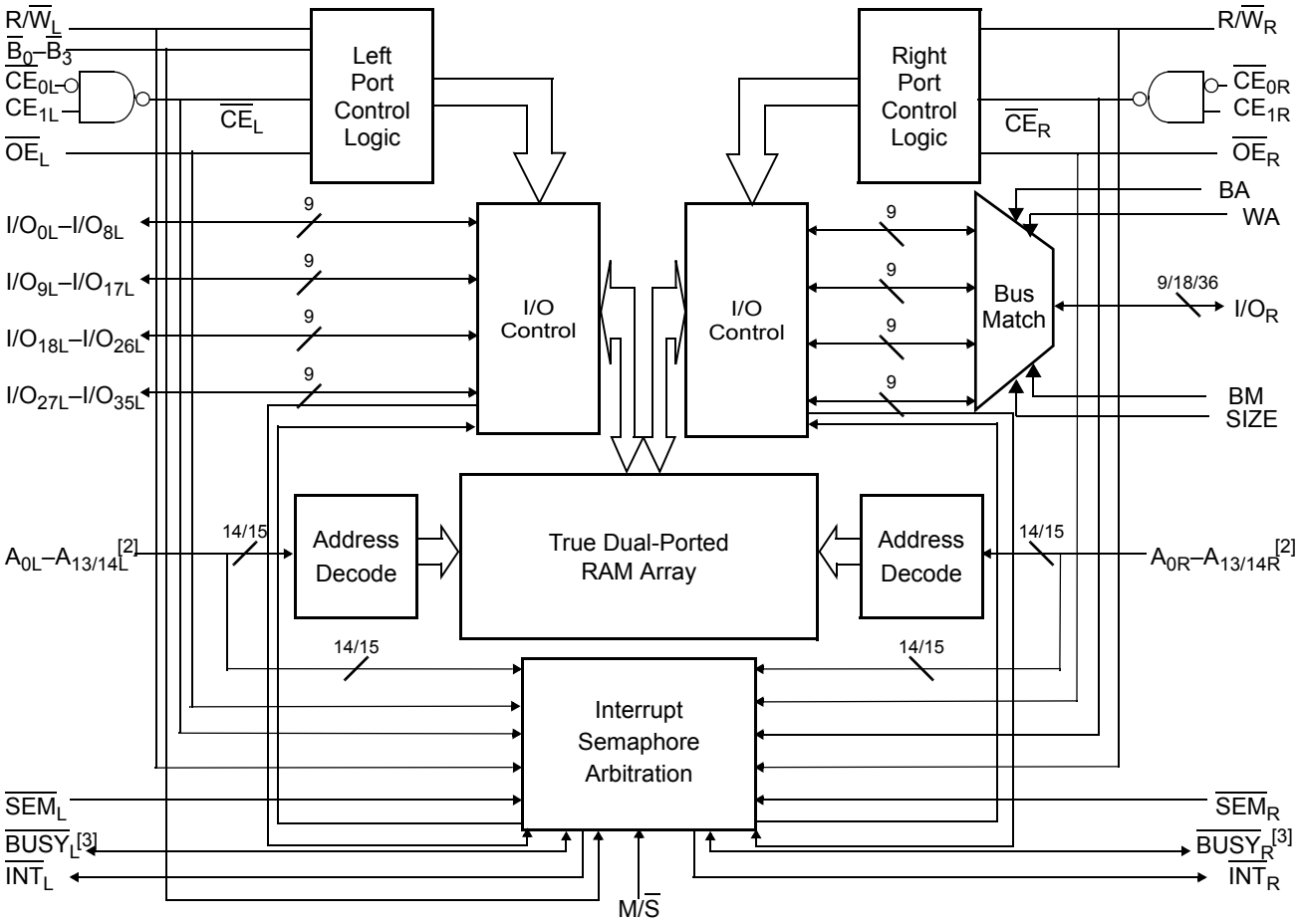
Logic Block Diagram

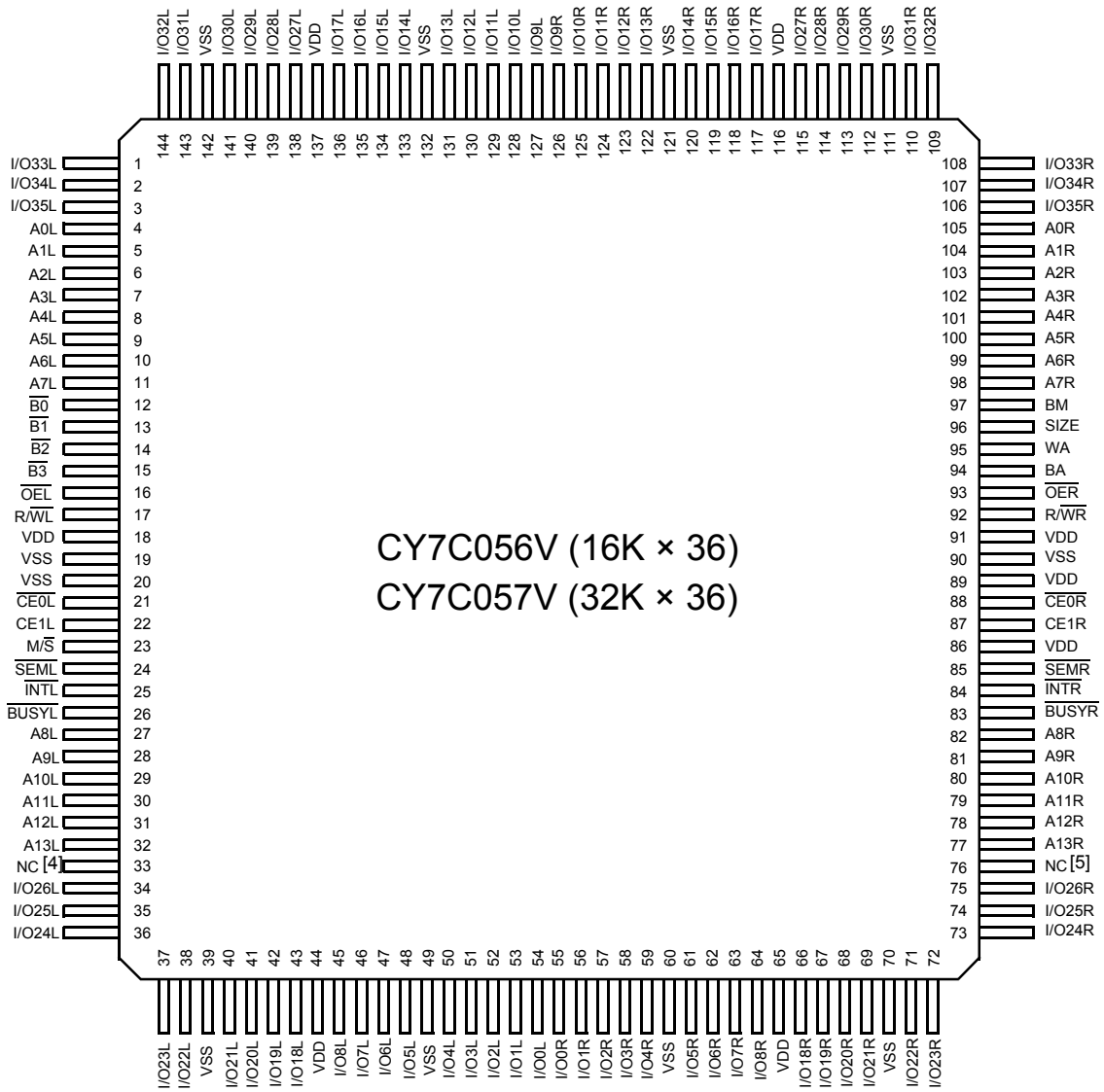


Notes
2. A_0–A_{13} for 16K; A_0–A_{14} for 32K devices.
3. BUSY is an output in Master mode and an input in Slave mode.

Contents

Pin Configurations

Figure 1. 144-pin TQFP pinout (Top View)



Notes
4. This pin is A14L for CY7C057V.
5. This pin is A14R for CY7C057V.

Pin Configurations (continued)

Figure 2. 172-ball BGA pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	I/O32L	I/O30L	NC	VSS	I/O13L	VDD	I/O11L	I/O11R	VDD	I/O13R	VSS	NC	I/O30R	I/O32R
B	A0L	I/O33L	I/O29	I/O17L	I/O14L	I/O12L	I/O9L	I/O9R	I/O12R	I/O14R	I/O17R	I/O29R	I/O33R	A0R
C	NC	A1L	I/O31L	I/O27L	NC	I/O15L	I/O10L	I/O10R	I/O15R	NC	I/O27R	I/O31R	A1R	NC
D	A2L	A3L	I/O35L	I/O34L	I/O28L	I/O16L	VSS	VSS	I/O16R	I/O28R	I/O34R	I/O35R	A3R	A2R
E	A4L	A5L	NC	$\overline{B0L}$	NC	NC			NC	NC	BM	NC	A5R	A4R
F	VDD	A6L	A7L	$\overline{B1L}$	NC					NC	SIZE	A7R	A6R	VDD
G	$\overline{OEL}$	$\overline{B2L}$	$\overline{B3L}$	$\overline{CE0L}$							$\overline{CE0R}$	BA	WA	$\overline{OER}$
H	VSS	R/$\overline{W}$L	A8L	CE1L							CE1R	A8R	R/$\overline{W}$R	VSS
J	A9L	A10L	VSS	M/$\overline{S}$	NC					NC	VDD	VDD	A10R	A9R
K	A11L	A12L	NC	$\overline{SEML}$	NC	NC			NC	NC	$\overline{SEMR}$	NC	A12R	A11R
L	$\overline{BUSYL}$	A13L	$\overline{INTL}$	I/O26L	I/O25L	I/O19L	VSS	VSS	I/O19R	I/O25R	I/O26R	$\overline{INTR}$	A13R	$\overline{BUSYR}$
M	NC	NC[4]	I/O22L	I/O18L	NC	I/O7L	I/O2L	I/O2R	I/O7R	NC	I/O18R	I/O22R	NC[5]	NC
N	I/O24L	I/O20L	I/O8L	I/O6L	I/O5L	I/O3L	I/O0L	I/O0R	I/O3R	I/O5R	I/O6R	I/O8R	I/O20R	I/O24R
P	I/O23L	I/O21L	NC	VSS	I/O4L	VDD	I/O1L	I/O1R	VDD	I/O4R	VSS	NC	I/O21R	I/O23R

Pin Definitions

Left Port	Right Port	Description
A_{0L}–$A_{13/14L}$	A_{0R}–$A_{13/14R}$	Address (A_0–A_{13} for 16K; A_0–A_{14} for 32K devices)
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enable ($\overline{CE}$ is LOW when $\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy flag
I/O_{0L}–I/O_{35L}	I/O_{0R}–I/O_{35R}	Data bus input/output
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{B}_0$–$\overline{B}_3$		Byte select inputs. Asserting these signals enables read and write operations to the corresponding bytes of the memory array.
	BM, SIZE	See bus matching for details.
	WA, BA	See bus matching for details.
$M/\overline{S}$		Master or Slave select
V_{SS}		Ground
V_{DD}		Power

Architecture

The CY7C056V and CY7C057V consist of an array of 16K and 32K words of 36 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}_0$/CE_1, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two Interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two Semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the devices can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The devices also have an automatic power-down feature controlled by $\overline{CE}_0$/CE_1. Each port is provided with its own Output Enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Overview

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the R/$\overline{W}$ pin (see Write Cycle No. 1 waveform) or the $\overline{CE}_0$ and CE_1 pins (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in Table 1. If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Table 1. Non-Contending Read/Write [6]

Inputs					Outputs	Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{B_0}$, $\overline{B_1}$, $\overline{B_2}$, $\overline{B_3}$	$\overline{SEM}$	I/O_0–I/O_{35}	
H	X	X	X	H	High Z	Deselected: Power-down
X	X	X	All H	H	High Z	Deselected: Power-down
L	L	X	H/L	H	Data in and High Z	Write to selected bytes only
L	L	X	All L	H	Data in	Write to all bytes
L	H	L	H/L	H	Data out and High Z	Read selected bytes only
L	H	L	All L	H	Data out	Read all bytes
X	X	H	X	X	High Z	Outputs disabled
H	H	L	X	L	Data out	Read data in semaphore flag
X	H	L	All H	L	Data out	Read data in semaphore flag
H	⎍	X	X	L	Data in	Write D_{IN0} into semaphore flag
X	⎍	X	All H	L	Data in	Write D_{IN0} into semaphore flag
L	X	X	Any L	L		Not allowed

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$[6] pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$[6] pin, and $\overline{OE}$ must also be asserted.

Note
6. $\overline{CE}$ is LOW when $\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (3FFF for the CY7C056V, 7FFF for the CY7C057V) is the mailbox for the right port and the second-highest memory location (3FFE for the CY7C056V, 7FFE for the CY7C057V) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.The operation of the interrupts and their interaction with Busy are summarized in Table 2.

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = HIGH) [7, 8]

Function	Left Port					Right Port				
	$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L-13L/14L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R-13R/14R}$	$\overline{INT}_R$
Set right $\overline{INT}_R$ flag	L	L	X	3FFF (7FFF)	X	X	X	X	X	L[9]
Reset right $\overline{INT}_R$ flag	X	X	X	X	X	X	L	L	3FFF (7FFF)	H[10]
Set left $\overline{INT}_L$ flag	X	X	X	X	L[10]	L	L	X	3FFE (7FFE)	X
Reset left $\overline{INT}_L$ flag	X	L	L	3FFE (7FFE)	H[9]	X	X	X	X	X

Busy

The CY7C056V and CY7C057V provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' Chip Enables are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLC} or t_{BLA}), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Notes

7. $\overline{CE}$ is LOW when $\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$.
8. A_{0L-14L} and A_{0R-14R}, 7FFF/7FFE for the CY7C057V.
9. If $\overline{BUSY}_L$=L, then no change.
10. If $\overline{BUSY}_R$=L, then no change.

Semaphore Operation

The CY7C056V and CY7C057V provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available t_{SWRD} + t_{DOE} after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control of the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches. For normal semaphore access, $\overline{CE}$[11] must remain HIGH during $\overline{SEM}$ LOW. A $\overline{CE}$ active semaphore access is also available. The semaphore may be accessed through the right port with $\overline{CE}_{0R}$/CE_{1R} active by asserting the Bus Match Select (BM) pin LOW and asserting the Bus Size Select (SIZE) pin HIGH. The semaphore may be accessed through the left port with $\overline{CE}_{0L}$/CE_{1L} active by asserting all $\overline{B}_{0–3}$ Byte Select pins HIGH. $A_{0–2}$ represents the semaphore address. $\overline{OE}$ and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the port showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both ports. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. Table 3 shows sample semaphore operations.

Table 3. Semaphore Operation Example

Function	I/O_0–I/O_8 Left	I/O_0–I/O_8 Right	Status
No action	1	1	Semaphore free
Left port writes 0 to Semaphore	0	1	Left port has semaphore token
Right port writes 0 to Semaphore	0	1	No change. Right side has no write access to Semaphore
Left port writes 1 to Semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to Semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to Semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to Semaphore	1	1	Semaphore free
Right port writes 0 to Semaphore	1	0	Right port has semaphore token
Right port writes 1 to Semaphore	1	1	Semaphore free
Left port writes 0 to Semaphore	0	1	Left port has semaphore token
Left port writes 1 to Semaphore	1	1	Semaphore free

Note
11. $\overline{CE}$ is LOW when $\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$.

Table 4. Right Port Configuration [12, 13, 14]

BM	SIZE	Configuration	I/O Pins Used
0	0	× 36 (standard)	$I/O_{0–35}$
0	1	× 36 ($\overline{CE}$ active $\overline{SEM}$ mode)	$I/O_{0–35}$
1	0	× 18	$I/O_{0–17}$
1	1	× 9	$I/O_{0–8}$

Table 5. Right Port Operation

Configuration	WA	BA	Data Accessed [15]	I/O Pins Used
× 36	X	X	$DQ_{0–35}$	$I/O_{0–35}$
× 18	0	X	$DQ_{0–17}$	$I/O_{0–17}$
× 18	1	X	$DQ_{18–35}$	$I/O_{0–17}$
× 9	0	0	$DQ_{0–8}$	$I/O_{0–8}$
× 9	0	1	$DQ_{9–17}$	$I/O_{0–8}$
× 9	1	0	$DQ_{18–26}$	$I/O_{0–8}$
× 9	1	1	$DQ_{27–35}$	$I/O_{0–8}$

Table 6. Left Port Operation

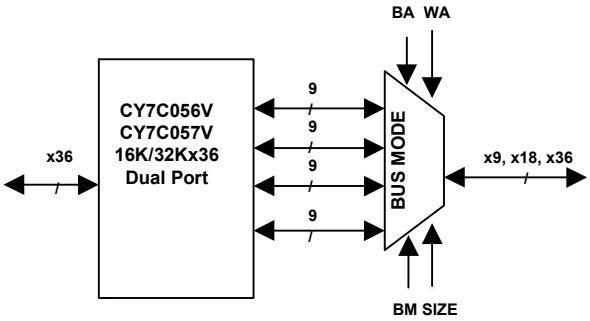
Control Pin	Effect
$\overline{B0}$	$I/O_{0–8}$ Byte control
$\overline{B1}$	$I/O_{9–17}$ Byte control
$\overline{B2}$	$I/O_{18–26}$ Byte control
$\overline{B3}$	$I/O_{27–35}$ Byte control

When reading a semaphore, data lines 0 through 8 output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Notes
12. BM and SIZE must be configured one clock cycle before operation is guaranteed.
13. In × 36 mode WA and BA pins are “Don’t Care.”
14. In × 18 mode BA pin is a “Don’t Care.”
15. DQ represents data output of the chip.

Bus Match Operation

The right port of the CY7C057V 32K × 36 dual-port SRAM can be configured in a 36-bit long-word, 18-bit word, or 9-bit byte format for data I/O. The data lines are divided into four lanes, each consisting of 9 bits (byte-size data lines).



The bus match select (BM) pin works with bus size select (SIZE) to select bus width (long-word, word, or byte) for the right port of the dual-port device. The data sequencing arrangement is selected using the word address (WA) and byte address (BA) input pins. A logic “0” applied to both the bus match select (BM) pin and to the bus size select (SIZE) pin will select long-word (36-bit) operation. A logic “1” level applied to the bus match select (BM) pin will enable either byte or word bus width operation on the right port I/Os depending on the logic level applied to the SIZE pin. The level of bus match select (BM) must be static throughout device operation.

Normally, the bus size select (SIZE) pin would have no standard-cycle application when BM = LOW and the device is in long-word (36-bit) operation. A “special” mode has been added however to disable ALL right port I/Os while the chip is active. This I/O disable mode is implemented when SIZE is forced to a logic “1” while BM is at a logic “0”. It allows the bus-matched port to support a chip enable “Don’t care” semaphore read/write access similar to that provided on the left port of the device when all Byte Select ($\overline{B}_{0-3}$) control inputs are deselected.

The bus size select (SIZE) pin selects either a byte or word data arrangement on the right port when the bus match select (BM) pin is HIGH. A logic “1” on the SIZE pin when the BM pin is HIGH selects a byte bus (9-bit) data arrangement). A logic “0” on the SIZE pin when the BM pin is HIGH selects a word bus (18-bit) data arrangement. The level of the bus size select (SIZE) must also be static throughout normal device operation.

Long-Word (36-bit) Operation

Bus match select (BM) and bus size select (SIZE) set to a logic “0” will enable standard cycle long-word (36-bit) operation. In this mode, the right port’s I/O operates essentially in an identical fashion as does the left port of the dual-port SRAM. However no byte select control is available. All 36 bits of the long-word are shifted into and out of the right port’s I/O buffer stages. All read and write timing parameters may be identical with respect to the two data ports. When the right port is configured for a long-word size, word address (WA), and byte Address (BA) pins have no application and their inputs are “Don’t Care” [16] for the external user.

Word (18-bit) Operation

Word (18-bit) bus sizing operation is enabled when bus match select (BM) is set to a logic “1” and the bus size select (SIZE) pin is set to a logic “0.” In this mode, 18 bits of data are ported through I/O_{0R-17R}. The level applied to the word address (WA) pin during word bus size operation determines whether the most-significant or least-significant data bits are ported through the I/O_{0R-17R} pins in an Upper word/Lower word select fashion (note that when the right port is configured for word size operation, the Byte Address pin has no application and its input is “Don’t care” [16]).

Device operation is accomplished by treating the WA pin as an additional address input and using standard cycle address and data setup/hold times. When transferring data in word (18-bit) bus match format, the unused $I/O_{18R-35R}$ pins are three-stated.

Byte (9-bit) Operation

Byte (9-bit) bus sizing operation is enabled when bus match select (BM) is set to a logic “1” and the bus size select (SIZE) pin is set to a logic “1.” In this mode, data is ported through I/O_{0R-8R} in four groups of 9-bit bytes. A particular 9-bit byte group is selected according to the levels applied to the word address (WA) and byte address (BA) input pins.

I/Os	Rank	WA	BA
$I/O_{27R-35R}$	Upper-MSB	1	1
$I/O_{18R-26R}$	Lower-MSB	1	0
I/O_{9R-17R}	Upper-MSB	0	1
I/O_{0R-8R}	Lower-MSB	0	0

Device operation is accomplished by treating the word address (WA) pin and the byte address (BA) pins as additional address inputs having standard cycle address and data set-up/hold times. When transferring data in byte (9-bit) bus match format, the unused I/O_{9R-35R} pins are three-stated.

Note
16. Even though a logic level applied to a “Don’t Care” input will not change the logical operation of the dual-port, inputs that are temporarily a “Don’t Care” (along with unused inputs) must not be allowed to float. They must be forced either HIGH or LOW.

Maximum Ratings

Exceeding maximum ratings[17] may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to +4.6 V

DC voltage applied to outputs in High Z state ..... –0.5 V to V_{DD}+0.5 V

DC input voltage ..... –0.5 V to V_{DD} + 0.5 V [18]

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0 °C to +70 °C	3.3 V ± 165 mV
Industrial	–40 °C to +85 °C	3.3 V ± 165 mV

Electrical Characteristics

Over the Operating Range

Parameter [19]	Description		CY7C056V CY7C057V						Unit
			-12			-15			
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH voltage (V_{DD} = Min., I_{OH} = –4.0 mA)		2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW voltage (V_{DD} = Min., I_{OL} = +4.0 mA)		–		0.4	–		0.4	V
V_{IH}	Input HIGH voltage		2.0		–	2.0		–	V
V_{IL}	Input LOW voltage		–		0.8	–		0.8	V
I_{OZ}	Output leakage current		–10		10	–10		10	µA
I_{CC}	Operating current (V_{DD} = Max., I_{OUT} = 0 mA), output disabled	Commercial	–	250	385	–	240	360	mA
		Industrial		–			265	385	mA
I_{SB1}	Standby current (Both ports TTL level and deselected), f = f_{MAX}	Commercial		55	75		50	70	mA
		Industrial		–			65	95	mA
I_{SB2}	Standby current (One port TTL level and deselected), f = f_{MAX}	Commercial		180	240		175	230	mA
		Industrial		–			190	255	mA
I_{SB3}	Standby current (Both ports CMOS level and deselected), f =0	Commercial		0.01	1		0.01	1	mA
		Industrial		–			0.01	1	mA
I_{SB4}	Standby current (One Port CMOS level and deselected), f = f_{MAX}[20]	Commercial		160	210		155	200	mA
		Industrial		–			170	215	mA

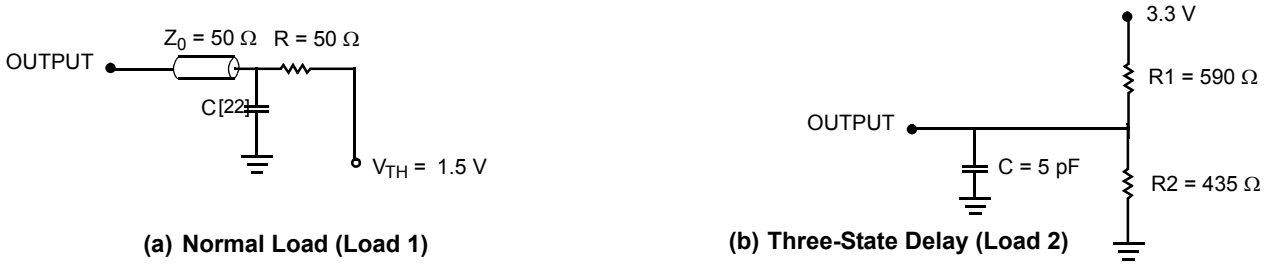
Notes
17. The voltage on any input or I/O pin can not exceed the power pin during power-up.
18. Pulse width < 20 ns.
19. Deselection for a port occurs if $\overline{CE}_0$ is HIGH or if CE_1 is LOW.
20. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except Output Enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance

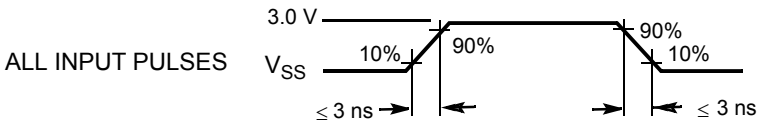
Parameter [21]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V	10	pF
C_{OUT}	Output capacitance		10	pF

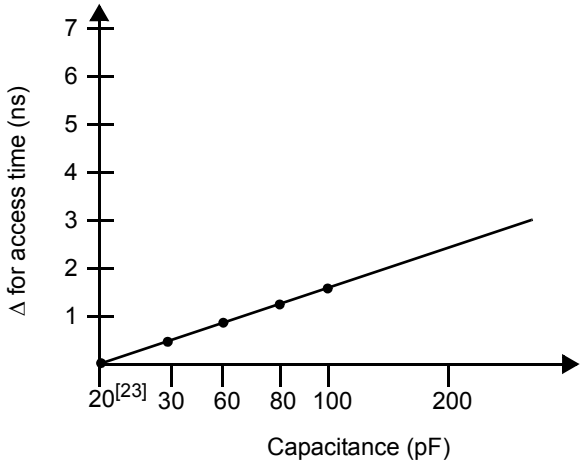
AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



(a) Normal Load (Load 1) **(b) Three-State Delay (Load 2)**





(b) Load Derating Curve

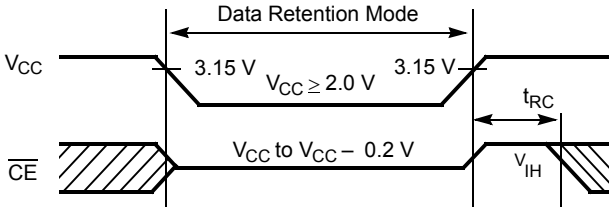
Notes
21. Tested initially and after any design or process changes that may affect these parameters.
22. External AC Test Load Capacitance = 10 pF.
23. (Internal I/O pad Capacitance = 10 pF) + AC Test Load.

Data Retention Mode

The CY7C056V and CY7C057V are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{CE}$)[24] must be held HIGH during data retention, within V_{DD} to V_{DD} – 0.2 V.
2. $\overline{CE}$ must be kept between V_{DD} – 0.2 V and 70% of V_{DD} during the power-up and power-down transitions.
3. The RAM can begin operation > t_{RC} after V_{DD} reaches the minimum operating voltage (3.15 volts).

Timing



Parameter	Test Conditions[25]	Max	Unit
ICC_{DR1}	@ VDD_{DR} = 2 V	50	µA

Notes
24. $\overline{CE}$ is LOW when $\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$.
25. $\overline{CE}$ = V_{DD}, V_{in} = V_{SS} to V_{DD}, T_A = 25 °C. This parameter is guaranteed but not tested.

Switching Characteristics

Over the Operating Range

Parameter [26]	Description	CY7C056V CY7C057V				Unit
		-12		-15		
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	12	–	15	–	ns
t_{AA}	Address to data valid	–	12	–	15	ns
t_{OHA}	Output hold from address change	3	–	3	–	ns
t_{ACE}[27, 28]	$\overline{CE}$ LOW to data valid	–	12	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	8	–	10	ns
t_{LZOE}[27, 29, 30, 31]	$\overline{OE}$ Low to low Z	0	–	0	–	ns
t_{HZOE}[27, 29, 30, 31]	$\overline{OE}$ HIGH to High Z	–	10	–	10	ns
t_{LZCE}[27, 26, 30, 31]	$\overline{CE}$ LOW to Low Z	3	–	3	–	ns
t_{HZCE}[27, 29, 30, 31]	$\overline{CE}$ HIGH to High Z	–	10	–	10	ns
t_{LZBE}	Byte Enable to Low Z	3	–	3	–	ns
t_{HZBE}	Byte Enable to High Z	–	10	–	10	ns
t_{PU}[27, 31]	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t_{PD}[27, 31]	$\overline{CE}$ HIGH to power-down	–	12	–	15	ns
t_{ABE}[28]	Byte Enable access time	–	12	–	15	ns
Write Cycle						
t_{WC}	Write cycle time	12	–	15	–	ns
t_{SCE}[27, 28]	$\overline{CE}$ LOW to write end	10	–	12	–	ns
t_{AW}	Address valid to write end	10	–	12	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}[28]	Address set-up to write start	0	–	0	–	ns
t_{PWE}	Write pulse width	10	–	12	–	ns
t_{SD}	Data set-up to write end	10	–	10	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}[30, 31]	R/$\overline{W}$ LOW to High Z	–	10	–	–	ns
t_{LZWE}[30, 31]	R/$\overline{W}$ HIGH to Low Z	3	–	3	–	ns
t_{WDD}[32]	Write pulse to data delay	–	25	–	–	ns
t_{DDD}[32]	Write data valid to read data valid	–	20	–	25	ns

Notes

26. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OI}/I_{OH} and 10-pF load capacitance.
27. $\overline{CE}$ is LOW when $\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$.
28. To access RAM, $\overline{CE}$ = L and $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{SCE} time.
29. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
30. Test conditions used are Load 2.
31. This parameter is guaranteed by design, but it is not production tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
32. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.

Switching Characteristics (continued)

Over the Operating Range

Parameter [26]	Description	CY7C056V CY7C057V				Unit
		-12		-15		
		Min	Max	Min	Max	
Busy Timing [33]						
t_{BLA}	$\overline{BUSY}$ LOW from address match	–	12	–	15	ns
t_{BHA}	$\overline{BUSY}$ HIGH from address mismatch	–	12	–	15	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	12	–	15	ns
Busy Timing [33]						
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH	–	12	–	15	ns
t_{PS}	Port set-up for priority	5	–	5	–	ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ (Slave)	0	–	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	11	–	13	–	ns
t_{BDD} [34]	$\overline{BUSY}$ HIGH to data valid	–	12	–	15	ns
Interrupt Timing [33]						
t_{INS}	$\overline{INT}$ set time	–	12	–	15	ns
t_{INR}	$\overline{INT}$ reset time	–	12	–	15	ns
Semaphore Timing						
t_{SOP}	SEM flag update pulse ($\overline{OE}$ or $\overline{SEM}$)	10	–	10	–	ns
t_{SWRD}	SEM flag write to read time	5	–	5	–	ns
t_{SPS}	SEM flag contention window	5	–	5	–	ns
t_{SAA}	SEM address access time	–	12	–	15	ns

Notes
33. Test conditions used are Load 1.
34. t_{BDD} is a calculated parameter and is the greater of t_{WDD}–t_{PWE} (actual) or t_{DDD}–t_{SD} (actual).

Switching Waveforms

Figure 4. Read Cycle No. 1 (Either Port Address Access) [35, 36, 37]

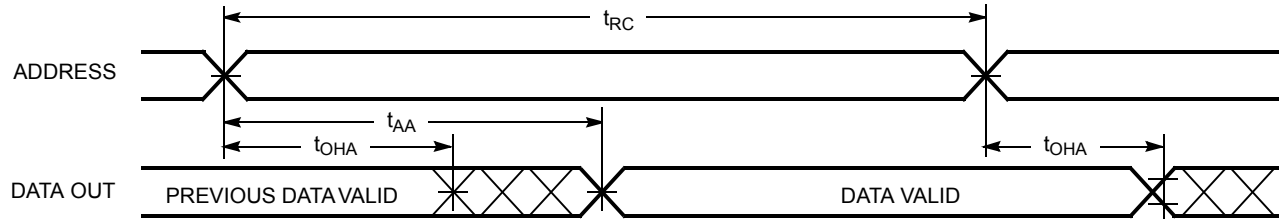


Figure 5. Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access) [35, 38, 39]

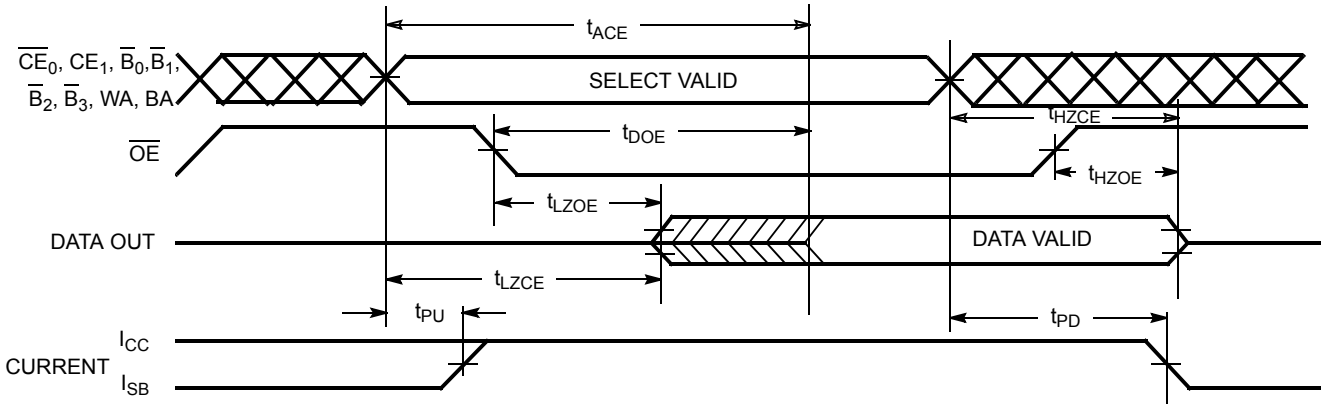
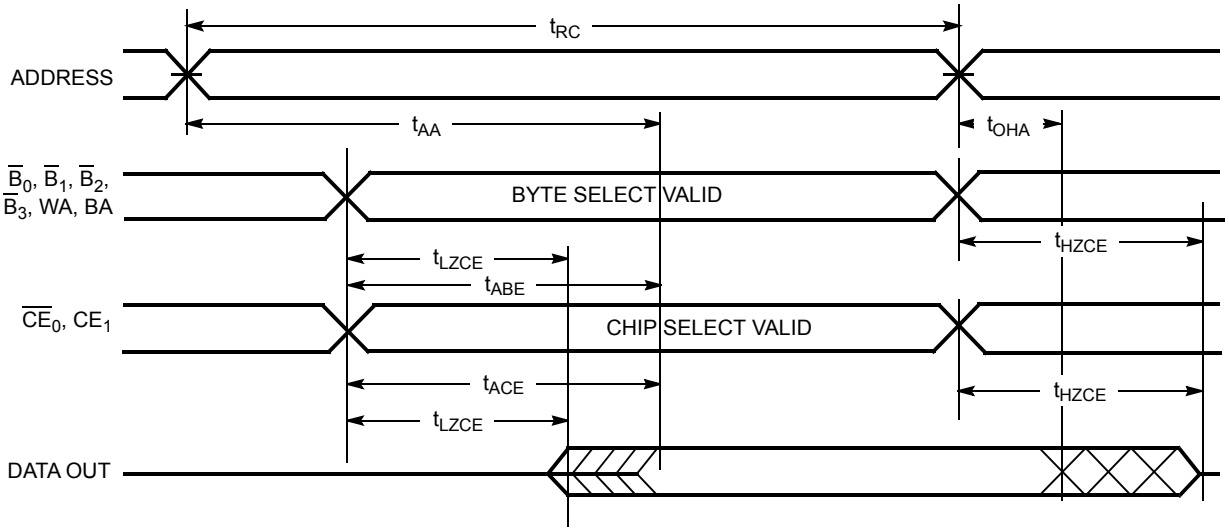


Figure 6. Read Cycle No. 3 (Either Port) [35, 37, 38, 39]



Notes

35. R/$\overline{W}$ is HIGH for read cycles.
36. Device is continuously selected. $\overline{CE}_0 = V_{IL}$, $CE_1 = V_{IH}$, and $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$, WA, BA are valid. This waveform cannot be used for semaphore reads.
37. $\overline{OE} = V_{IL}$.
38. Address valid prior to or coinciding with $\overline{CE}_0$ transition LOW and CE_1 transition HIGH.
39. To access RAM, $\overline{CE}_0 = V_{IL}$, $CE_1 = V_{IH}$, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$, WA, BA are valid, and $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE}_0 = V_{IH}$, $CE_1 = V_{IL}$ and $\overline{SEM} = V_{IL}$ or $\overline{CE}_0$ and $\overline{SEM} = V_{IL}$, and $CE_1 = \overline{B}_0 = \overline{B}_1 = \overline{B}_2 = \overline{B}_3, = V_{IH}$.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (R/$\overline{W}$ Controlled Timing) [40, 41, 42, 43]

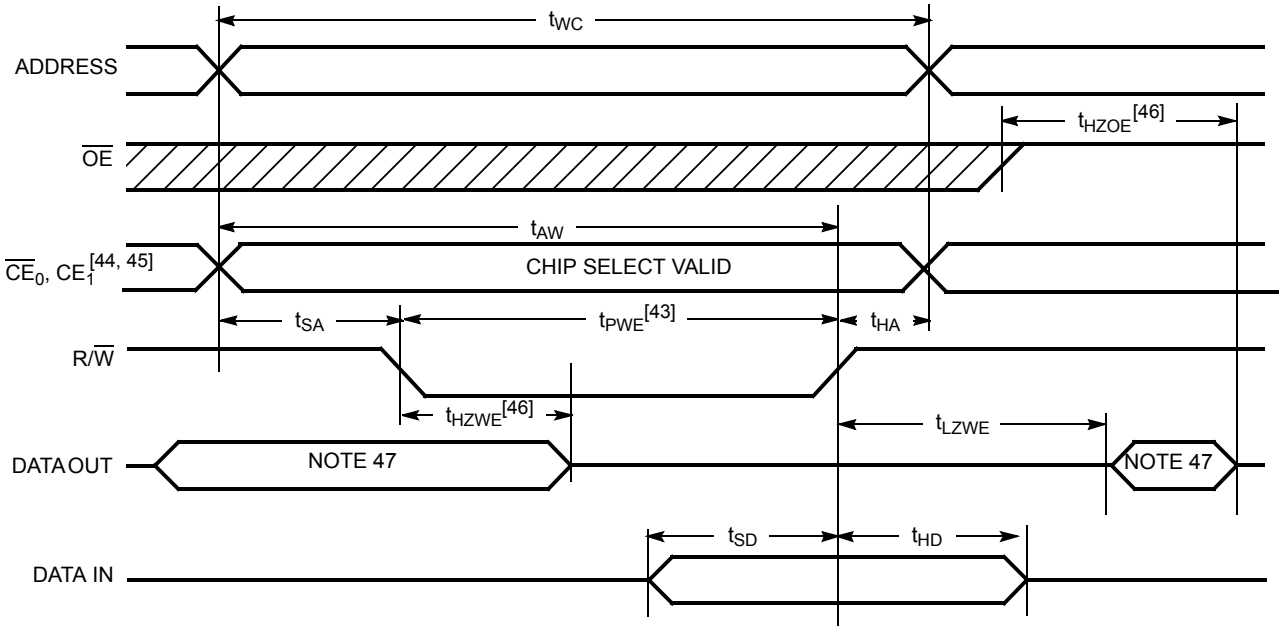
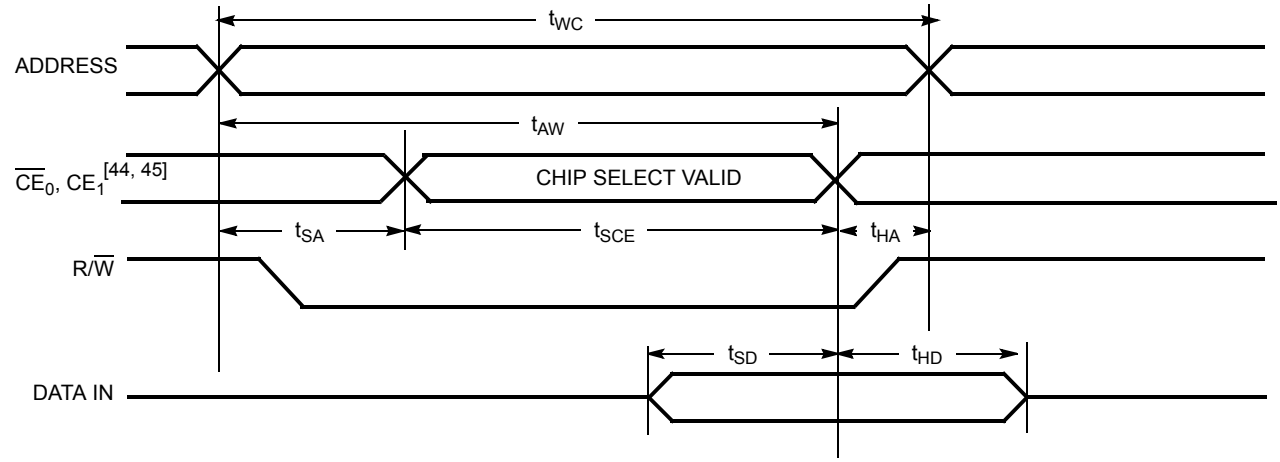


Figure 8. Write Cycle No. 2 ($\overline{CE}$ Controlled Timing) [40, 41, 42, 48]



Notes

40. R/$\overline{W}$ must be HIGH during all address transitions.
41. A write occurs during the overlap (t_{SCE} or t_{PWE}) of $\overline{CE}_0$=V_{IL} and CE_1=V_{IH} or $\overline{SEM}$=V_{IL} and $\overline{B}_{0-3}$ LOW.
42. t_{HA} is measured from the earlier of $\overline{CE}_0$/CE_1 or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of Write Cycle.
43. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
44. To access RAM, $\overline{CE}_0$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
45. To access byte $\overline{B}_0$, $\overline{CE}_0$ = V_{IL}, $\overline{B}_0$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
    To access byte $\overline{B}_1$, $\overline{CE}_0$ = V_{IL}, $\overline{B}_1$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
    To access byte $\overline{B}_2$, $\overline{CE}_0$ = V_{IL}, $\overline{B}_2$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
    To access byte $\overline{B}_3$, $\overline{CE}_0$ = V_{IL}, $\overline{B}_3$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
46. Transition is measured ±150 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
47. During this period, the I/O pins are in the output state, and input signals must not be applied.
48. If the $\overline{CE}_0$ LOW and CE_1 HIGH or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms (continued)

Figure 9. Semaphore Read After Write Timing, Either Side [49]

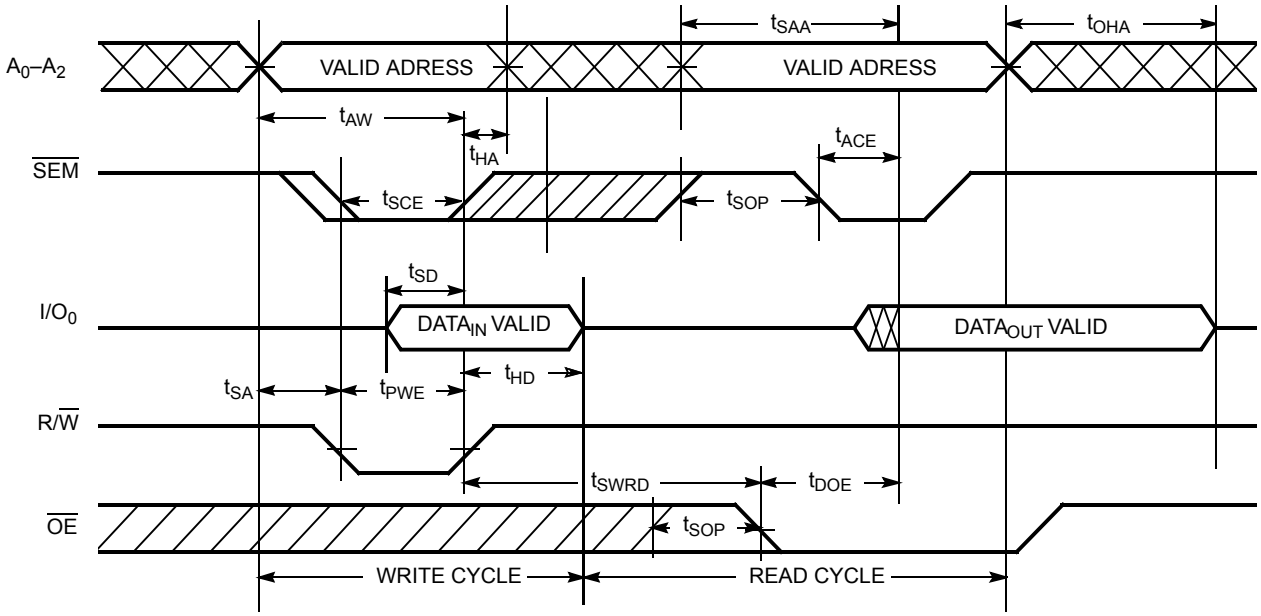
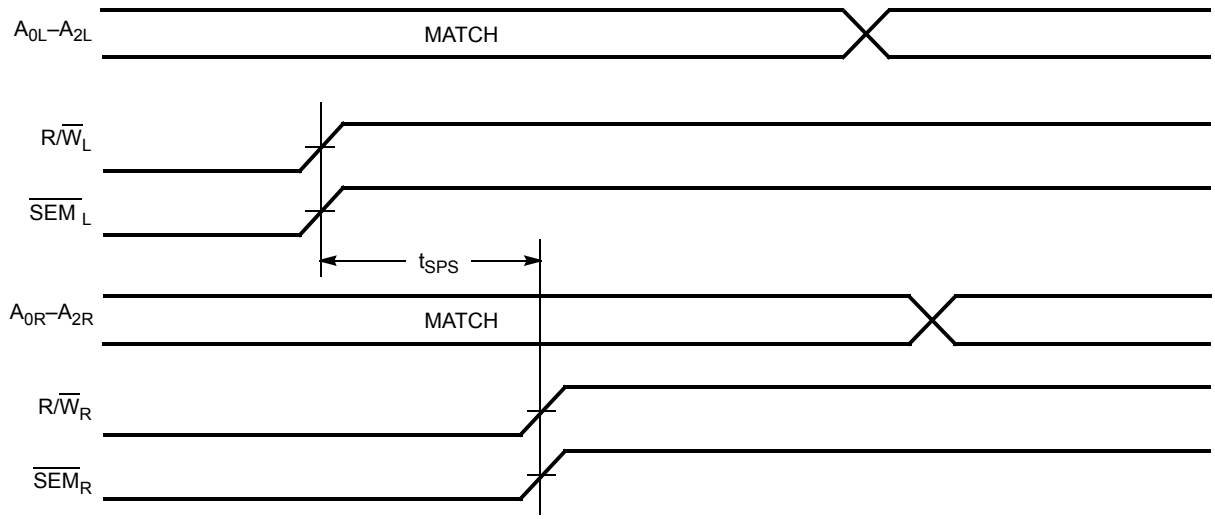


Figure 10. Timing Diagram of Semaphore Contention [50, 51, 52]



Notes
49. $\overline{CE}_0$ = HIGH and CE_1 = LOW for the duration of the above timing (both write and read cycle).
50. I/O_{0R} = I/O_{0L} = LOW (request semaphore); $\overline{CE}_{0R}$ = $\overline{CE}_{0L}$ = HIGH and CE_{1R} = CE_{1L} = LOW.
51. Semaphores are reset (available to both ports) at cycle start.
52. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms (continued)

Figure 11. Timing Diagram of Write with $\overline{BUSY}$ (M/$\overline{S}$ = HIGH) [53]

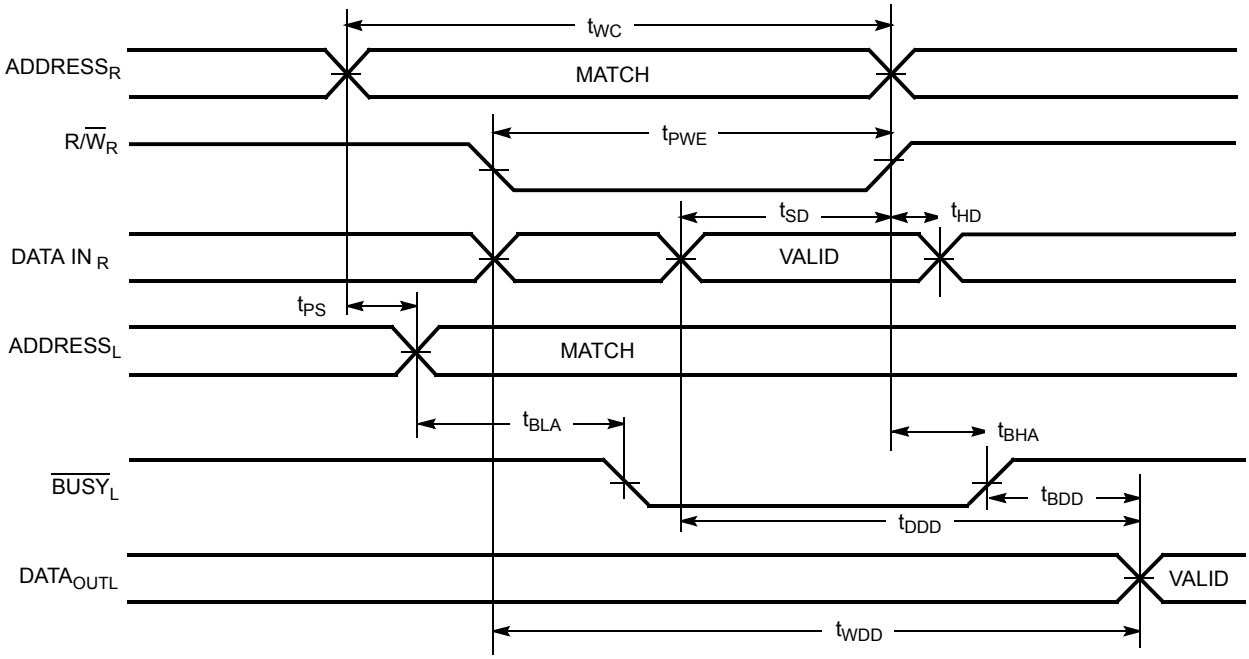
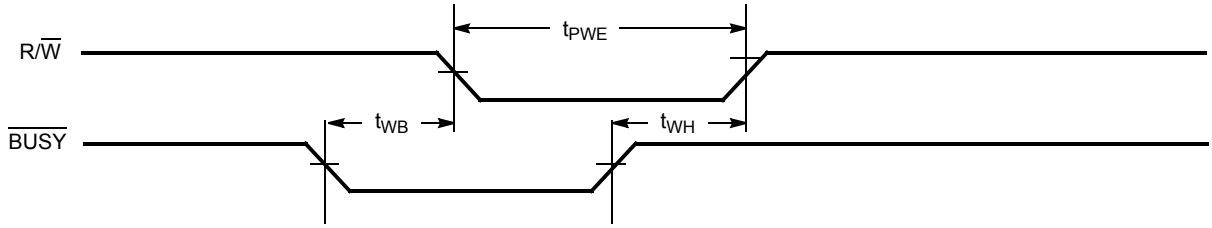


Figure 12. Write Timing with Busy Input (M/$\overline{S}$ = LOW)



Note
53. $\overline{CE}_{0L}$ = $\overline{CE}_{0R}$ = LOW; CE_{1L} = CE_{1R} = HIGH.

Switching Waveforms (continued)

Figure 13. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration) [54]

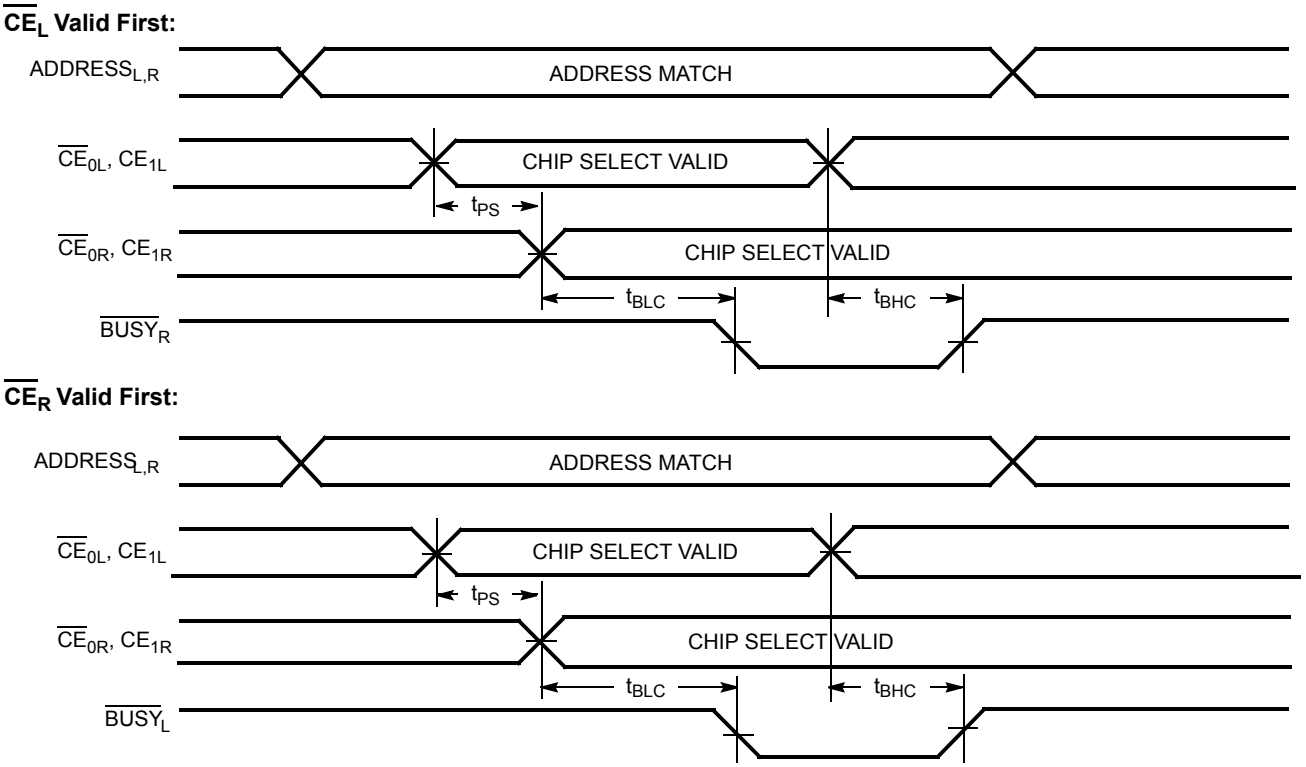
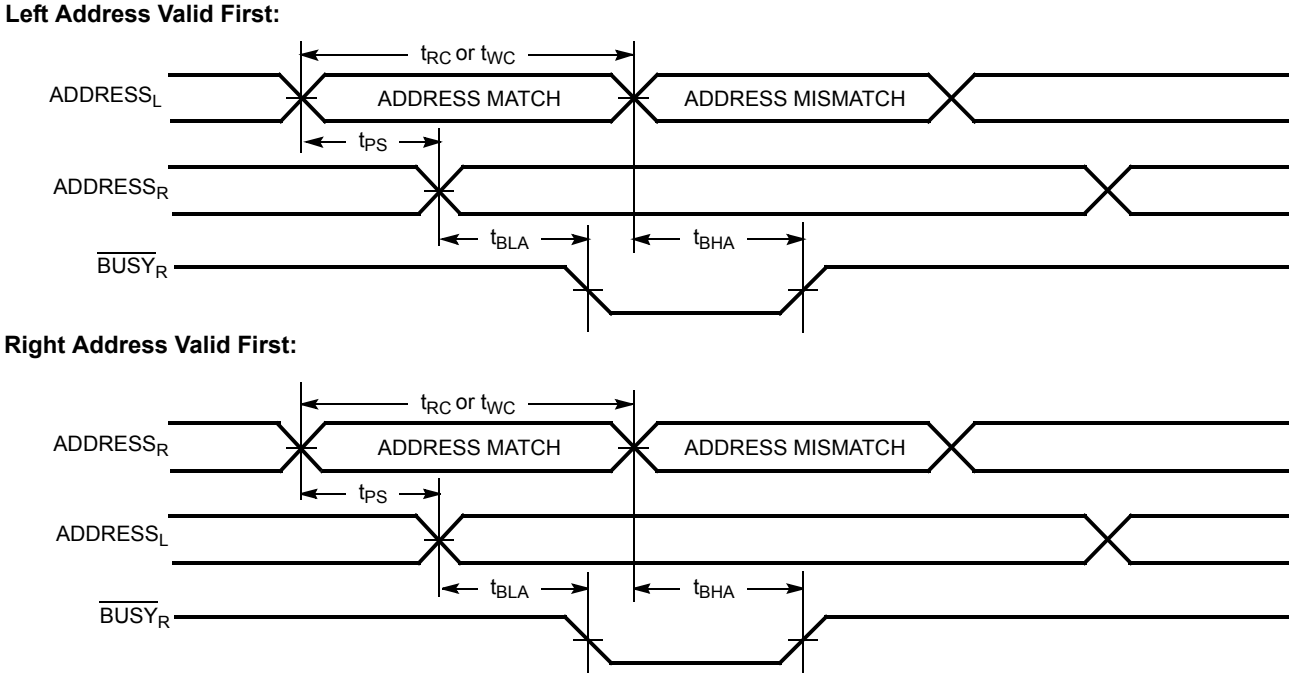


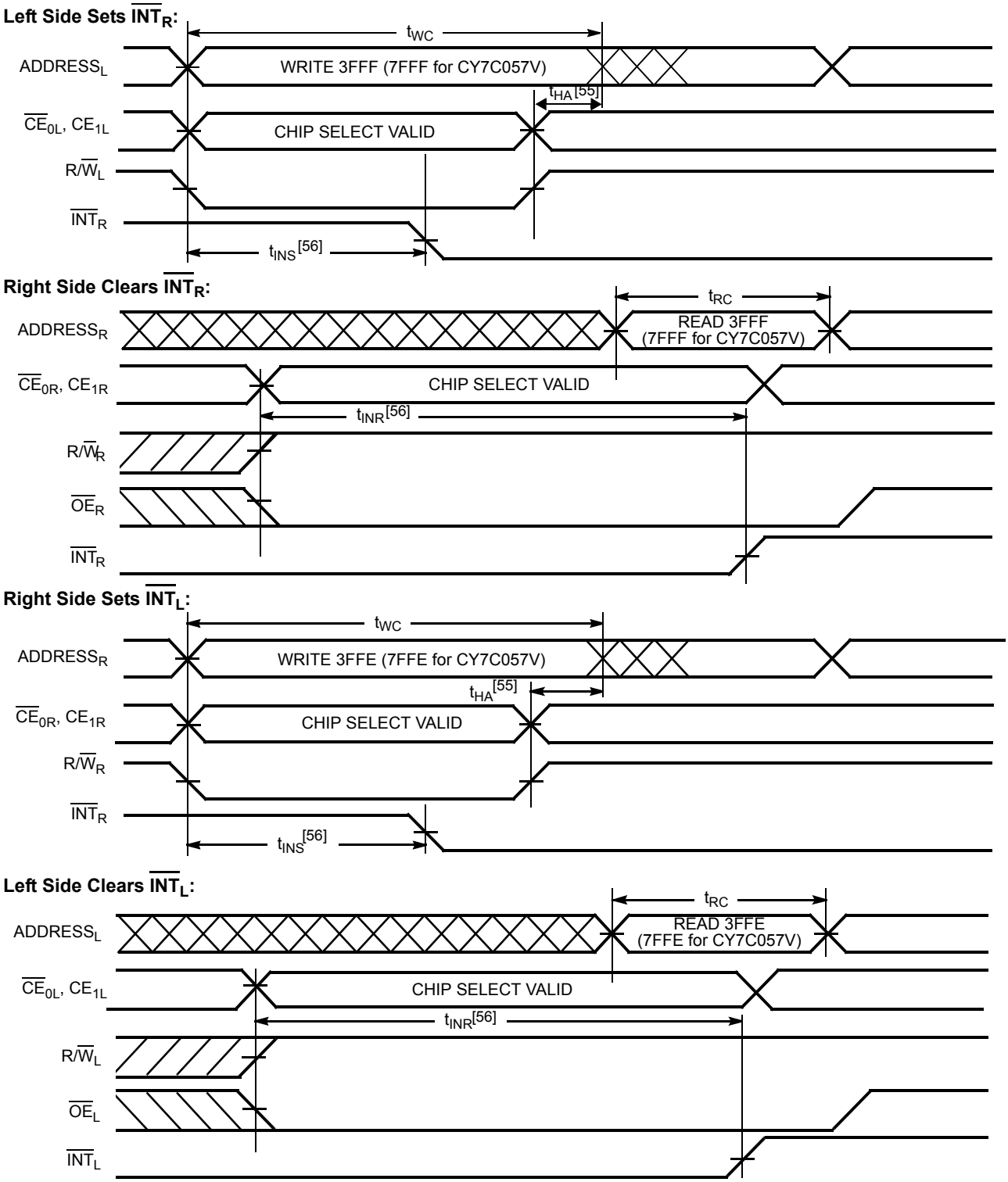
Figure 14. Busy Timing Diagram No. 2 (Address Arbitration) [54]



Note
54. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

Switching Waveforms (continued)

Figure 15. Interrupt Timing Diagrams



Notes

55. t_{HA} depends on which enable pin ($\overline{CE}_{0L}$/CE_{1L} or R/$\overline{W}_L$) is deasserted first.
56. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_{0L}$/CE_{1L} or R/$\overline{W}_L$) is asserted last.

Ordering Information

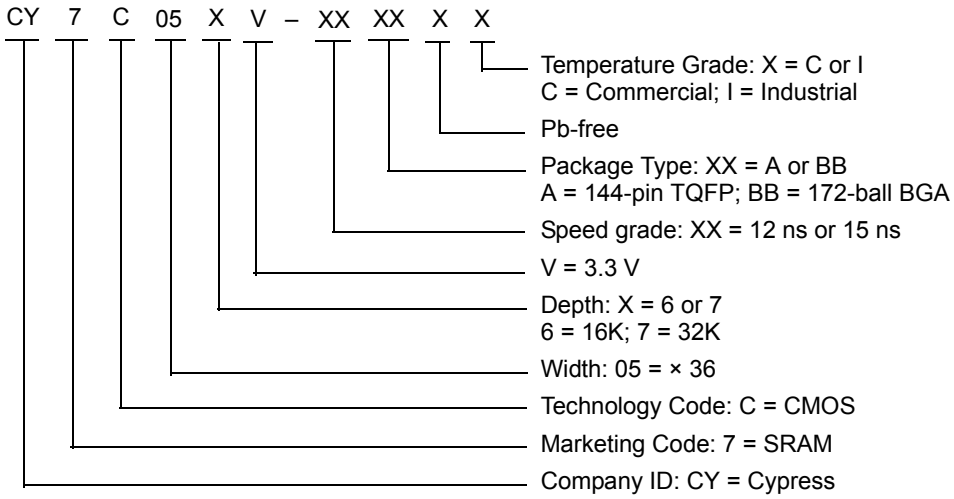
16K × 36 3.3 V Asynchronous Dual Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C056V-15AXC	A144	144-pin TQFP (Pb-free)	Commercial

32K × 36 3.3 V Asynchronous Dual Port SRAM

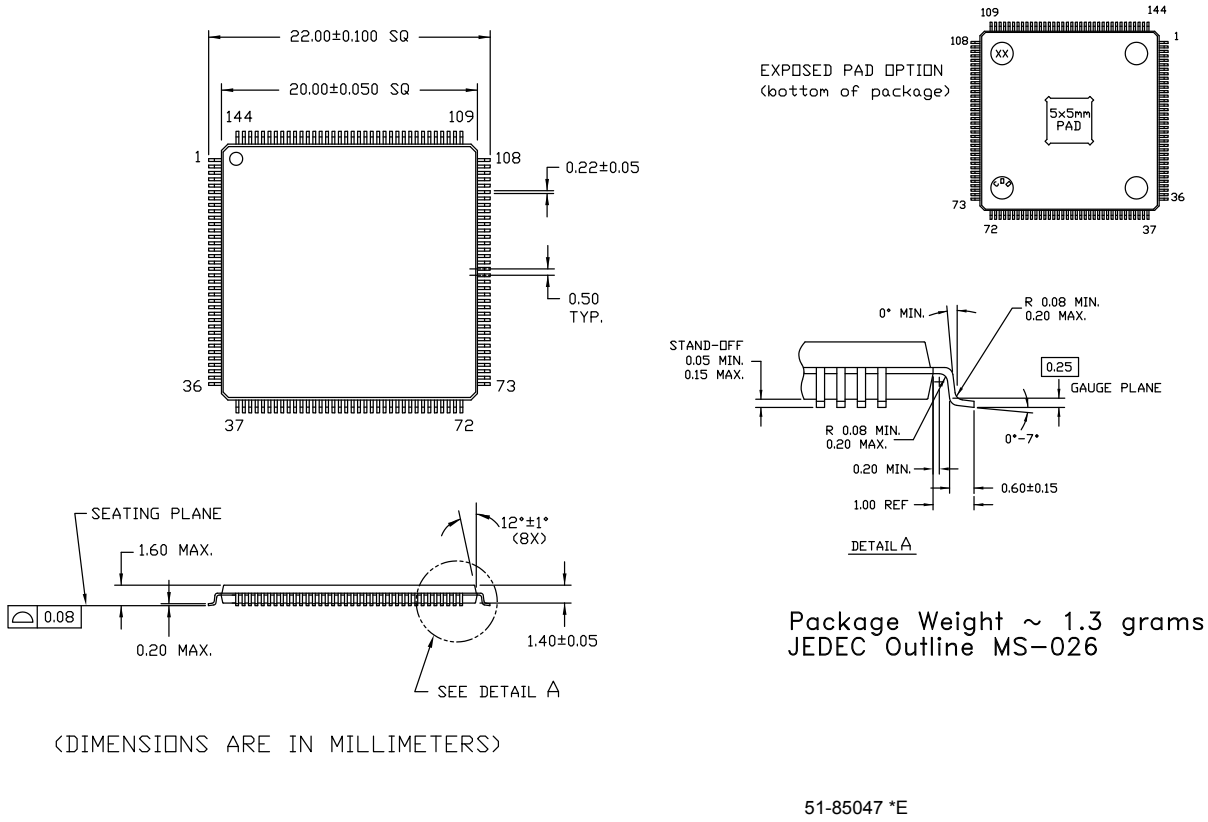
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C057V-12AXC	A144	144-pin TQFP (Pb-free)	Commercial
15	CY7C057V-15AXC	A144	144-pin TQFP (Pb-free)	Commercial
	CY7C057V-15AXI	A144	144-pin TQFP (Pb-free)	Industrial
	CY7C057V-15BBI	BB172	172-ball BGA	Industrial
	CY7C057V-15BBXC	BB172	172-ball BGA	Commercial

Ordering Code Definitions



Package Diagrams

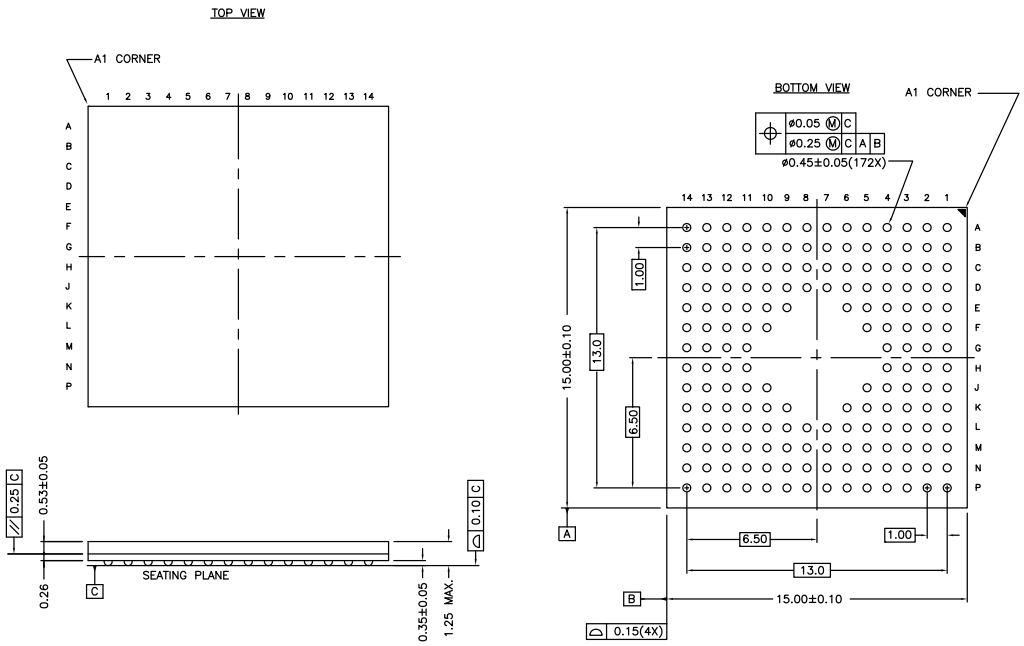
Figure 16. 144-pin TQFP (20 × 20 × 1.4 mm) A144SA Package Outline, 51-85047



51-85047 *E

Package Diagrams (continued)

Figure 17. 172-ball FBGA (15 × 15 × 1.25 mm) BB172 Package Outline, 51-85114



Package Weight – Refer to PMDD spec.

51-85114 *E

Acronyms

Acronym	Description
BGA	Ball Grid Array
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{INT}$	Interrupt
$\overline{OE}$	Output Enable
R/$\overline{W}$	Read or Write Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Errata

This section describes the errata for the 32K/16K × 36 Asynchronous Dual-Port Static RAM – CY7C057V / CY7C056V. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

If you have questions, contact your local Cypress Sales Representative or raise a technical support case at www.cypress.com/go/support.

Part Numbers Affected

Part Number	Device Characteristics
CY7C057V/CY7C056V (all packages and options)	32K/16K × 36 Asynchronous Dual-Port Static RAM

Qualification Status

Product Status: This device is currently in production.

Errata Summary

This table defines the errata applicability to the devices.

Items	Part Numbers	Minimum value	Maximum Value	Fix Status
VDD conditions during Brown-out	CY7C057V / CY7C056V	V_{DD} drops to less than 1.5 V during a Brown-out	–	None planned

1. V_{DD} conditions during Brown-out

■ **Problem Definition**

In the event of a brown-out, if the supply voltage (V_{DD}) drops to a value less than 1.5 V, there is a possibility that the internal POR (power-on-reset) circuit could malfunction, resulting in functional failures after power-up again.

■ **Parameters Affected**

Device functionality would be affected on following power-up cycles. Hence, all parameters would be affected.

■ **Trigger Condition**

If the supply voltage (V_{DD}) drops to a value less than 1.5 V, there is a possibility that the internal POR (power-on-reset) circuit could malfunction, resulting in functional failures after power-up again.

■ **Scope of Impact**

This issue could affect end systems where there are brown-out events.

■ **Workaround**

It is recommended that customers take adequate measures to avoid supply voltage (V_{DD}) dropping below 1.5 V.

If the above workaround is not possible, we recommend performing a forced power cycle, for a period greater than 500 ms.

■ **Fix Status**

Fix is none planned for this issue. It is recommended to implement the Workaround mentioned above.

Document History Page

Document Title: CY7C056V/CY7C057V, 3.3 V 16K/32K × 36 FLEx36™ Asynchronous Dual-Port Static RAM Document Number: 38-06055				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110214	12/16/01	SZV	Change from Spec number: 38-00742 to 38-06055
*A	122305	12/27/02	RBI	Updated Maximum Ratings: Added Note 17 and referred the same note in maximum ratings.
*B	393770	See ECN	YIM	Added Pb-Free Logo. Updated Ordering Information (Added Pb-Free parts to ordering information namely CY7C056V-12AXC, CY7C056V-15AXC, CY7C057V-12AXC, CY7C057V-15AXC, CY7CO57V-15AXI).
*C	2897217	03/22/2010	RAME	Updated Ordering Information. Updated Package Diagrams.
*D	3093365	11/25/2010	ADMU	Updated Ordering Information (Removed part CY7C057V-15BBC, added part CY7C057V-15AXI) and added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated all footnotes. Updated to new template.
*E	3210221	03/30/2011	ADMU	Updated Ordering Information (Removed parts CY7C056V-15AC and CY7C057V-12BBC).
*F	3403652	10/14/2011	ADMU	Updated Ordering Information (Removed part CY7C057V-12AC). Updated Package Diagrams.
*G	3828475	12/03/2012	SMCH	Updated Functional Overview: Updated Interrupts: Updated Table 2. Updated Semaphore Operation: Updated description. Updated Package Diagrams: spec 51-85114 – Changed revision from *D to *E.
*H	4613785	01/05/2015	AJU	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated to new template.
*I	4632386	01/20/2015	AJU	Updated Package Diagrams: spec 51-85047 – Changed revision from *D to *E. Added Errata.
*J	5018928	11/18/2015	NILE	Updated to new template. Completing Sunset Review.
*K	5446521	09/27/2016	VINI	Updated Errata: Updated Errata Summary: Updated details in “Fix Status” column in the table. Updated details in “Fix Status” bulleted item. Updated to new template. Completing Sunset Review.
*L	5977230	11/27/2017	AESATMP8	Updated logo and Copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support