2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		,
2	gate		لِي
3	source	[1]	2 — — 3
			sym039

^[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package			
	Name	Description	Version	
BLA0912-250R	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A	

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	75	V
V_{GS}	gate-source voltage		-	±22	V
P _{tot}	total power dissipation	$T_h \leq 25$ °C; t_p = 50 $\mu s; \delta$ = 2 %	-	700	W
T _{stg}	storage temperature		-65	+150	°C
T _i	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$Z_{\text{th(j-h)}}$	transient thermal impedance from junction to heatsink	T _h = 25 °C	<u>11</u> 0.18	K/W

^[1] Thermal resistance is determined under RF operating conditions; t_p = 100 μ s, δ = 10 %.

6. Characteristics

Table 6. DC characteristics

 $T_i = 25$ °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 3 \text{ mA}$	75	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_{D} = 300 mA	4	-	5	V
I _{DSS}	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 36 \text{ V}$	-	-	1	μА
I _{DSX}	drain cut-off current	$V_{GS} = V_{GSth} + 9 V;$ $V_{DS} = 10 V$	45	-	-	Α
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V	-	-	1	μА
g _{fs}	forward transconductance	V_{DS} = 10 V; I_{D} = 10 A	-	9	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 9 \text{ V}; I_D = 10 \text{ A}$	-	60	-	$m\Omega$

Table 7. RF characteristics

RF performance in common source class-AB circuit; $T_h = 25$ °C; $Z_{th} = 0.15$ K/W; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage		-	-	36	V
f	frequency		960	-	1215	MHz
P_{L}	output power	t_p = 100 μ s; δ = 10 %	250	-		W
Gp	power gain	P _L = 250 W	12	13		dB
η_{D}	drain efficiency	t_p = 100 μ s; δ = 10 %	40	50		%
$Z_{th(j-h)}$	transient thermal impedance from junction to heatsink	t_p = 100 μ s; δ = 10 %	-	-	0.2	K/W
T _h	heatsink temperature		-55	-	+70	°C
P _{droop(pulse)}	pulse droop power	t_p = 100 μ s; δ = 10 %	-	0.1	0.5	dB
$\alpha_{resp(sp)}$	spurious response	VSWR _{load} = 2 : 1	-	-	-60	dBc
t _r	rise time		-	25	50	ns
t _f	fall time		-	6	25	ns

6.1 Ruggedness in class-AB operation

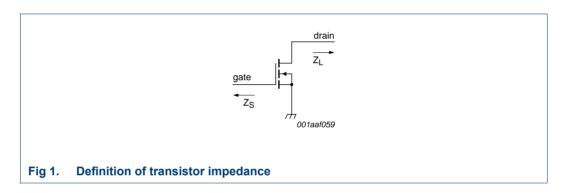
The BLA0912-250R is capable of withstanding a load mismatch corresponding to VSWR = 5:1 through all phases under the following conditions: $V_{DS} = 36 \text{ V}$; f = 960 MHz to 1215 MHz at rated load power.

7. Application information

7.1 Impedance information

Table 8. Typical impedance *Typical values per section unless otherwise specified.*

f	Z _S	Z _L
MHz	Ω	Ω
960	0.89 - j1.70	1.53 – j1.13
1030	1.37 – j1.23	1.47 – j0.99
1090	2.09 – j1.27	1.38 – j0.85
1140	2.40 - j1.97	1.30 – j0.71
1215	1.51 – j2.61	1.17 – j0.47



7.2 Application circuit

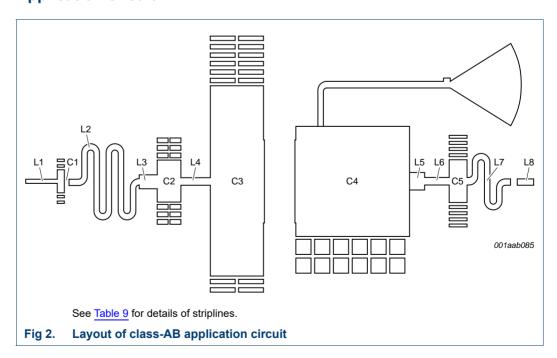


Table 9. Layout details

See Figure 2.

Striplines are on a Rodgers Duroid 6010 Printed-Circuit Board (PCB); $\varepsilon_r = 10.2$ F/m; thickness = 0.64 mm

Component	Description	Dimensions	
Input circuit			
L1	stripline	$5 \text{ mm} \times 0.8 \text{ mm}$	
C1	stripline	$1.2 \text{ mm} \times 3.5 \text{ mm}$	
L2	stripline	capacitor pad: 1 mm \times 1 mm (1 \times)	
		curve: width 0.8 mm; angle 90°; radius 0.8 mm (10×)	
		vertical: $3.9 \text{ mm} \times 0.8 \text{ mm} (2\times)$	
		vertical: 9.4 mm \times 0.8 mm (3 \times)	
		horizontal: $0.5 \text{ mm} \times 0.8 \text{ mm } (4\times)$	
L3	stripline	3 mm × 2 mm	
C2	stripline	4 mm × 6.5 mm	
L4	stripline	5 mm × 1 mm	
C3	stripline	8.8 mm × 30 mm + 0.2 mm × 13 mm	
Output circui	t		
C4	stripline	0.2 mm × 13 mm + 19 mm × 17.1 mm	
L5	stripline	$2.5~\text{mm} \times 2.3~\text{mm}$	
L6	stripline	4 mm × 1 mm	
C5	stripline	3 mm × 6.6 mm	
L7	stripline	curve: width 0.8 mm; angle 90°; radius 0.8 mm (6×)	
		vertical: 2.2 mm \times 0.8 mm (2 \times)	
		vertical: 6 mm \times 0.8 mm (1 \times)	
		horizontal: 1 mm \times 0.8 mm (2 \times)	
L8	stripline	2.5 mm × 0.8 mm	
1/4 λ line	stripline	curve: width 1 mm; angle 90°; radius 0.8 mm	
		vertical: 5 mm × 1 mm	
		horizontal: 19 mm × 1 mm	

Product data sheet

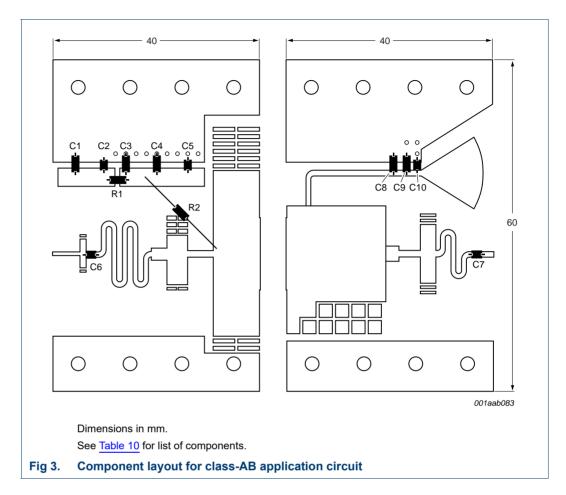


Table 10. List of components See Figure 3.

Component	Description	Value		Remarks
C1, C3, C9	multilayer ceramic chip capacitor	1 nF	[1]	
C2, C6, C10	multilayer ceramic chip capacitor	22 pF	[2]	
C4	tantalum SMD capacitor	47 μF; 20 V		KEMET: T491D476M020AS
C5	multilayer ceramic chip capacitor	56 pF	[2]	
C7	multilayer ceramic chip capacitor	47 pF	[2]	
C8	tantalum SMD capacitor	22 μF; 63 V		
R1	SMD resistor	51 Ω		0805
R2	resistor	49.9 Ω		

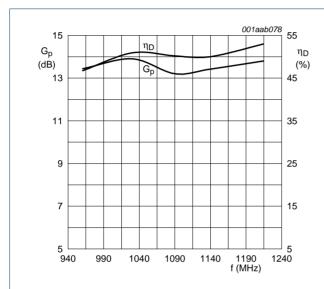
^[1] American Technical Ceramics type 100B or capacitor of same quality.

^[2] American Technical Ceramics type 100A or capacitor of same quality.

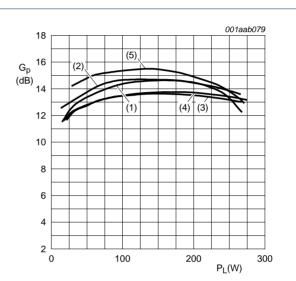
8. Test information

8.1 RF performance

Typical RF performance measured in common source class-AB test circuit at P_L = 250 W and 960 MHz to 1215 MHz frequency band. T_h = 25 °C; $Z_{th(j-h)}$ = 0.15 K/W; unless otherwise specified.



 T_h = 25 °C; V_{DS} = 36 V; I_{Dq} = 150 mA; class-AB; t_p = 100 μ s; δ = 10 %.

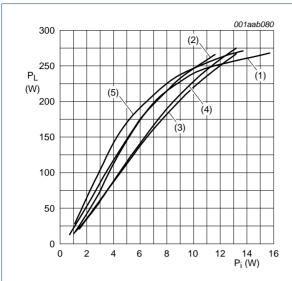


 T_h = 25 °C; V_{DS} = 36 V; I_{Dq} = 150 mA; class-AB; t_p = 100 μ s; δ = 10 %.

- (1) f = 960 MHz
- (2) f = 1030 MHz
- (3) f = 1090 MHz
- (4) f = 1140 MHz
- (5) f = 1215 MHz

Fig 4. Power gain and drain efficiency as function of frequency; typical values

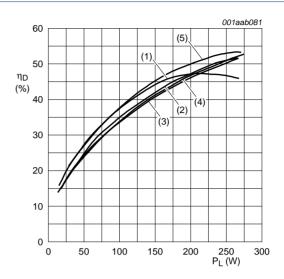
Fig 5. Power gain as a function of load power; typical values



 T_h = 25 °C; V_{DS} = 36 V; I_{Dq} = 150 mA; class-AB; t_p = 100 μ s; δ = 10 %.

- (1) f = 960 MHz
- (2) f = 1030 MHz
- (3) f = 1090 MHz
- (4) f = 1140 MHz
- (5) f = 1215 MHz

Fig 6. Load power as a function of input power; typical values



 T_h = 25 °C; V_{DS} = 36 V; I_{Dq} = 150 mA; class-AB; t_p = 100 μ s; δ = 10 %.

- (1) f = 960 MHz
- (2) f = 1030 MHz
- (3) f = 1090 MHz
- (4) f = 1140 MHz
- (5) f = 1215 MHz

Fig 7. Efficiency as a function of load power; typical values

Product data sheet

9. Package outline



SOT502A

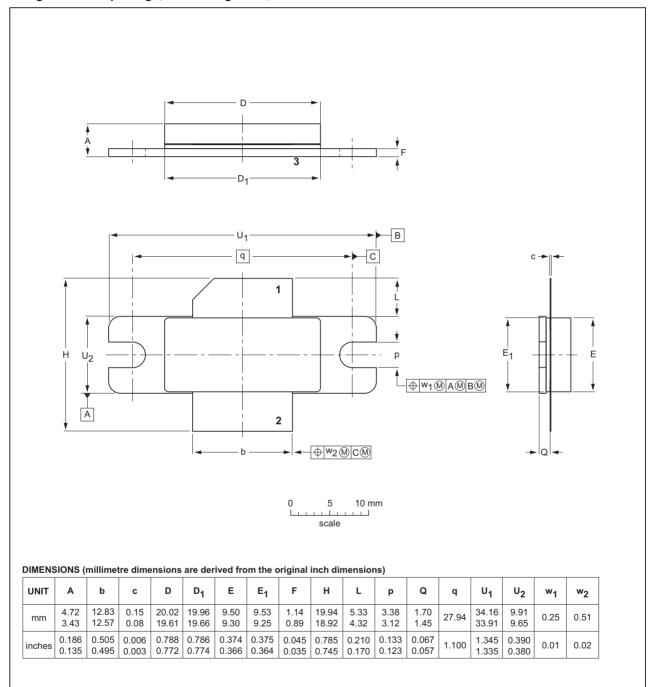


Fig 8. Package outline SOT502A

IEC

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ISSUE DATE

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12-05-02

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OUTLINE

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SOT502A

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
DC	Direct Current
DME	Distance Measuring Equipment
JTIDS	Joint Tactical Information Distribution System
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
Mode-S	Mode Select
RF	Radio Frequency
SMD	Surface Mounted Device
TACAN	TACtical Air Navigation
TCAS	Traffic Collision Avoidance System
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA0912-250R#4	20150901	Product data sheet	-	BLA0912-250R v.3
Modifications:	of Ampleon.	this document has been redove		
BLA0912-250R v.3	20101201	Product data sheet	-	BLA0912-250R v.2
BLA0912-250R v.2	20101015	Product data sheet	-	BLA0912-250R v.1
BLA0912-250R v.1	20100303	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Product data sheet

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BLA0912-250R

Avionics LDMOS power transistor

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