Pin Configuration

(TOP VIEW)

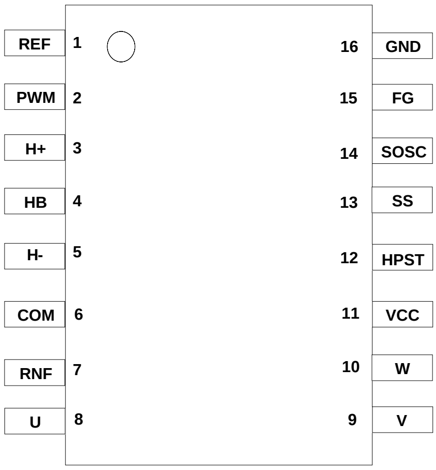


Figure1. Pin configuration

Pin Description

Pin No.	Pin Name	Function
1	REF	Reference voltage terminal
2	PWM	Output duty control terminal
3	H+	Hall + input terminal
4	HB	Hall bias terminal
5	H-	Hall – input terminal
6	COM	Motor central tap terminal
7	RNF	Output current detecting resistor connecting terminal
8	U	Motor drive output U terminal
9	V	Motor drive output V terminal
10	W	Motor drive output W terminal
11	VCC	Power supply terminal
12	HPST	Hybrid phase setting terminal
13	SS	Capacitor for Soft-Start current charge connecting terminal
14	SOSC	Oscillating capacitor connecting terminal for open sine drive
15	FG	Signal output terminal FG
16	GND	Ground terminal

Block Diagram

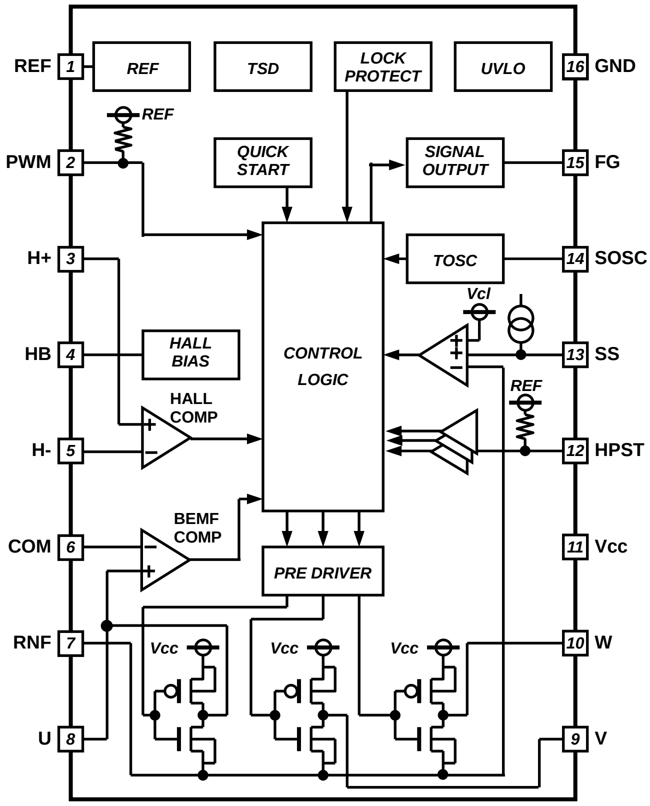


Figure 2. Block diagram

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Power Supply Voltage [VCC]	V_{CC}	20	V
Power Dissipation	P_d	0.875	W
Operating Temperature Range	T_{opr}	-40 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Motor Drive Output Voltage [U, V, W]	V_O	20	V
Motor Drive Output Current [U, V, W]	I_O	1.0 (Note 2)	A
FG Output Voltage	V_{FG}	20	V
FG Output Current	I_{FG}	10	mA
REF Output Current Ability	I_{REF}	10	mA
HB Output Current Ability	I_{HB}	10	mA
Input Voltage1 [COM]	V_{IN1}	18	V
Input Voltage2 [PWM, HPST, SS]	V_{IN2}	7	V
Input Voltage3 [H+, H-]	V_{IN3}	7	V
Input Voltage4 [RNF]	V_{IN4}	4.5	V
Maximum Junction Temperature	T_j	150	°C

(Note 1) Derating in done 7.0 mW/°C for operating above Ta≧25°C (Mount on 2-layer 70.0mm x 70.0mm GND board)
(Note 2) This value is not exceed Pd and ASO

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended operating condition

Parameter	Symbol	Limit	Unit
Power Supply Voltage [VCC]	V_{CC}	5.0 to 16	V
Input Voltage1 [COM]	V_{IN1}	5.0 to 16	V
Input Voltage2 [PWM, HPST, SS]	V_{IN2}	0 to V_{REF}	V
Input Voltage3 [H+, H-]	V_{IN3}	0 to V_{HB}	V
Input frequency (PWM)	F_{PWM}	20 to 50	kHz

Electrical characteristics (Unless otherwise specified Ta=25°C, Vcc=12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	3.6	6	8.4	mA	
<Hall input>						
Hall Input Hysteresis Voltage +	V_{HYS+}	5	10	15	mV	
Hall Input Hysteresis Voltage -	V_{HYS-}	-15	-10	-5	mV	
<REF / HB>						
REF Voltage	V_{REF}	4.65	5.00	5.35	V	I_{REF}=-5mA
Hall Bias Voltage	V_{HB}	1.00	1.25	1.50	V	I_{HB}=-5mA
<SOSC>						
SOSC High Voltage	V_{SOSCH}	0.8	1.0	1.2	V	
SOSC Low Voltage	V_{SOSCL}	0.3	0.5	0.7	V	
SOSC Charge Current	I_{CSOSC}	-46	-40	-34	µA	V_{SOSC}=0.75V
SOSC Discharge Current	I_{DSOSC}	34	40	46	µA	V_{SOSC}=0.75V
<PWM>						
PWM Input High Voltage	V_{PWM}	2.5	-	-	V	
PWM Input Low Voltage	V_{PWM}	-	-	0.8	V	
PWM Input Current	I_{PWM}	-75	-50	-25	µA	V_{PWM}=0V
<Current Limit>						
Current Limit Voltage	V_{CL}	120	150	180	mV	
<Soft Start>						
SS Charge Current	I_{SS}	-2.4	-1.8	-1.2	µA	
<FG>						
FG Output Low Voltage	V_{FGL}	-	0.3	0.4	V	I_{FG}=5mA
FG Output Leak Current	I_{FGL}	-	-	10	µA	V_{FG}=20V
<Lock Protection>						
Lock Detection ON Time	t_{ON1}	0.6	1	1.6	s	
Lock Detection OFF Time	t_{OFF}	3.3	5	8.3	s	
<Output>						
Output High Voltage	V_{OH}	-	0.15	0.2	V	I_O= -0.3A, for Vcc Voltage
Output Low Voltage	V_{OL}	-	0.09	0.16	V	I_O= 0.3A
<Lead angle Setting>						
HPST Input Current	I_{HPST}	-35	-25	-15	µA	V_{HPST}=0V
AUTO Mode	V_{HPST1}	3.85	-	5.00	V	
25° Mode	V_{HPST2}	2.6	-	3.65	V	
10° Mode	V_{HPST3}	1.35	-	2.40	V	
0° Mode	V_{HPST4}	0	-	1.15	V	

About a current item, define the inflow current to IC as a positive notation, and the outflow current from IC as a negative notation.

Application Example

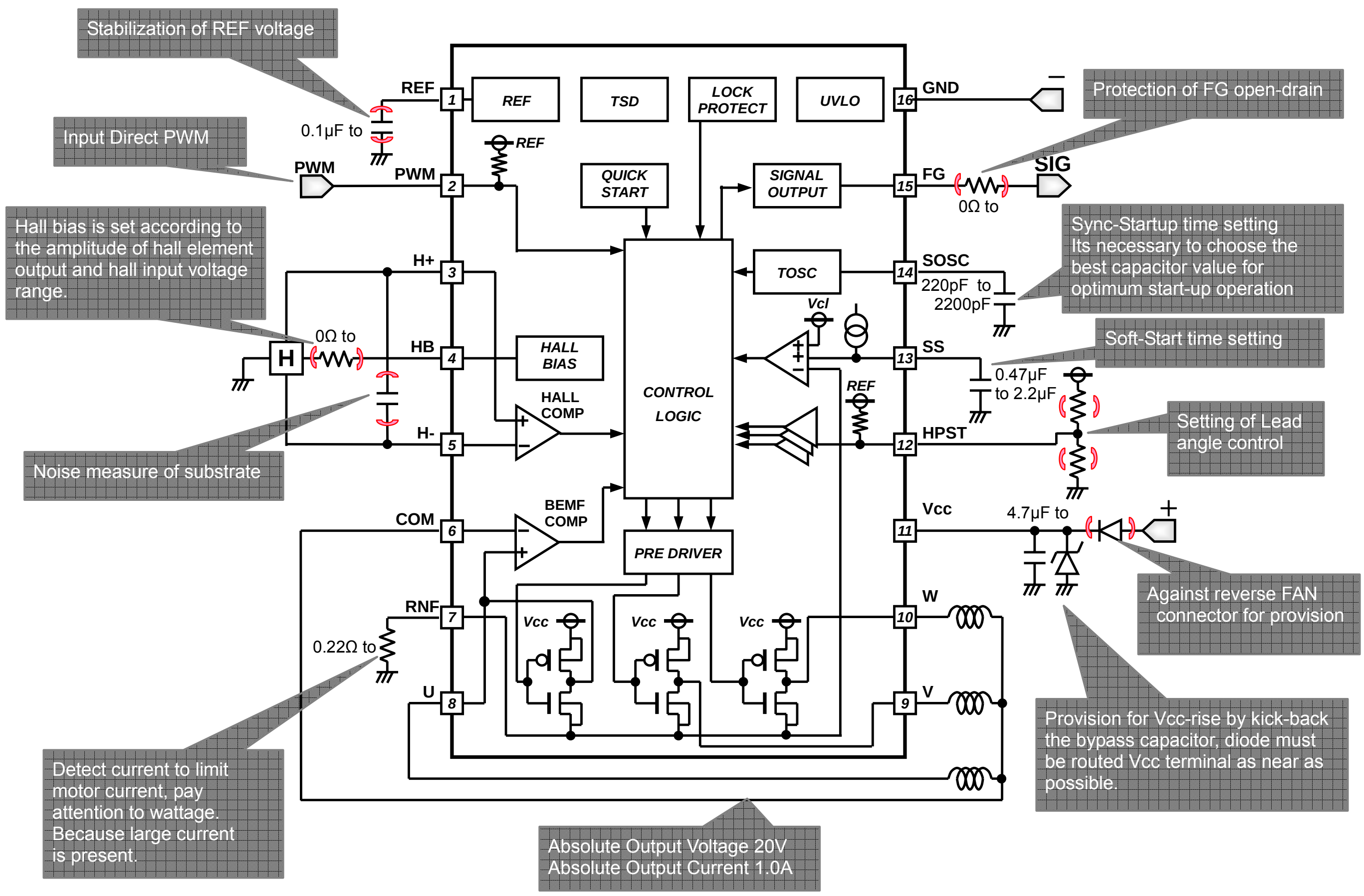


Figure 3. Application

Substrate design note

a) IC power, motor outputs, and motor ground lines are made as fat as possible.
b) IC ground (signal ground) line arranged near to (–) land.
c) The bypass capacitor is arrangement near to VCC pin.
d) When substrates of outputs are noisy, add capacitor as needed.

Typical Performance Curves1 (Reference data)

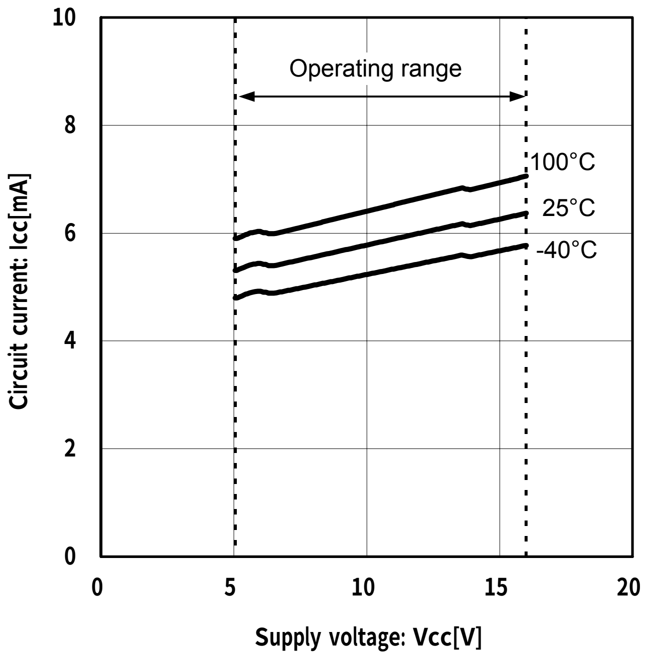


Figure 4. Circuit current

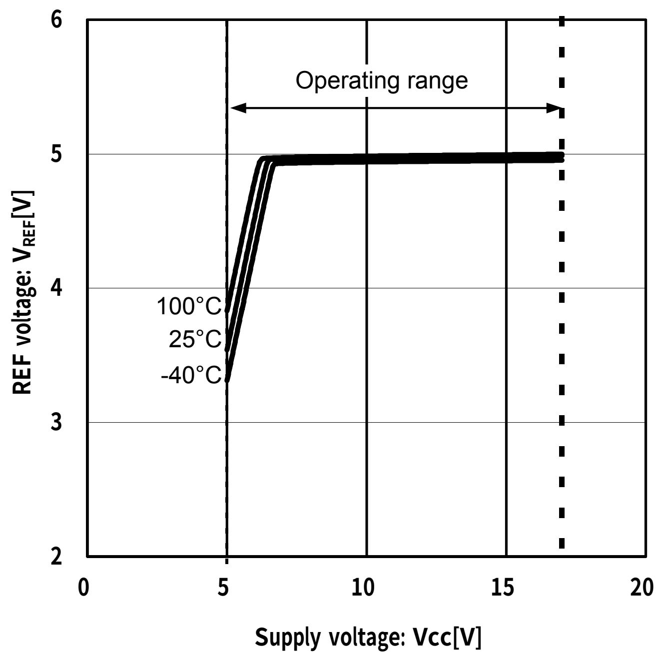


Figure 5. REF Voltage

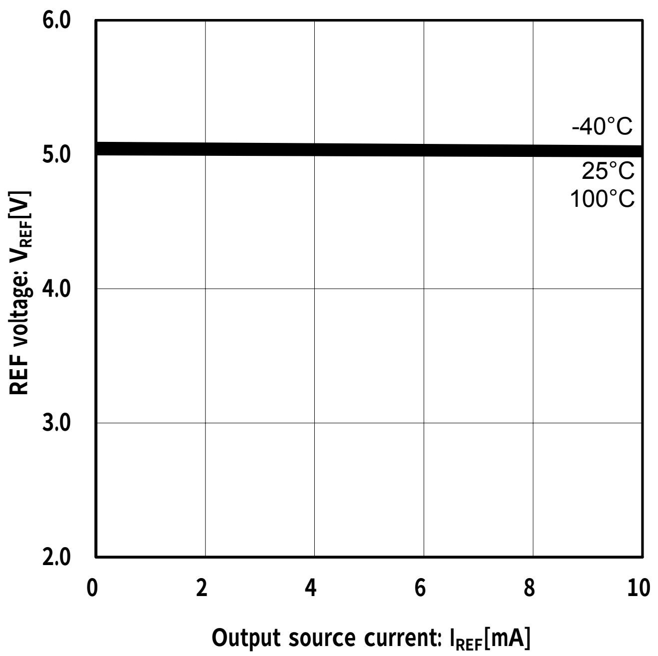


Figure 6. REF Voltage current ability (Vcc=12V)

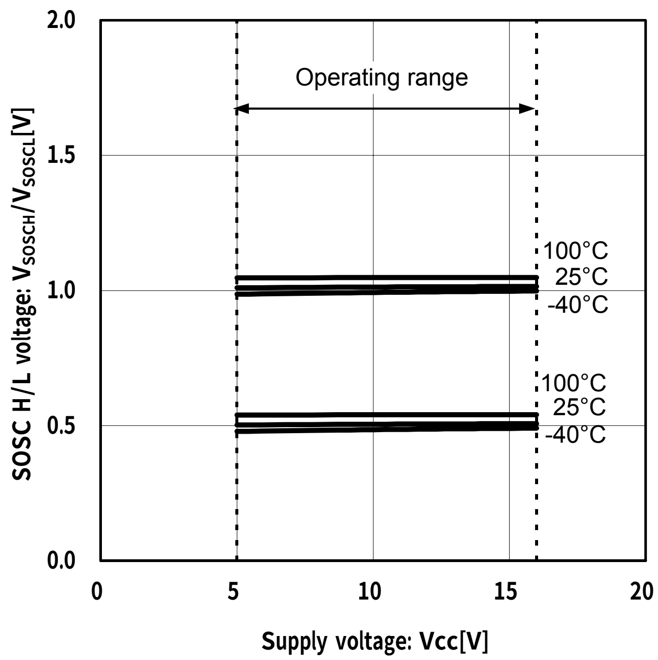


Figure 7. SOSC High/Low Voltage

Typical Performance Curves2 (Reference data)

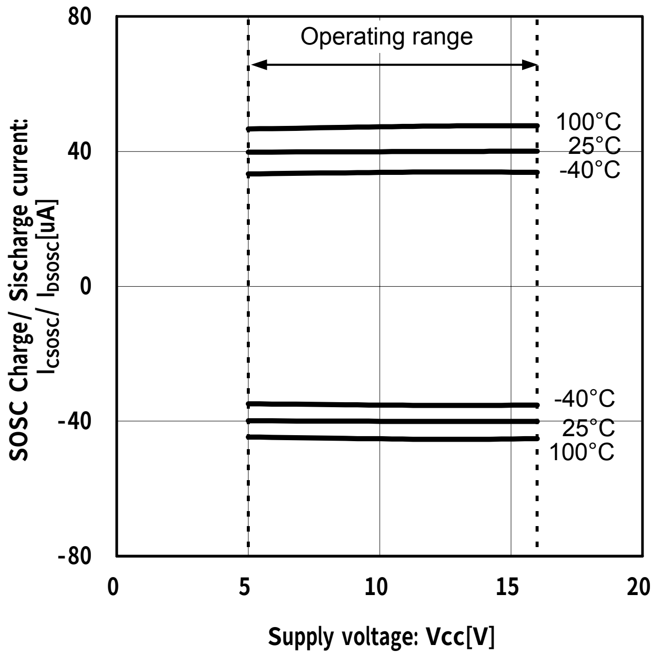


Figure 8. SOSC charge/discharge current

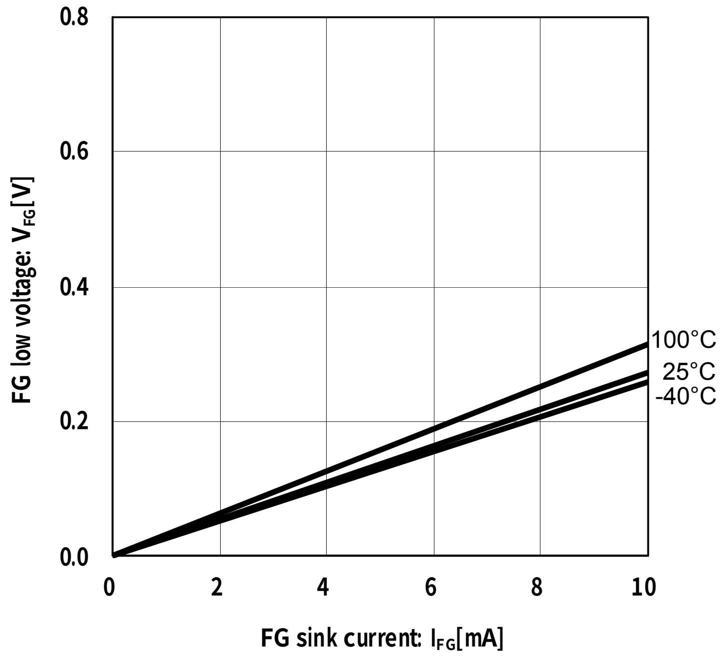


Figure 9. FG Low Voltage (Vcc=12V)

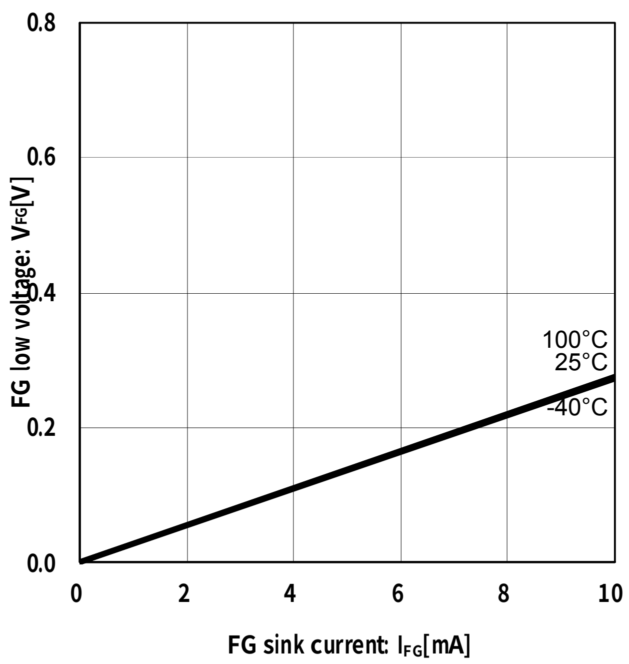


Figure 10. FG low voltage (Ta25°C)

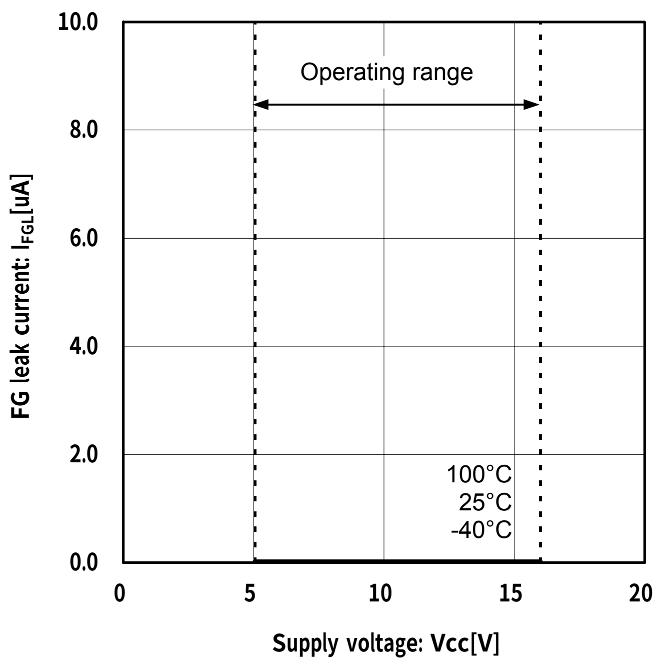


Figure 11. FG leak current

Typical Performance Curves3 (Reference data)

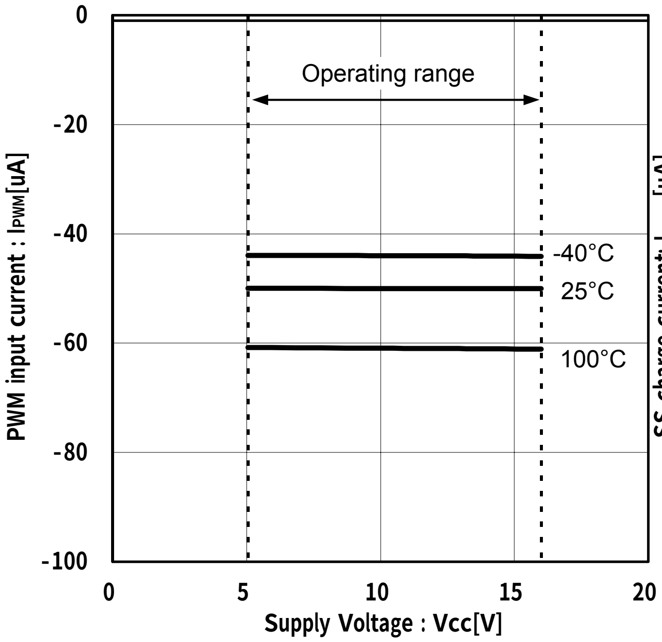


Figure 12. PWM input current

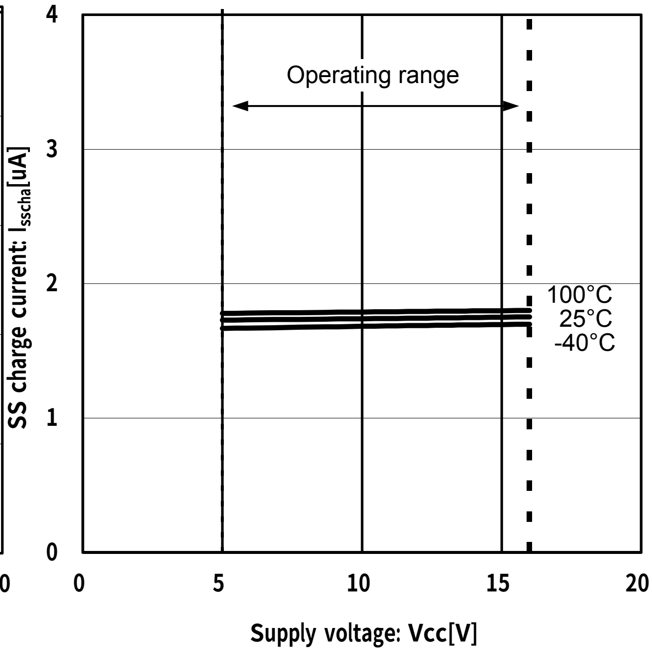


Figure 13. SS charge current

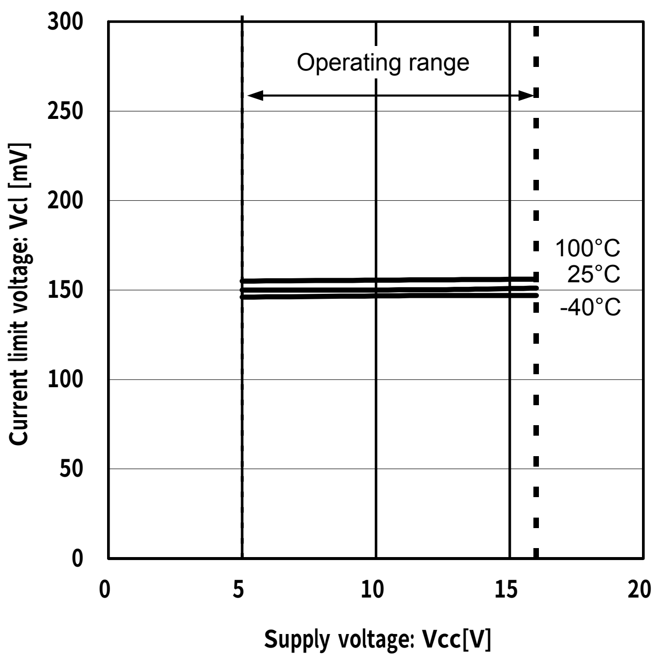


Figure 14. Current limit voltage

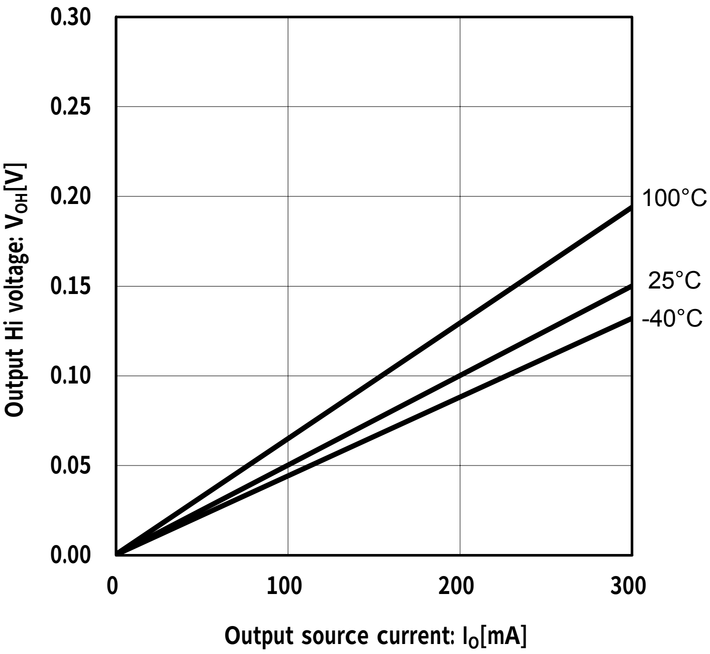


Figure 15. Output Hi Voltage (Vcc=12V)

Typical Performance Curves4 (Reference data)

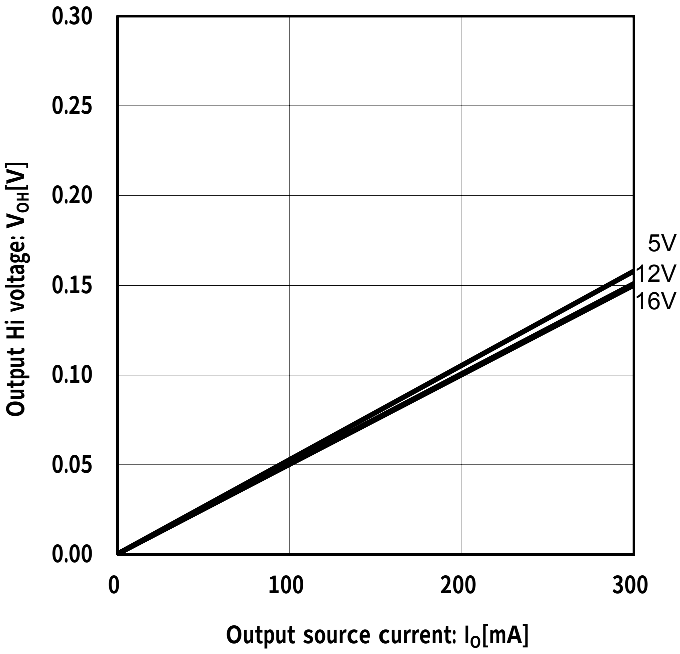


Figure 16. Output Hi Voltage (Ta=25°C)

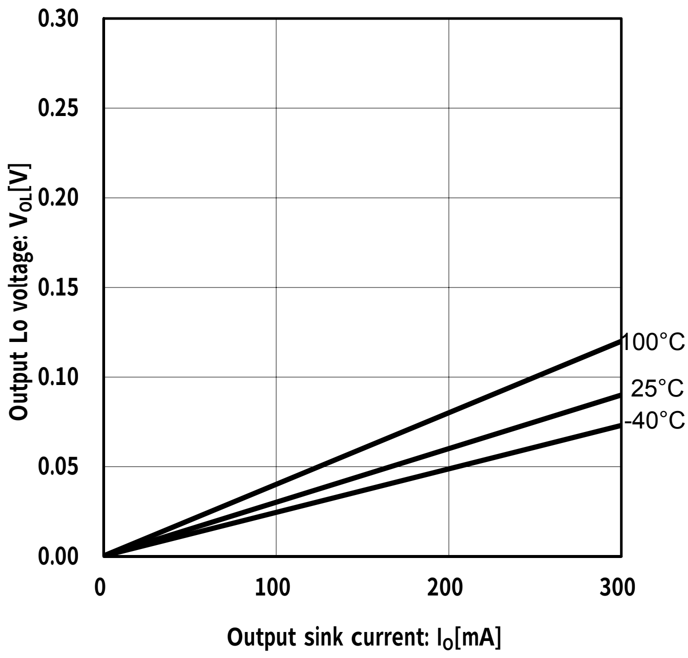


Figure 17 Output Lo Voltage (Vcc=12V)

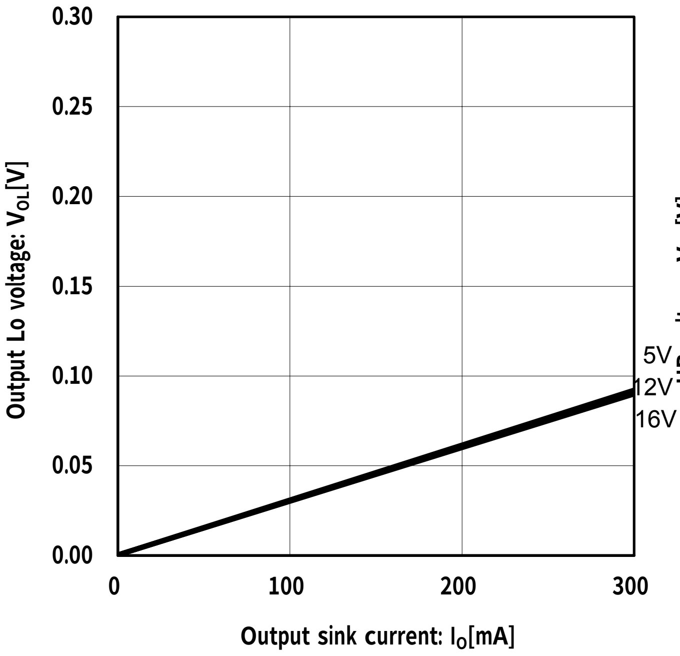


Figure 18 Output Lo Voltage (Ta=25°C)

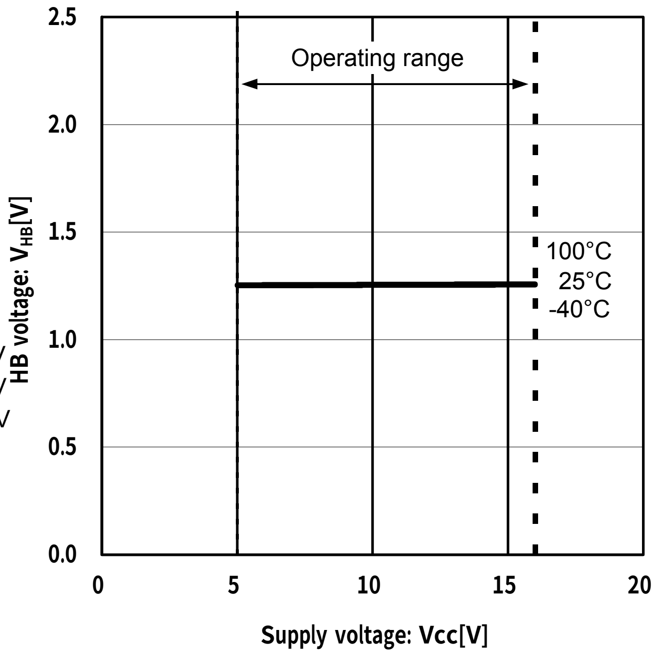


Figure 19 HB Voltage

Typical Performance Curves5 (Reference data)

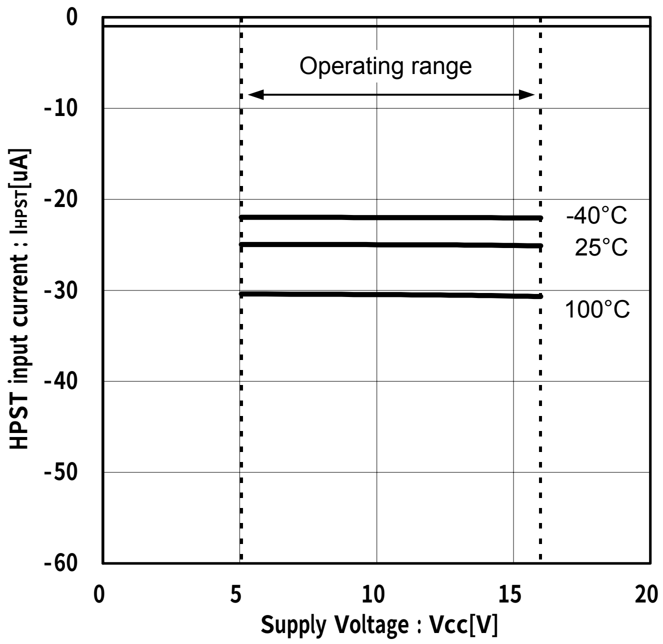


Figure 20. HPST input current

Description of Function Operation

1)1 Hall Full-Sine Drive

BD63241FV is a motor driver IC for Full-Sine driving a three-phase brushless DC motor with 1 hall sensor.

1.1 1Hall detection Full-Sine drive

Full-Sine Synchronized start-up way with 1Hall detection,synchronized start-up mechanism outputs output logic forcibly by using standard synchronized signal (sync signal) and makes motor forward drive. This assistance of motor start-up Full-Sine drive as constant cycle is synchronized driving mechanism. Synchronized frequency is standard synchronized signal.

*1Hall placement

Please place 1Hall element so that phase relations of Hall signal(In HALL signal, the logic links H+ signal) and U phase BEMF voltage are as Figure.21 Hall detection driving timing chart.

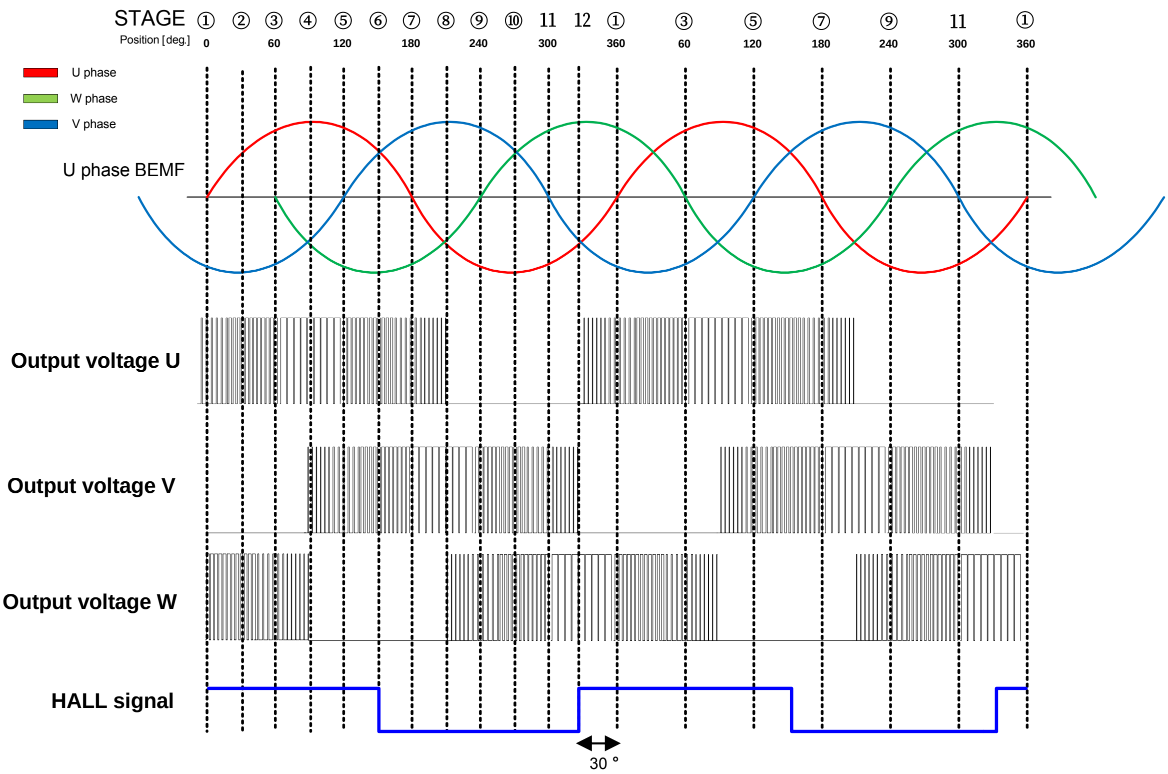


Figure 21. Hall detection driving timing chart

1.2 Start-up mechanism (Automatic 1 Hall Full-Sine start-up mechanism)

Automatic 1Hall Full-Sine drive start-up

Automatic 1Hall Full-Sine drive start-up is start method that outputs Full-Sine wave of internal setting. BD63241FV lets a motor accelerate in gradually raising frequency of output Full-Sine wave set by internal table. BD63241FV has section to compare Hall input signal (=rotation speed signal) with output drive timing. If phase of Hall input signal advances for output driving timing, driving section shifts to normal Hall driving section.
(In addition, automatic Full-Sine start-up section has limitation. Driving section shifts to normal Hall driving section over 27times electrical cycles in automatic Full-Sine start-up.)

Initial output waiting section

Start-up has initial output waiting section at first. In initial output waiting section, output is fixed to specific phase selected by Hall signal. Then section shifts to automatic Full-Sine start-up section.

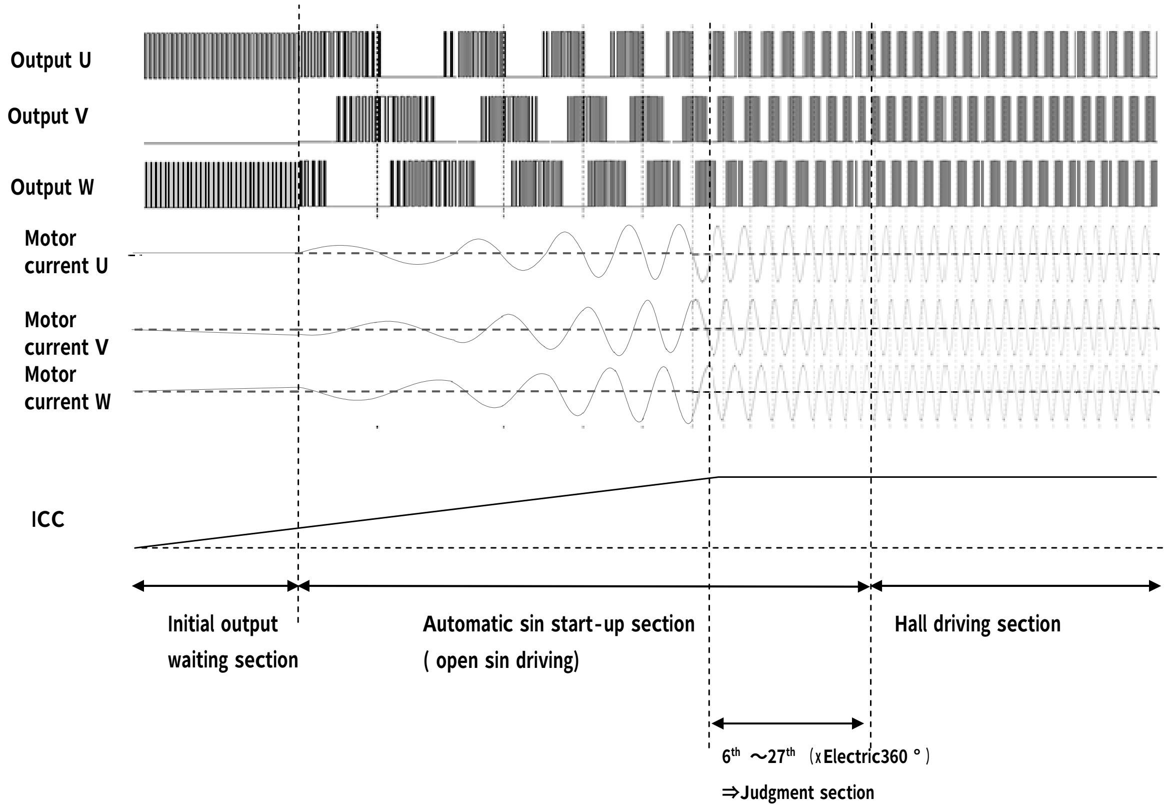


Figure 22. Automatic Full-Sine start-up and Hall detection driving timing

Table 1. Judgment for each section of automatic Full-SIne start-up

Driving section	judgment
Initial output waiting section	Driving Section shifts to Automatic sine start-up section after 400msec. (If hall signal is switched between intital output waiting section, 400msec counter is reset.)
Automatic sine start-up section	If phase of hall input signal advances for output driving timing between 6times～27times electrical cycles in automatic Full-Sine start-up, driving section shifts to normal hall driving section.
	Driving section shifts to normal hall driving section over 27times electrical cycles in automatic sine start-up.

1.3 Rotation speed setting of Automatic Full-Sine start-up section

Driving rotation speed in Automatic Full-Sine start-up section rises by internal start-up setting. Internal start-up setting is set by frequency of SOSC terminal (SOSC frequency can be adjusted by changing external capacitor)
In Fig. 23, this setting is shown.

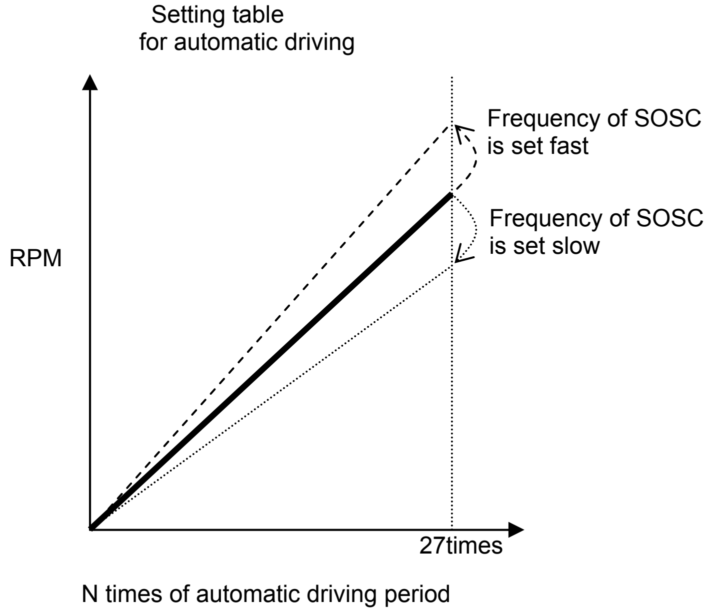


Figure 23. About setting table for automatic Full-Sine start-up section

・Adjusting of rotation speed setting
Rotation speed setting is adjusted by the following expressions

A (5 times electrical cycles from start-up: start of phase judgment section)
A[rpm] = SOSC[kHz] x 10

B (27times electrical cycles from start-up : the upper limit of automatic Full-Sine start-up section)
A[rpm] = SOSC[kHz] x 89.3

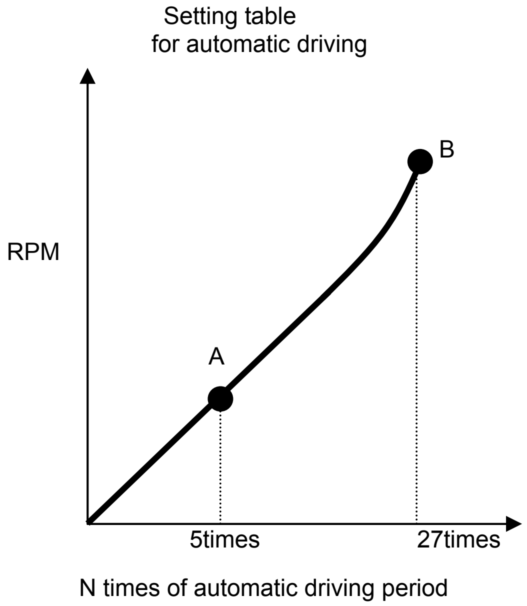


Figure 24. Adjusting for automatic Full-Sine start-up setting table

1.4 Synchronized time (SOSC)

The SOSC terminal starts a self-oscillation by connecting a capacitor between the SOSC terminal and GND terminal. Start-up frequency can be adjusted by changing external capacitor. When the capacitor value is small, rotation speed setting of automatic sine start-up section becomes fast. It is necessary to choose the best capacitor value for optimum start-up operation. Relationship between external capacitor and SOSC frequency is shown in below.

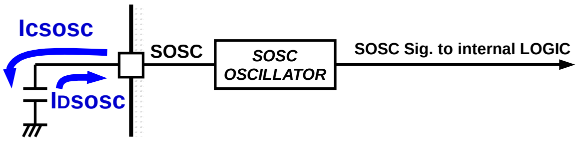


Figure 25. SOSC Capacitor and IC internal circuit

Equation

$$Sosc = 2x\frac{C_{SOSC}V_{SOSC}}{I}$$

C_{SOSC} :SOSC pin capacitor value
V_{SOSC} :SOSC pin Hi voltage – Lo voltage= 0.5V (typ.)
I :SOSC pin charge and discharge current

SOSC Capacitor (Csosc) [pF]	SOSC frequency (Fsosc) [kHz]
330	121.2
470	85.1
1000	40.0

Example
C_{SOSC} = 1000pF.
SOSC frequency = 40kHz (typ.).
SOSC period = 25us.

1.5 U, V, W phase and FG output signals

The timing charts of the output signals from the U, V and W phases as well as the FG terminal is shown (Figure 9). The three phases are driving in the order of U, V and W phases. About FG signal output, assuming that a three-slot tetrode motor is used, two pulse outputs of FG are produced for one motor cycle.

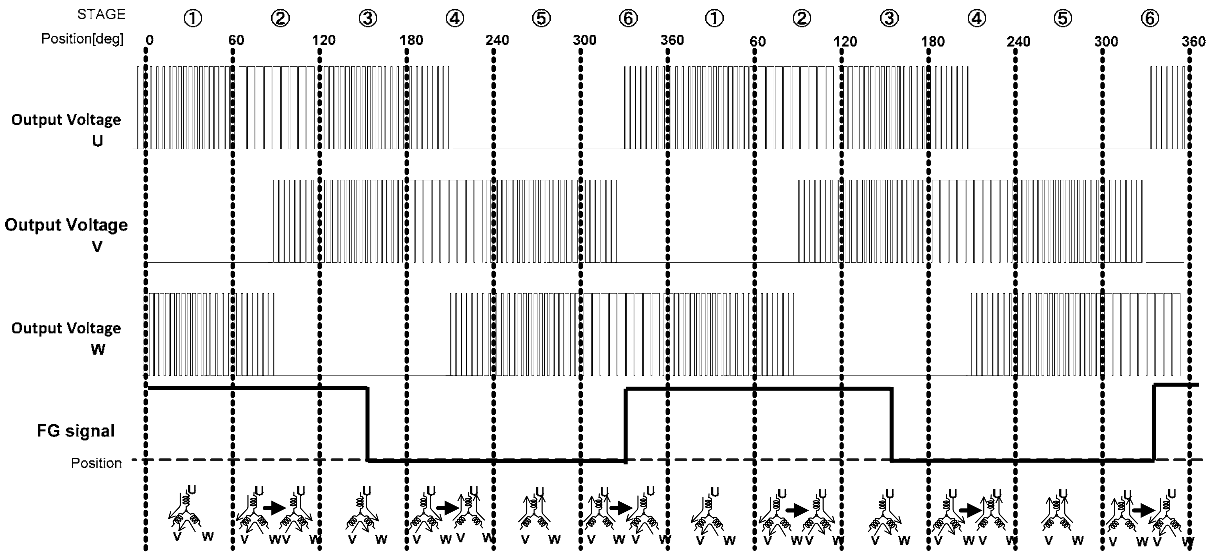


Figure 26. Timing chart of U, V, W, FG output signal (lead angle 0 °)

Table 2. Truth table of normal operation

Output pattern	Motor output		
	Motor output U	Motor output V	Motor output W
1	PWM	L	PWM
2	PWM	L→**PWM**	PWM→L
3	PWM	PWM	L
4	PWM→L	PWM	L→**PWM**
5	L	PWM	PWM
6	L→**PWM**	PWM→L	PWM

* **About the output pattern, It changes in the flow of "1→2→3 ～ 6→1".H; High, L; Low**

FG signal is masked between 5th of electrical cycles automatic Full-Sine start-up section .

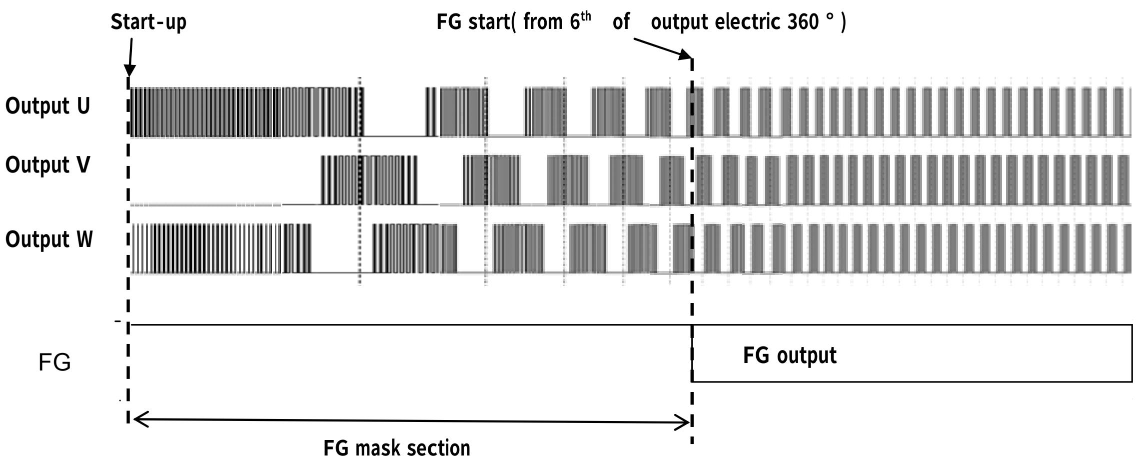


Figure 27. About FG mask section

2) Lock Protection Feature, Automatic Recovery Circuit

To prevent passing a coil current on any phase when a motor is locked, it is provided with a function, which can turn Low all output or a certain period of time (TOFF typ. 5.0s) and then automatically restore itself to the normal operation. During the motor rotation, Hall signal input detects hall signal switching continuously. And Hall signal input doesn't detect when a motor is locked. When the Hall signal switching is not detected for a predetermined period of time, it is judged that the motor is locked.
BD63241FV has 2 lock judgment conditions (start-up, normal driving)

a) Lock Protection in Start-up(Ton typ. 1.0s)
When hall signal switching is not detected during first 1.0sec (Ton) in initial output waiting section & automatic sine start-up section, it is judged that the motor is locked.
(But if Output driving period of Automatic sine start-up doesn't reach until a half period, this judgment is extended until a half period.) In Fig. 11, the timing chart is shown.

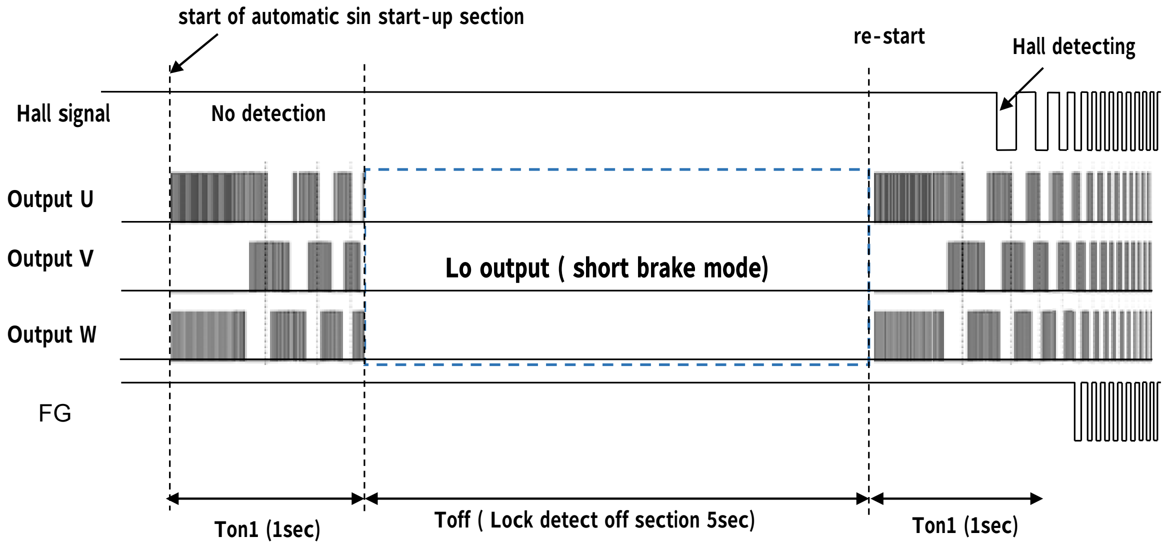


Figure 28. Lock protection operation in start-up

a) Lock Protection in normal hall driving

When the Hall signal switching (detection in the falling edge) is not detected between 400msec in normal hall driving section, it is judged that the motor is locked. In Fig. 12, the timing chart is shown.

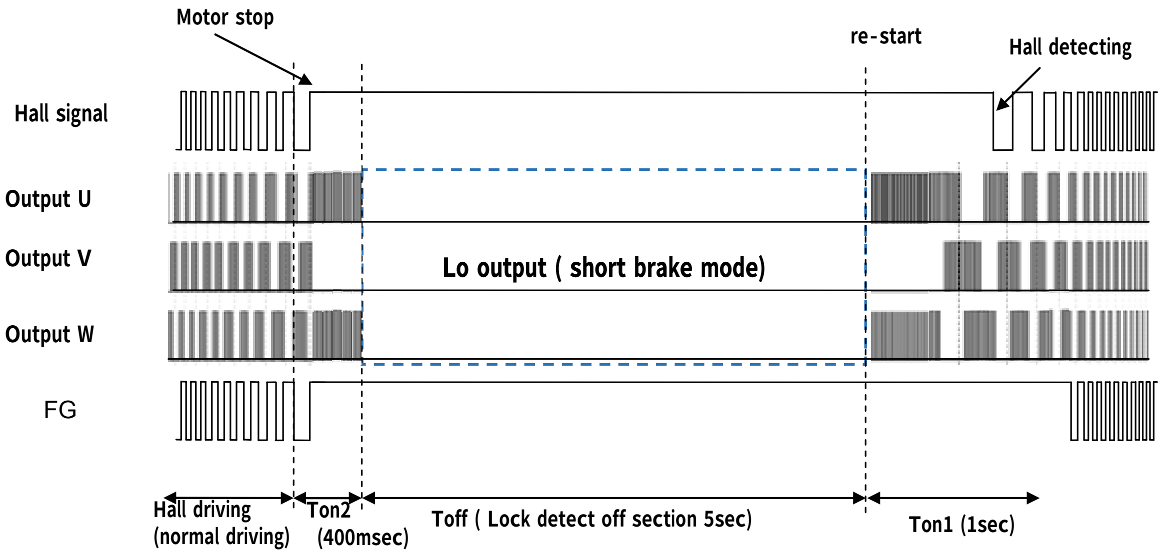


Figure 29. Lock protection operation in normal hall driving

3) UVLO（Under voltage lock out circuit）

In the operation area under the guaranteed operating power supply voltage of 16V (typ.), the transistor on the output can be turned OFF at a power supply voltage of 3.9V (typ.). A hysteresis width of 300mV is provided and a normal operation can be performed at 4.2V(typ.). This function is installed to prevent unpredictable operations, such as a large amount of current passing through the output, by means of intentionally turning OFF the output during an operation at a very low power supply voltage which may cause an abnormal function in the internal circuit.
About turning off a output voltage at UVLO, It becomes a OFF mode.
(Upper MOS FET and Under MOS FET are turned OFF.)

4) Current limit

A current passing through the motor coil can be detected on the output current detection resistance to prohibit a current flow larger than a current limit value (motor output off).The current limit value is determined by setting of the IC internal limit(Vcl) :150mV (typ.),and the output current detection resistance value using the following in below equation.

Io[A] = Vcl[V] / R1[Ω]
= 150[mV] / 0.2[Ω]
=0.750[A]

P_R[W] = Vcl[V] x Io[A]
= 150[mV] x 0.75[A]
= 0.19[W]

When no-use current limit function, RNF terminal is shorted GND.

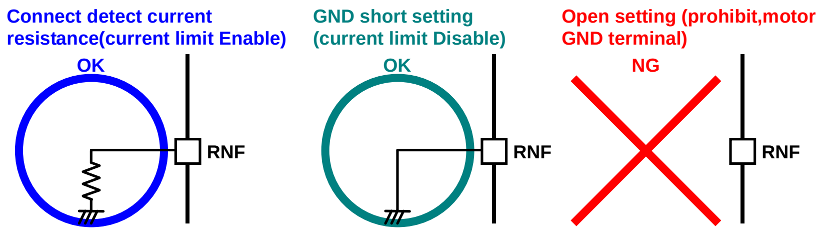


Figure30． Current limit function, RNF terminal setting

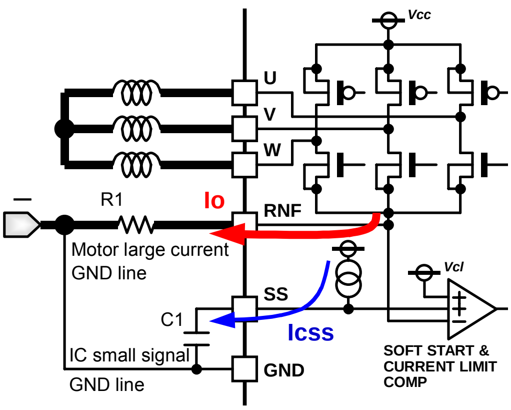


Figure 31. small signal and large current GND line

In Figure31, IC small signal GND line should be separated Motor large current GND line connected R1.Same as soft start Capacitor.(Pay attention to design board(b)) item reference)

5) Soft start

To prevent lush current, slowly up to rotation speed, when motor start in VCC on, quick start, restart lock detect on etc. Soft start time set by SS terminal connected CAP to charge current. No use soft start, SS terminal set open. 1uF is recommended for setting value at first, or 0.47uF-2.2uF.

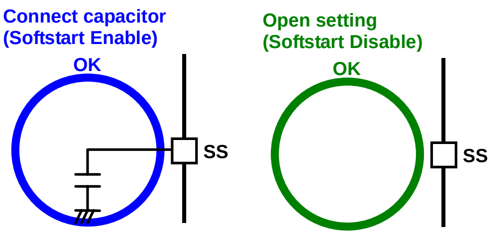


Figure 32. Soft start function, SS terminal setting

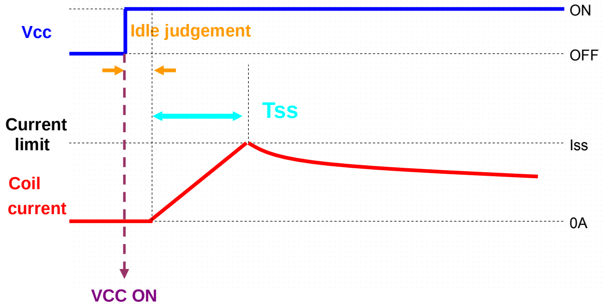


Figure 33. Characteristic of motor output current at soft-start setting separate

In Figure 31, SS terminal charge current (Icss) is 1.8uA (typ.), Set SS terminal connect Capacitor (C1) , lead to that current time(Tss) in below equation. Icss1 is reduced 1/15, SS terminal charge current (Icss) in internal IC.

Tss[s] = (C1[F] x Iss[A] x R1[Ω]) / Icss1[A]

(ex.) Assuming that C1 = 1.0[μF], Iss = 1.5[A], R1 = 0.1[Ω] then, soft-start time is 1.25[s]

(When R1=0.1**Ω**,current limit =1.5A)

Tss[s] = (1.0[μF] x 1.5[A] x 0.1[Ω]) / (1.9/15) [uA]

= 1.25 [s]

6) Auto lead angle control and Fix lead angle control at HPST terminal

By the setting of the HPST terminal, Lead angle setting is accomplished.
Set by the following tables, set it by the resistance division from REF terminal.

Table 3.

lead angle mode	HPST terminal voltage (V)
Auto	3.85 - 5.0
25°	2.6 - 3.65
10°	1.35 - 2.4
0°	0 - 1.2

*HPST terminal is open, auto setting

Safety measure

1. Reverse connection protection diode
   Reverse connection of power results in IC destruction as shown in Figure34a. When reverse connection is possible, reverse connection protection diode must be added between power supply and V_{CC}.

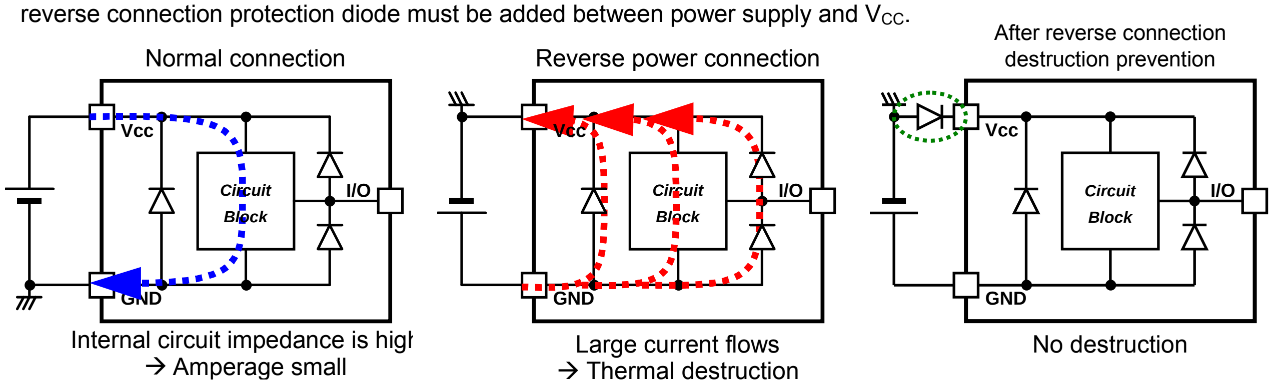


Figure.34a Flow of current when power is connected reversely

2. Measure against V_{CC} voltage rise by back electromotive force
   Back electromotive force (Back EMF) generates regenerative current to power supply. However, when reverse connection protection diode is connected, V_{CC} voltage rises because the diode prevents current flow to power supply.

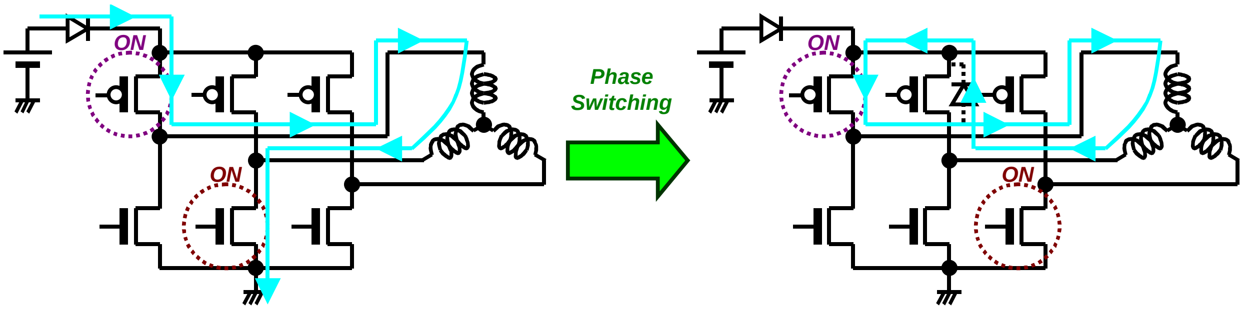


Figure. 34b Vcc voltage and output voltage rise by back electromotive

When you use reverse connection protection diode, Please connect Zenner diode, or capacitor.
Do not exceed absolute maximum ratings Vcc=20V.

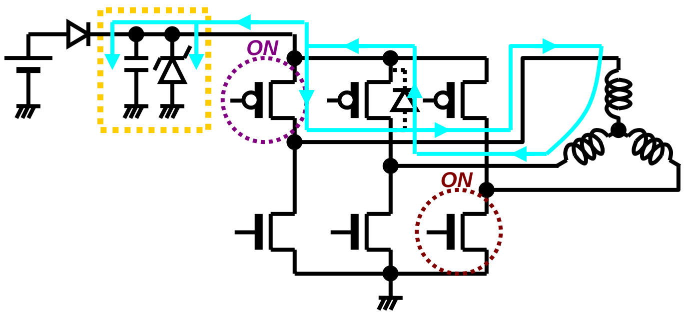


Figure.34c effect of the rise in voltage by connecting Zenner diode, or capacitor

3. Problem of GND line PWM switching
   Do not perform PWM switching of GND line because GND terminal potential cannot be kept to a minimum.

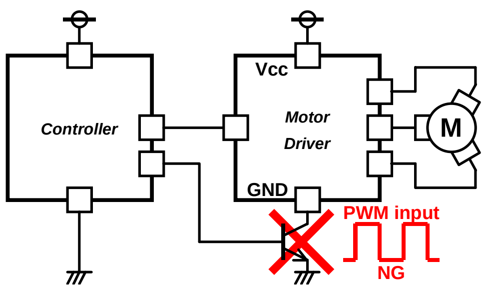


Figure 34d. GND line PWM switching prohibited

Power dissipation

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25°C (normal temperature). IC is heated when it consumes power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, etc, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is in general equal to the maximum value in the storage temperature range.

Heat generated by consumed power of IC is radiated from the mold resin or lead frame of package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called heat resistance, represented by the symbol θja[°C/W]. This heat resistance can estimate the temperature of IC inside the package. Figure 35a. shows the model of heat resistance of the package. Heat resistance θja, ambient temperature Ta, junction temperature Tj, and power consumption P can be calculated by the equation below:

$$\theta ja = (Tj - Ta) / P \ [°C/W]$$

Thermal derating curve indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θja. Thermal resistanceθja depends on chip size, power consumption, package ambient temperature, packaging condition, wind velocity, etc., even when the same package is used. Thermal derating curve indicates a reference value measured at a specified condition. Figure 35b. shows a thermal derating curve (Value when mounting FR4 glass epoxy board 70[mm]×70[mm] ×1.6[mm] (copper foil area below 3[%]))

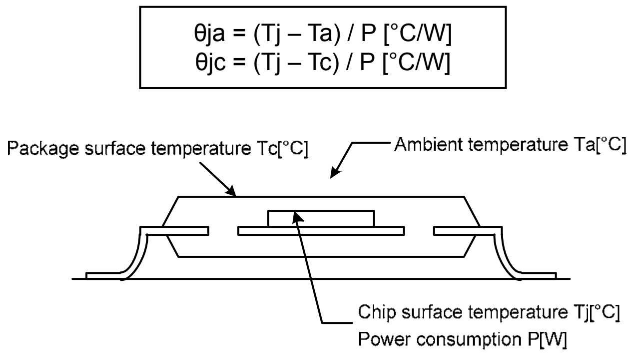


Figure 35a. Thermal resistance

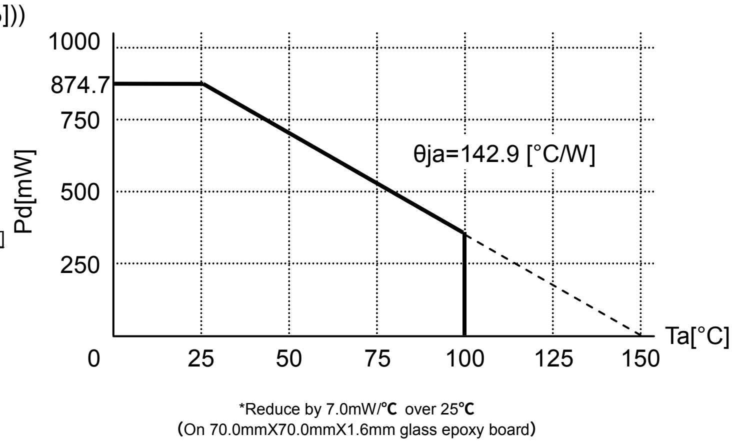
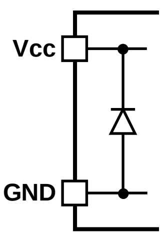


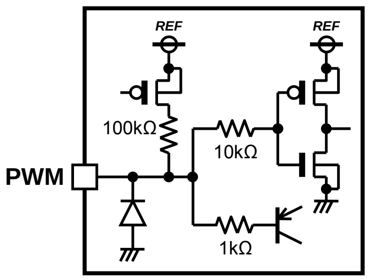
Figure 35b.Thermal derating curve

Equivalent circuit (resistor is reference value)

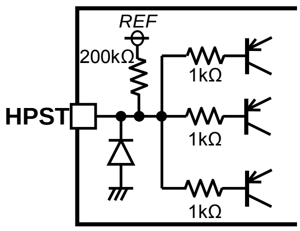
1) Vcc,GND terminal



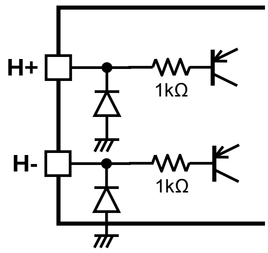
2) PWM terminal



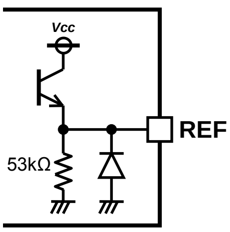
3) HPST terminal



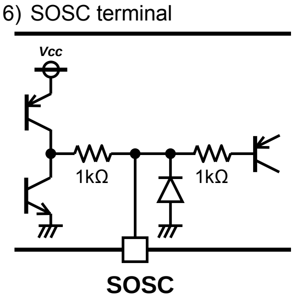
4) H+,H- terminal



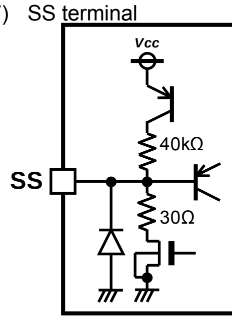
5) REF terminal



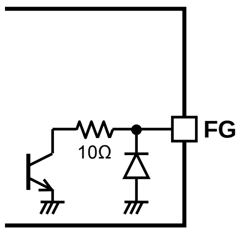
6) SOSC terminal



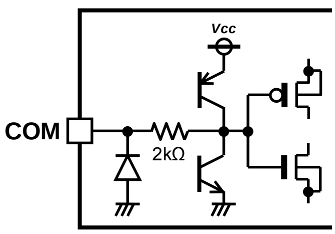
7) SS terminal



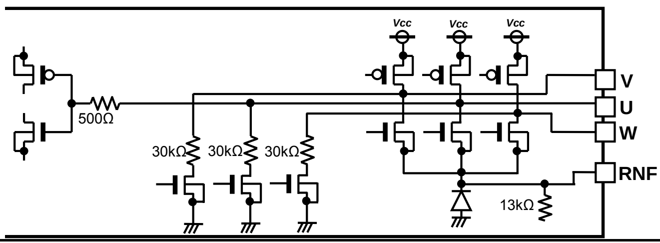
8) FG terminal



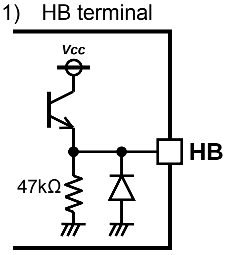
9) COM terminal



10) U,V,W,RNF terminal



11) HB terminal



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 74.2mm x 74.2mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

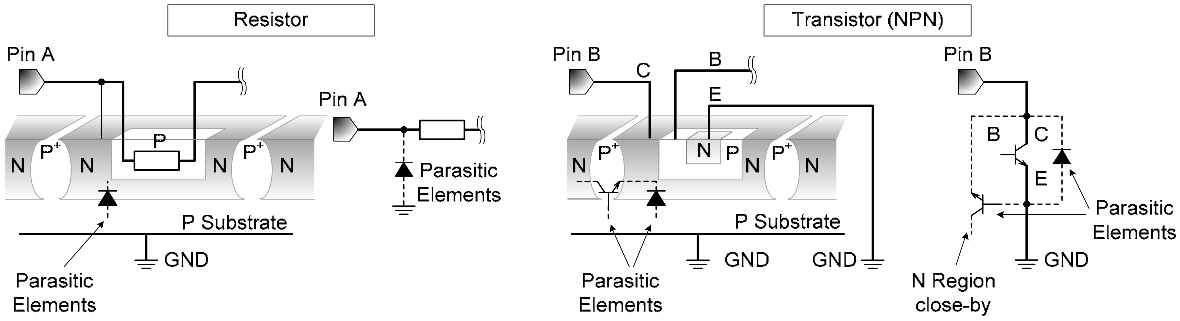


Figure 36. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

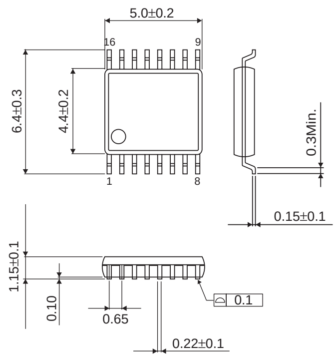
B	D	6	3	2	4	1	-	E 2

Part Number

Packaging and forming specification
E2: Embossed tape and reel

Physical dimension tape and reel information

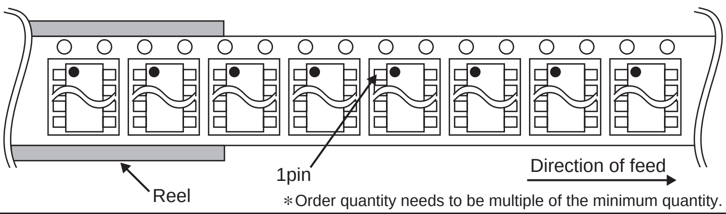
SSOP-B16



(Unit : mm)

<Tape and Reel information>

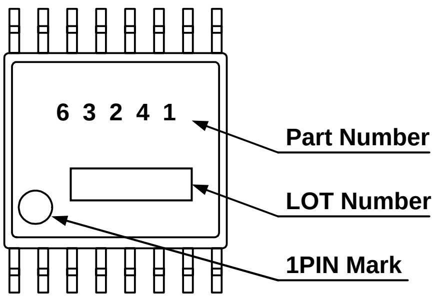
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Marking diagram

SSOP-B16 (TOP VIEW)



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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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