1. Description

The Atmel® ATA6632xx device family includes two basic products; a LIN system basis chip (SBC) and a low-drop voltage regulator with compatible footprints.

The Atmel ATA663231/54 (system basis chip) is a fully integrated LIN transceiver, designed according to the LIN specification 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2, with a low-drop voltage regulator (3.3V/5V/85mA). The combination of voltage regulator and bus transceiver makes it possible to develop simple but powerful slave nodes in LIN bus systems. Atmel ATA663231/54 is designed to handle the low-speed data communication in vehicles (for example, in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20Kbaud. The bus output is designed to withstand high voltage. Sleep mode and silent mode guarantee minimized current consumption even in the case of a floating or a short-circuited LIN bus.

The Atmel ATA663201/03 (voltage regulator) is a fully integrated low-drop voltage regulator, with 3.3V/5V output voltage and 85mA current capability. It is especially designed for the automotive environment. A key feature is that the current consumption is always below 170µA (without load), even if the supply voltage is below the regulator's nominal output voltage.

Table 1-1. ATA6632xx Device Family

Description	Atmel ATA6632xx
LIN-SBC with 3.3V regulator	31
LIN-SBC with 5V regulator	54
Voltage regulator 3.3V	01
Voltage regulator 5V	03

Figure 1-1. Block Diagram LIN Transceiver with Integrated Voltage Regulator (SBC)

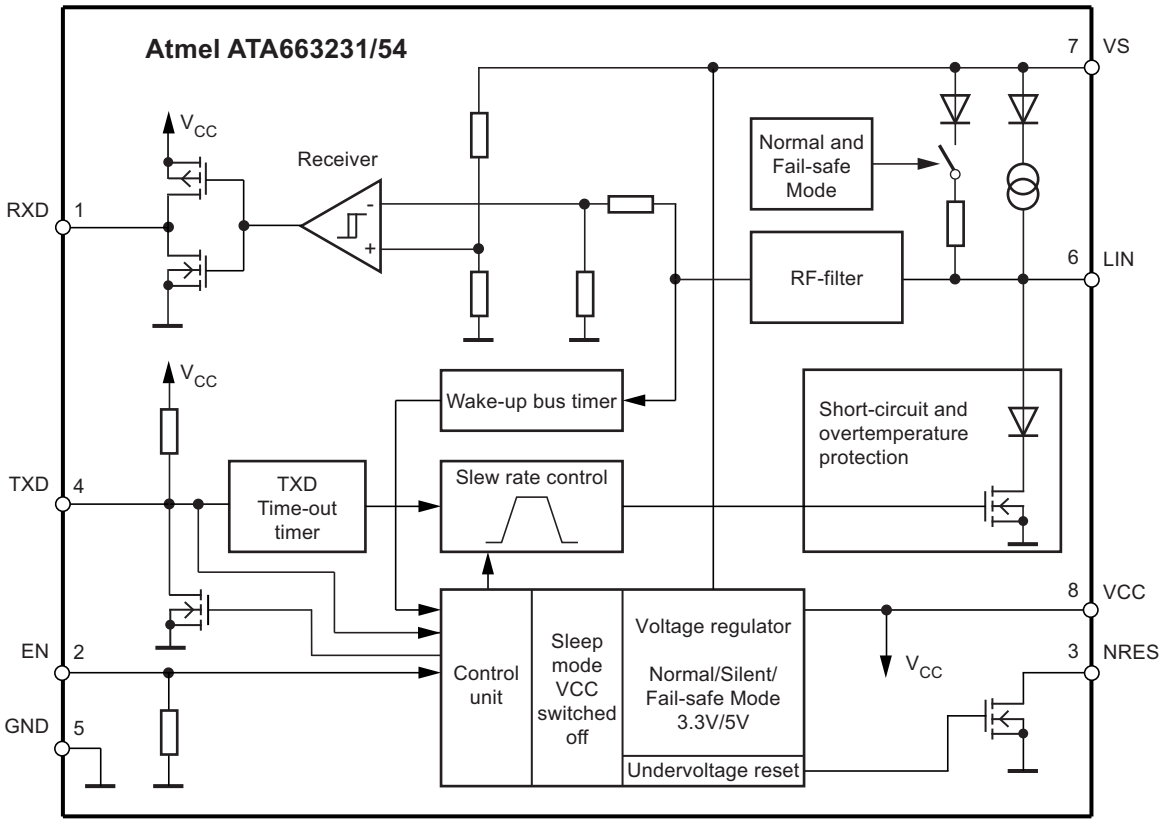
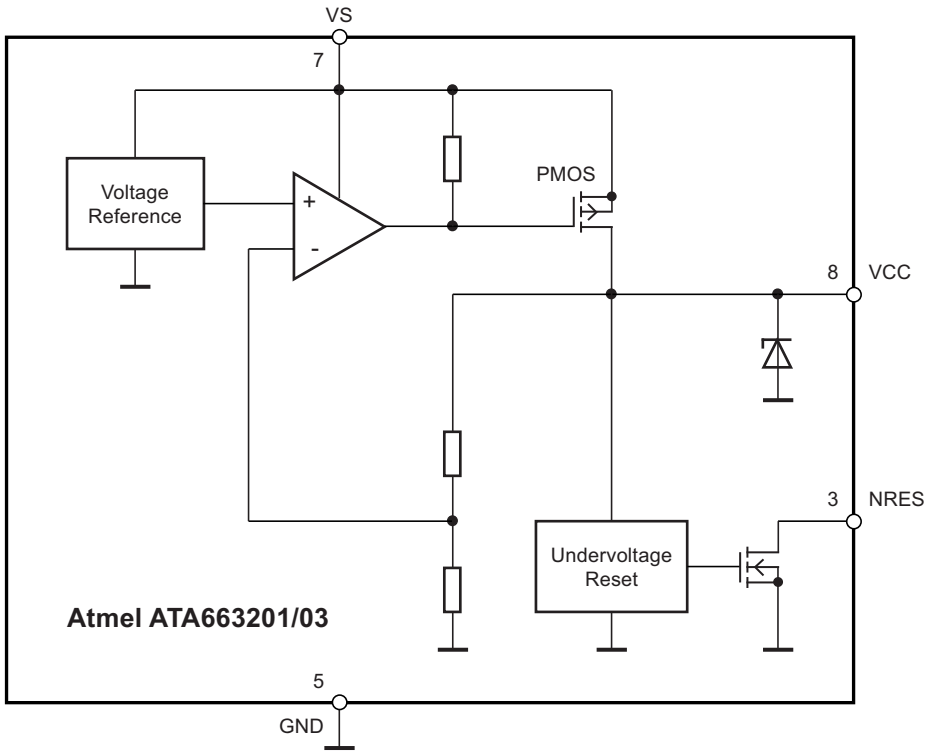


Figure 1-2. Block Diagram Voltage Regulator



2. Pin Configuration

Figure 2-1. Pinning DFN8

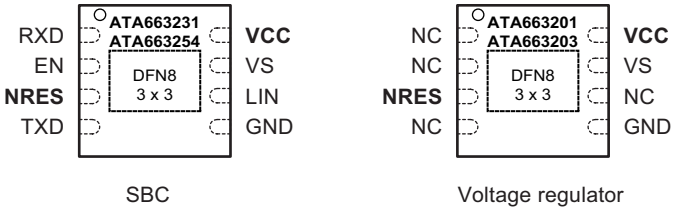


Figure 2-2. Pinning SO8

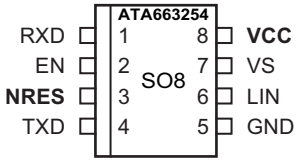


Table 2-1. Pin Description

Pin	Symbol	Function
1	RXD	Receive data output
2	EN	Enables normal mode if the input is high
3	NRES	VCC undervoltage output, open drain, low at reset
4	TXD	Transmit data input
5	GND	Ground
6	LIN	LIN bus line input/output
7	VS	Supply voltage
8	VCC	Output voltage regulator 3.3V/5V/85mA
Backside[1]		Heat slug, internally connected to the GND pin

Note: 1. Only for the DFN8 package.

3. Pin Description

3.1 Supply Pin (VS)

LIN operating voltage is V_S = 5V to 28V. Undervoltage detection is implemented to disable transmission if V_S falls below typ. 4.5V, thereby avoiding false bus messages. After switching on V_S, the IC starts in fail-safe mode and the voltage regulator is switched on.

The supply current in sleep mode is typically 9µA and 47µA in silent mode.

3.2 Ground Pin (GND)

The IC does not affect the LIN bus in the event of GND disconnection. It is able to handle a ground shift of up to 11.5% of V_S.

3.3 Voltage Regulator Output Pin (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 85mA, supplying the microcontroller and other ICs on the PCB and is protected against overload by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and causes a reset signal at the NRES output pin if it drops below a defined threshold $V_{VCC\_th\_uv\_down}$.

3.4 Undervoltage Reset Output (NRES)

If the V_{CC} voltage falls below the undervoltage detection threshold $V_{CC\_th\_uv\_down}$, NRES switches to low after t_{res_f}. The NRES stays low even if V_{CC} = 0V because NRES is internally driven from the V_S voltage. If V_S voltage ramps down, NRES stays low until V_S < 1.5V and then becomes highly impedant.

The implemented undervoltage delay keeps NRES low for t_{Reset} = 4ms after V_{CC} reaches its nominal value.

3.5 Bus Pin (LIN) (SBC only)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.x is implemented. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to V_S, even in the event of a GND shift or V_{Bat} disconnection. The LIN receiver thresholds comply with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope-controlled.

During a short circuit at LIN to V_{Bat}, the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. The V_{CC} regulator works independently during LIN overtemperature switch-off.

During a short circuit from LIN to GND the IC can be switched into sleep or silent mode and even in this case the current consumption is lower than 100µA in sleep mode and lower than 120µA in silent mode. If the short-circuit disappears, the IC starts with a remote wake-up.

The reverse current is < 2µA at pin LIN during loss of V_{Bat}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.

3.6 Input/Output (TXD) (SBC only)

In normal mode the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state. If the TXD pin stays at GND level while switching into normal mode, it must be pulled to high level longer than 10µs before the LIN driver can be activated. This feature prevents the bus line from being accidentally driven to dominant state after normal mode has been activated (also in case of a short circuit at TXD to GND). During fail-safe mode, this pin is used as output and signals the fail-safe source.

The TXD input has an internal pull-up resistor.

An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{dom} > 20ms, the LIN bus driver is switched to the recessive state. Nevertheless, when switching to sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (> 10µs).

3.7 Output Pin (RXD) (SBC only)

In normal mode this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD; LIN low (dominant state) is indicated by a low level at RXD.

The output is a push-pull stage switching between VCC and GND. The AC characteristics are measured by an external load capacitor of 20pF.

In silent mode the RXD output switches to high.

3.8 Enable Input Pin (EN) (SBC only)

The enable input pin controls the operating mode of the device. If EN is high, the circuit is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V/5V/85mA output capability.

If EN is switched to low while TXD is still high, the device is forced to silent mode. No data transmission is then possible, and current consumption is reduced to $I_{VSsilent}$ typ. 47µA. The VCC regulator retains its full functionality.

If EN is switched to low while TXD is low, the device is forced to sleep mode. No data transmission is possible, and the voltage regulator is switched off.

The EN pin provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.

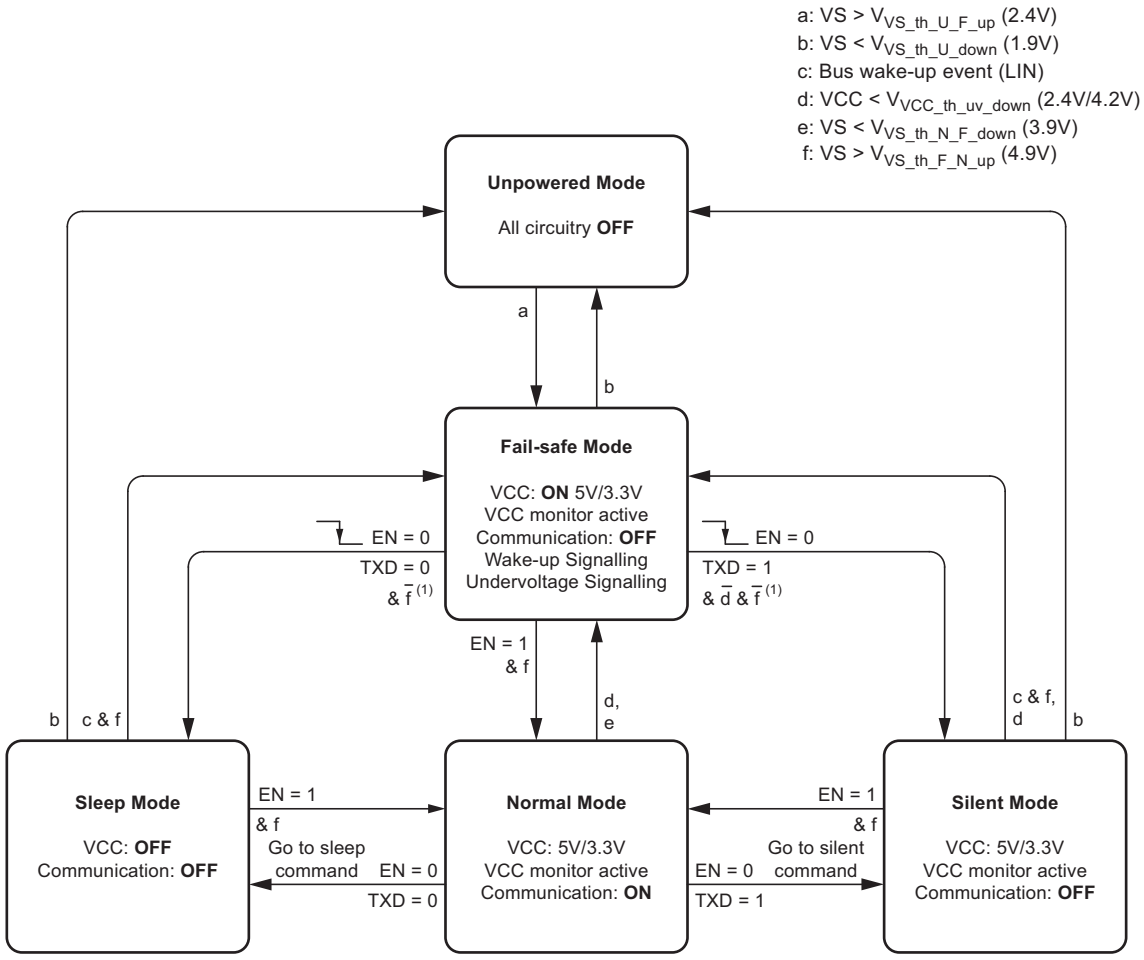
4. Functional Description

4.1 Physical Layer Compatibility

Because the LIN physical layer is independent of higher LIN layers (e.g., LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes based on earlier versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

4.2 Operating Modes

Figure 4-1. SBC Operating Modes

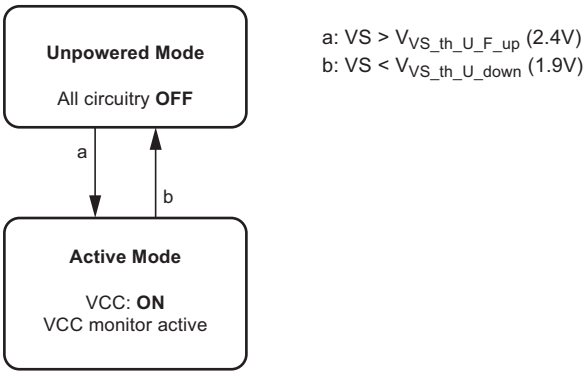


Note: 1. Condition $\bar{f}$ is valid for VS ramp up; at VS ramp down condition e is valid instead of $\bar{f}$.

Table 4-1. SBC (ATA663254, ATA663231) Operating Modes

Operating Mode	Transceiver	V_{CC} (SBC only)	LIN	TXD	RXD
Fail-safe	OFF	3.3V/5V	Recessive	Signaling fail-safe sources (see Table 4-2)	
Normal	ON	3.3V/5V	TXD-dependent	Follows data transmission	
Silent (SBC only)	OFF	3.3V/5V	Recessive	High	High
Sleep/Unpowered	OFF	0V	Recessive	Low	Low

Figure 4-2. Voltage Regulator Operating Modes



4.2.1 Normal Mode (SBC only)

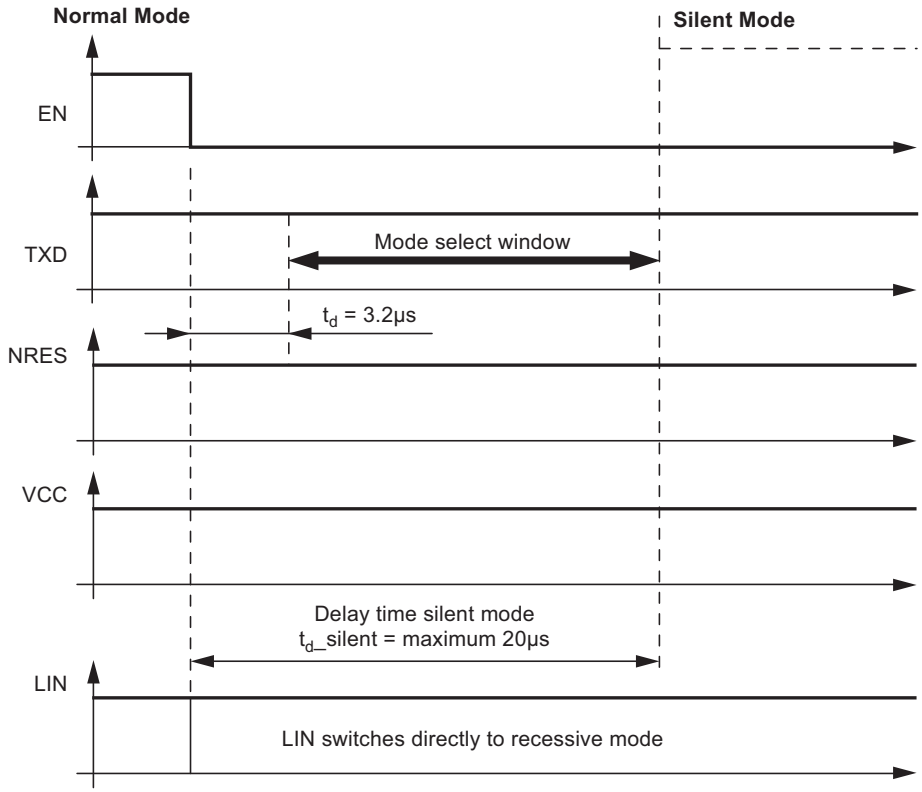
This is the normal transmitting and receiving mode of the LIN Interface, in accordance with LIN specification 2.x.

The VCC voltage regulator operates with 3.3V/5V output voltage, with a low tolerance of ±2% and a maximum output current of 85mA. If an undervoltage condition occurs, NRES is switched to low and the IC changes its state to fail-safe mode.

4.2.2 Silent Mode (SBC only)

A falling edge at EN while TXD is high switches the IC into silent mode. The TXD signal has to be logic high during the mode select window. The transmission path is disabled in silent mode. The voltage regulator is active. The overall supply current from V_{Bat} is a combination of the $I_{VSsilent}$ = 47µA plus the V_{CC} regulator output current I_{VCC}.

Figure 4-3. Switching to Silent Mode



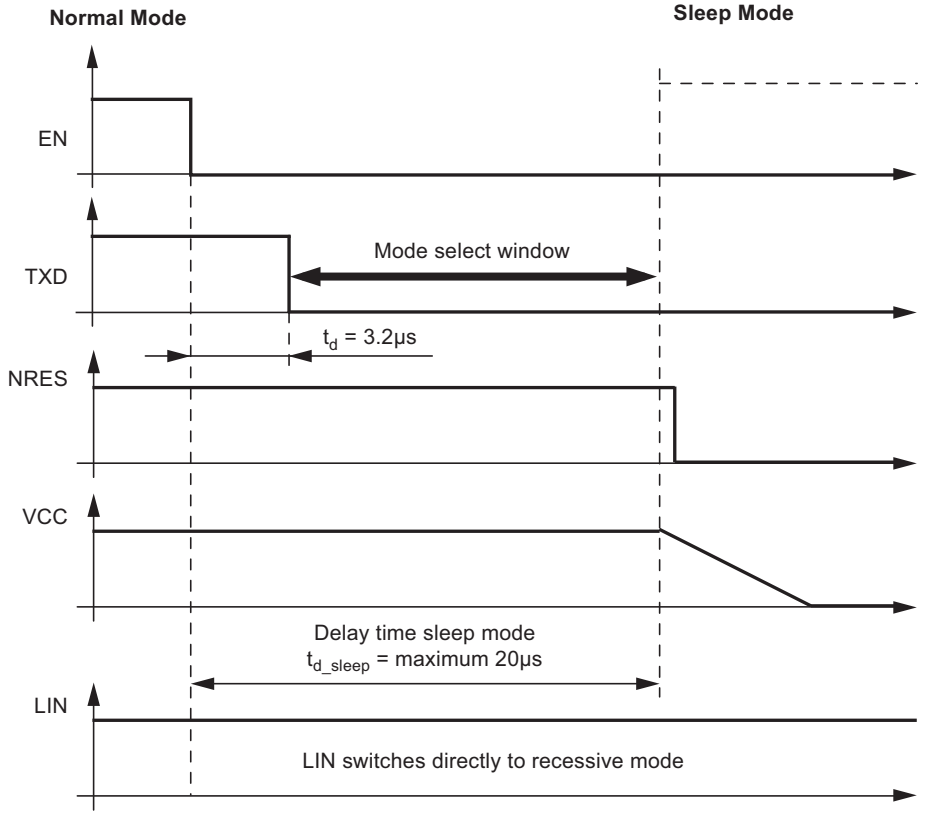
In silent mode the internal slave termination between the LIN pin and VS pin is disabled to minimize the current consumption in case the pin LIN is short-circuited to GND. Only a weak pull-up current (typically 10µA) between the LIN pin and VS pin is present. Silent mode can be activated independently from the current level on pin LIN.

If an undervoltage condition occurs, NRES is switched to low and the Atmel® SBC changes its state to fail-safe mode.

4.2.3 Sleep Mode (SBC only)

A falling edge at EN while TXD is low switches the IC into sleep mode. The TXD signal has to be logic low during the mode select window (Figure 4-6).

Figure 4-4. Switching to Sleep Mode



In order to avoid any influence to the LIN pin when switching into sleep mode it is possible to switch the EN up to 3.2µs earlier to low than the TXD. The easiest and best way to do this is by having two falling edges at TXD and EN at the same time.

In sleep mode the transmission path is disabled. Supply current from V_{Bat} is typically $I_{VSsleep}$ = 9µA. The V_{CC} regulator is switched off; NRES and RXD are low. The internal slave termination between the LIN pin and VS pin is disabled to minimize the current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10µA) between the LIN pin and the VS pin is present. The sleep mode can be activated independently from the current level on the LIN pin. Voltage below the LIN pre-wake detection V_{LINL} at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

If the TXD pin is short-circuited to GND, it is possible to switch to sleep mode via EN after $t > t_{dom}$.

4.2.4 Fail-Safe Mode (SBC only)

The device automatically switches to fail-safe mode at system power-up. The voltage regulator is switched on. The NRES output remains low for t_{res} = 4ms and causes the microcontroller to be reseted. LIN communication is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to normal mode. A low at NRES switches the IC into fail-safe mode directly. During fail-safe mode the TXD pin is an output and, together with the RXD output pin, signals the fail-safe source.

If the device enters fail-safe mode coming from the normal mode (EN=1) due to an V_S undervoltage condition ($V_S < V_{VS\_th\_N\_F\_down}$), it is possible to switch into sleep or silent mode by a falling edge at the EN input. With this feature the current consumption can be further reduced.

A wake-up event from either silent or sleep mode is signalled to the microcontroller using the RXD pin and the TXD pin. A V_S undervoltage condition is also signalled at these two pins. The coding is shown in the table below.

A wake-up event switches the IC to fail-safe mode.

Table 4-2. Signaling in Fail-safe Mode

Fail-Safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
VS_{th} (battery) undervoltage detection (VS < 3.9V)	High	Low

4.2.5 Active Mode (Voltage Regulator only)

The device automatically switches to active mode at system power-up. The VCC voltage regulator operates with 3.3V/5V output voltage, with a low tolerance of ±2% and a maximum output current of 85mA. The NRES output remains low for t_{res} = 4ms and causes the microcontroller to be reseted. The current consumption is typically 47µA.

If an undervoltage condition occurs, NRES switches to low.

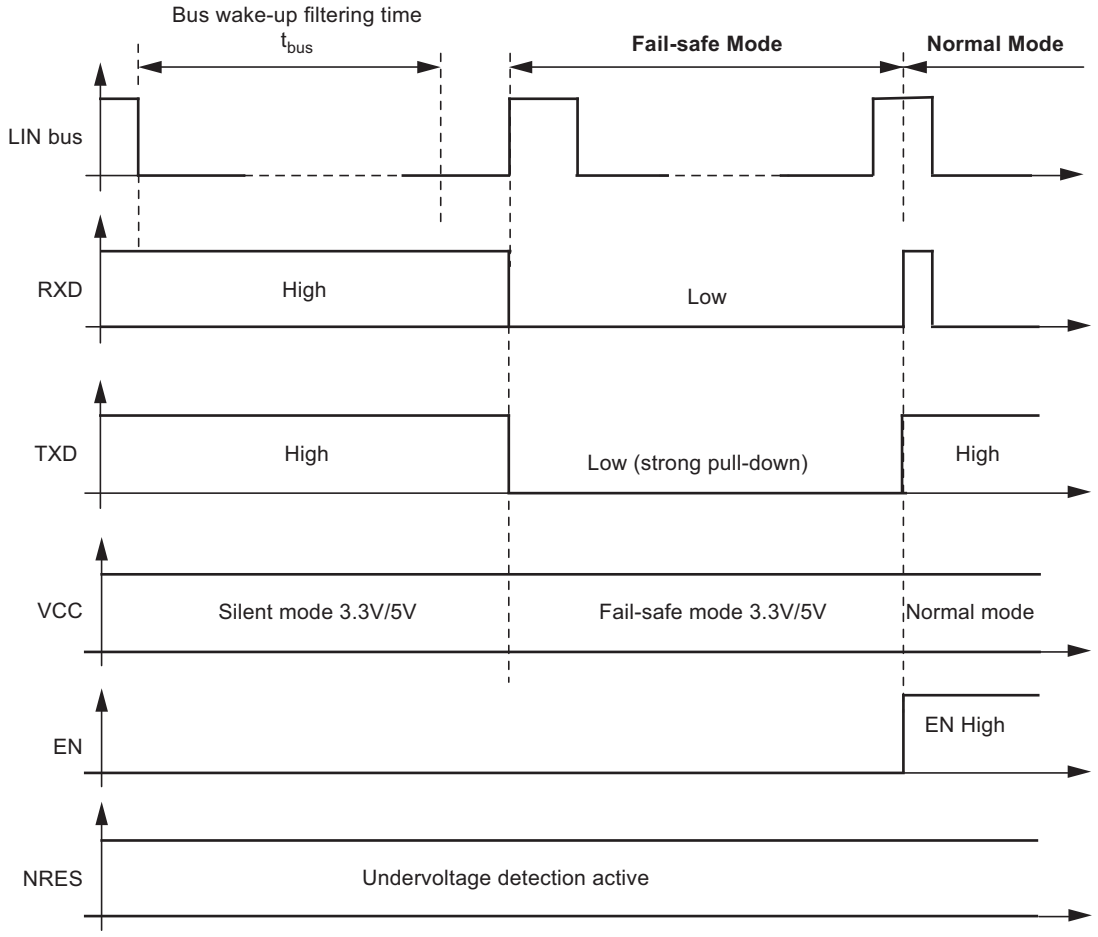
4.3 Wake-up Scenarios from Silent Mode or Sleep Mode

4.3.1 Remote Wake-up via LIN Bus

4.3.1.1 Remote Wake-up from Silent Mode (SBC only)

A remote wake-up from silent mode is only possible if TXD is high. A voltage less than the LIN pre-wake detection VLINL at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer. A falling edge at the LIN pin followed by a dominant bus level maintained for a certain period of time (> t_{bus}) and the following rising edge at pin LIN (see Figure 4-5) result in a remote wake-up request. The device switches from silent mode to fail-safe mode, the VCC voltage regulator remains activated and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD pin and TXD pin (strong pull-down at TXD). EN high can be used to switch directly to normal mode.

Figure 4-5. LIN Wake-up from Silent Mode



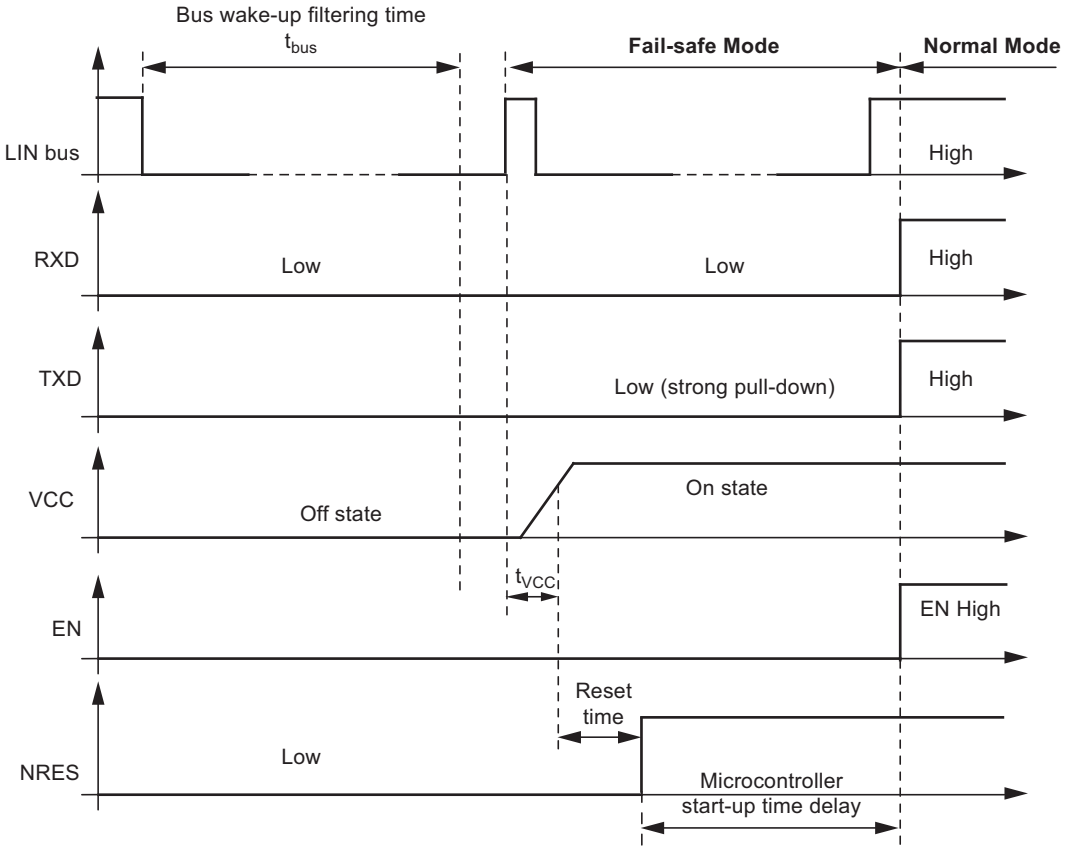
4.3.1.2 Remote Wake-up from Sleep Mode (SBC only)

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain period of time (> t_{bus}) and a following rising edge at the LIN pin result in a remote wake-up request, causing the device to switch from sleep mode to fail-safe mode.

The V_{CC} regulator is activated, and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at RXD and TXD (strong pull-down at TXD) (see Figure 4-6).

EN high can be used to switch directly from sleep/silent mode to fail-safe mode. If EN is still high after VCC ramp-up and undervoltage reset time, the IC switches to normal mode.

Figure 4-6. LIN Wake-up from Sleep Mode



4.3.2 Wake-up Source Recognition (SBC only)

The device can distinguish between different wake-up sources. The wake-up source can be read on the TXD and RXD pin in fail-safe mode. These flags are immediately reset if the microcontroller sets the EN pin to high and the IC is in normal mode.

Table 4-3. Signaling in Fail-safe Mode

Fail-Safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
VS_{th} (battery) undervoltage detection (VS < 3.9V)	High	Low

4.4 Behavior under Low Supply Voltage Condition

After the battery voltage has been connected to the application circuit, the voltage at the VS pin increases according to the block capacitor used in the application (see Figure 9-1 on page 25). If V_{VS} is higher than the minimum VS operation threshold $V_{VS\_th\_U\_F\_up}$, the IC mode changes from unpowered mode to fail-safe mode. As soon as V_{VS} exceeds the undervoltage threshold $V_{VS\_th\_F\_N\_up}$, the LIN transceiver can be activated.

The VCC output voltage reaches its nominal value after t_{VCC}. This parameter depends on the externally applied VCC capacitor and the load. The NRES output is low for the reset time delay t_{reset}. No mode change is possible during this time t_{reset}.

The behavior of VCC, NRES and VS is shown in the following diagrams (ramp-up and ramp-down):

Figure 4-7. VCC and NRES versus VS (Ramp-up) for 3.3V (SBC and Voltage Regulator)

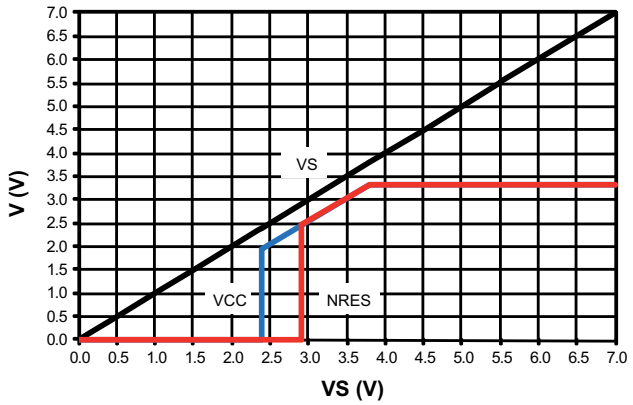


Figure 4-8. VCC and NRES versus VS (Ramp-down) for 3.3V (SBC and Voltage Regulator)

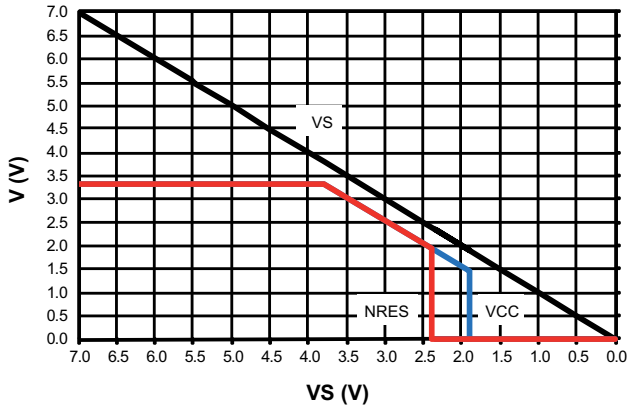


Figure 4-9. VCC and NRES versus VS (Ramp-up) for 5V (SBC and Voltage Regulator)

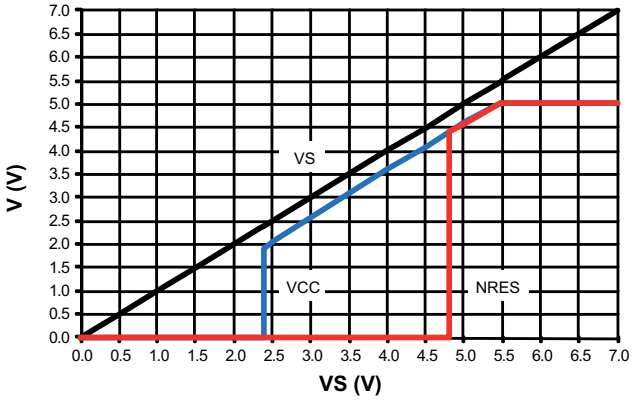
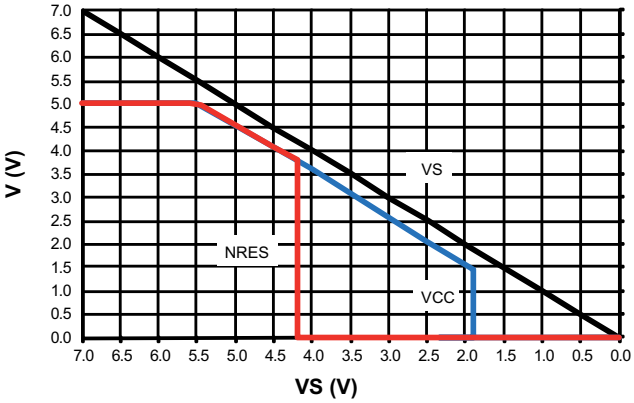


Figure 4-10. VCC and NRES versus VS (Ramp-down) for 5V (SBC and Voltage Regulator)



Please note that the upper graphs are only valid if the VS ramp-up and ramp-down times are much slower than the VCC ramp-up time t_{Vcc} and the NRES delay time t_{reset}.

If during **sleep mode** the voltage level of V_{VS} drops below the undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typ. 4.3V), the operation mode is not changed and no wake-up is possible. Only if the supply voltage on pin VS drops below the VS operation threshold $V_{VS\_th\_U\_down}$ (typ. 2.05V), does the IC switch to unpowered mode.

If during **silent mode** the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$ the IC switches into fail-safe mode. If the supply voltage on pin VS drops below the VS operation threshold $V_{VS\_th\_U\_down}$ (typ. 2.05V), does the IC switch to unpowered mode.

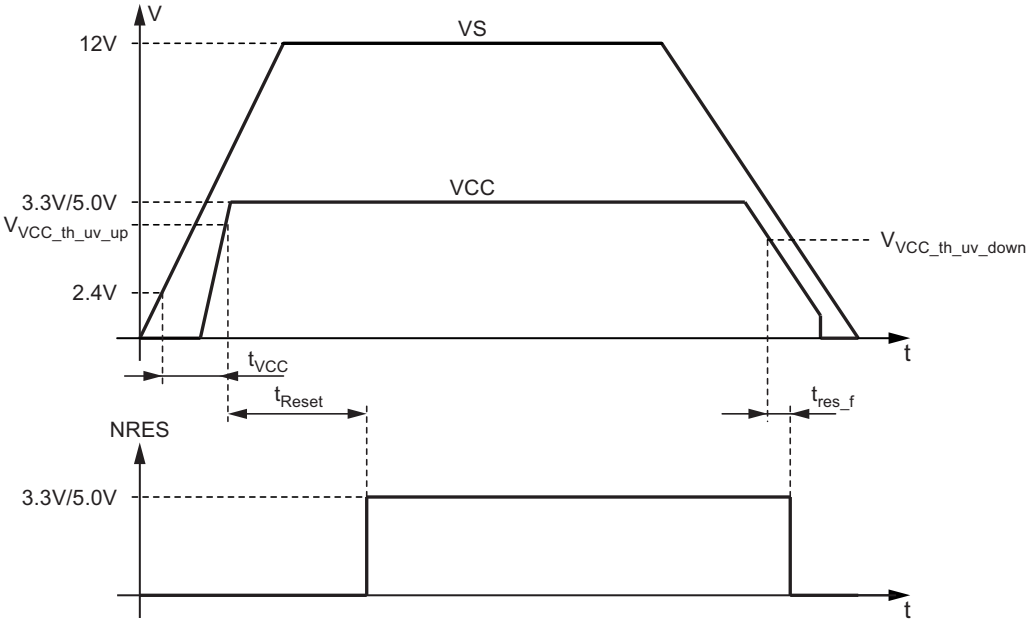
If during **normal mode** the voltage level on the VS pin drops below the VS undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typ. 4.3V), the IC switches to fail-safe mode. This means the LIN transceiver is disabled in order to avoid malfunctions or false bus messages. The voltage regulator remains active.

> **For 3.3V SBC**: In this undervoltage situation it is possible to switch the device into sleep mode or silent mode by a falling edge at the EN input. For this feature, switching into these two current saving modes is always guaranteed, allowing current consumption to be reduced even further.
>
> When the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$ (typ. 2.6V) the IC switches into fail-safe mode.
>
> **For 5V SBC**: Because of the VCC undervoltage condition in this situation, the IC is in fail-safe mode and can be switched into sleep mode only.
>
> Only when the supply voltage V_{VS} drops below the operation threshold $V_{VS\_th\_U\_down}$ (typ. 2.05V) does the IC switch into unpowered mode.

The current consumption of the SBC in silent mode or in fail-safe mode and the voltage regulator is always below 170µA, even when the supply voltage VS is lower than the regulator's nominal output voltage VCC.

4.5 Voltage Regulator

Figure 4-11. Voltage Regulator: Supply Voltage Ramp-up and Ramp-down



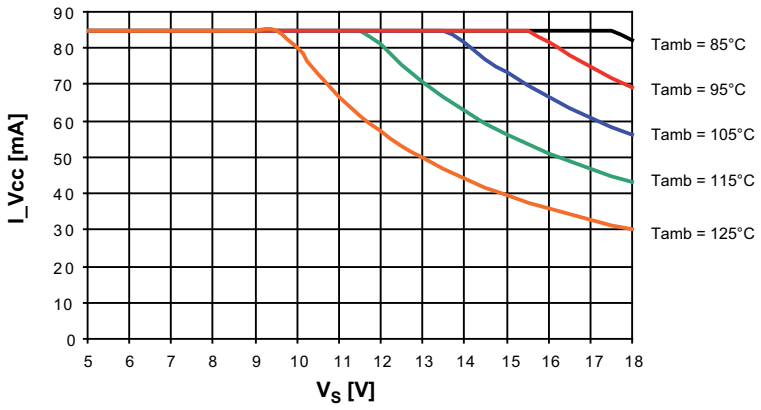
The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use a MLC capacitor with a minimum capacitance of 1.8µF together with a 100nF ceramic capacitor. Depending on the application, the values of these capacitors can be modified by the customer.

During a short circuit at VCC, the output limits the output current to I_{VCClim}. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. If the chip temperature exceeds the value T_{VCCoff}, the VCC output switches off. The chip cools down and, after a hysteresis of T_{hys}, switches the output on again.

When the Atmel® ATA6632xx in the DFN8 package is being soldered onto the PCB it is mandatory to connect the heat slug with a wide GND plate on the printed board to get a good heat sink.

The main power dissipation of the IC is created from the VCC output current IVCC, which is needed for the application. Figure 4-12 shows the safe operating area of the ATA6632xx in the DFN8 package.

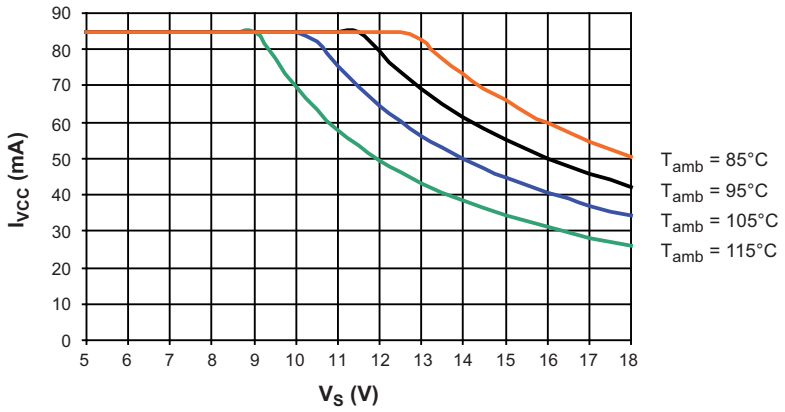
Figure 4-12. DFN8 Package Power Dissipation: Safe Operating Area: Regulator's Output Current I_{VCC} versus Supply Voltage V_S at Different Ambient Temperatures (R_{thja} = 50K/W assumed)



When the Atmel® ATA663254 in its special SO8 package (fused lead frame to pin 5) is being soldered on to the PCB, it is mandatory to connect pin 5 with a wide GND plate on the printed board to get a good heat sink.

Figure 4-13 shows the safe operating area of the Atmel ATA663254 in the SO8 package.

Figure 4-13. SO8 Package Power Dissipation: Safe Operating Area: Regulator's Output Current I_{VCC} versus Supply Voltage V_S at Different Ambient Temperatures (R_{thja} = 80K/W assumed)



5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_S	V_S	–0.3		+40	V
Pulse time ≤ 500ms T_a = 25°C Output current I_{VCC} ≤ 85mA	V_S			+43.5	V
Pulse time ≤ 2min T_a = 25°C Output current I_{VCC} ≤ 85mA	V_S			28	V
Logic pins voltage levels (RxD, TxD, EN, NRES)	V_{Logic}	–0.3		+5.5	V
Logic pins output DC currents	I_{Logic}	–5		+5	mA
LIN - DC voltage - Pulse time < 500ms	V_{LIN}	–27		+40 +43.5	V V
V_{CC} - DC voltage - DC input current	V_{VCC} I_{VCC}	–0.3		+5.5 +200	V mA
ESD according to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2 - Pin VS, LIN to GND (with external circuitry acc. applications diagram)		±6			kV
ESD HBM following STM5.1 with 1.5kΩ/100pF - Pin VS, LIN to GND		±6			kV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		±3			kV
CDM ESD STM 5.3.1		±750			V
Machine Model ESD AEC-Q100-RevF(003)		±200			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C

6. Thermal Characteristics DFN8

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to heat slug	R_{thjC}		10		K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB according to JEDEC	R_{thja}		50		K/W
Thermal shutdown of V_{CC} regulator	T_{VCCoff}	150	165	180	°C
Thermal shutdown of LIN output	T_{LINoff}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}		10		°C

7. Thermal Characteristics SO8

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to ambient with a heat sink at GND (pin 5) on PCB (fused lead frame to pin 5)	R_{thJA}		80		K/W
Thermal shutdown of V_{CC} regulator	T_{VCCoff}	150	165	180	°C
Thermal shutdown of LIN output	T_{LINoff}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}		10		°C

8. Electrical Characteristics

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	VS pin								
1.1	Nominal DC voltage range		VS	V_S	5	13.5	28	V	A
1.2	Supply current in sleep mode	Sleep mode V_{LIN} > V_S – 0.5V V_S < 14V, T = 27°C	VS	$I_{VSsleep}$	6	9	12	µA	B
		Sleep mode V_{LIN} > V_S – 0.5V V_S < 14V	VS	$I_{VSsleep}$	3	10	15	µA	A
		Sleep mode, V_{LIN} = 0V bus shorted to GND V_S < 14V	VS	$I_{VSsleep\_short}$	20	50	100	µA	A
1.3	Supply current in silent mode (SBC) / Active mode (voltage regulator)	Bus recessive 5.5V< V_S < 14V without load at VCC T = 27°C	VS	$I_{VSsilent}$	30	47	58	µA	B
		Bus recessive 5.5V< V_S < 14V without load at VCC	VS	$I_{VSsilent}$	30	50	64	µA	A
		Bus recessive 2.0V< V_S < 5,5V without load at VCC	VS	$I_{VSsilent}$	50	130	170	µA	A
		Silent mode 5.5V< V_S < 14V bus shorted to GND without load at VCC	VS	$I_{VSsilent\_short}$	50	80	120	µA	A
1.4	Supply current in normal mode	Bus recessive V_S < 14V without load at VCC	VS	I_{VSrec}	150	230	290	µA	A
1.5	Supply current in normal mode	Bus dominant (internal LIN pull-up resistor active) V_S < 14V without load at VCC	VS	I_{VSdom}	200	700	950	µA	A
1.6	Supply current in fail-safe mode	Bus recessive 5.5V < V_S < 14V without load at VCC	VS	I_{VSfail}	40	55	80	µA	A
		Bus recessive 2.0V < V_S < 5.5V without load at VCC	VS	I_{VSfail}	50	130	170	µA	A
1.7	VS undervoltage threshold (switching from normal to fail-safe mode)	Decreasing supply voltage	VS	$V_{VS\_th\_N\_F\_down}$	3.9	4.3	4.7	V	A
		Increasing supply voltage	VS	$V_{VS\_th\_F\_N\_up}$	4.1	4.6	4.9	V	A
1.8	VS undervoltage hysteresis		VS	$V_{VS\_hys\_F\_N}$	0.1	0.25	0.4	V	A
1.9	VS operation threshold (switching to unpowered mode)	Switch to unpowered mode	VS	$V_{VS\_th\_U\_down}$	1.9	2.05	2.3	V	A
		Switch from unpowered to fail-safe mode	VS	$V_{VS\_th\_U\_F\_up}$	2.0	2.25	2.4	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.10	VS undervoltage hysteresis		VS	$V_{VS\_hys\_U}$	0.1	0.2	0.3	V	A
2	RXD output pin (only SBC)								
2.1	Low-level output sink capability	Normal mode, V_{LIN} = 0V, I_{RXD} = 2mA	RXD	V_{RXDL}		0.2	0.4	V	A
2.2	High-level output source capability	Normal mode V_{LIN} = V_S, I_{RXD} = –2mA	RXD	V_{RXDH}	V_{CC} – 0.4V	V_{CC} – 0.2V		V	A
3	TXD input/output pin (only SBC)								
3.1	Low-level voltage input		TXD	V_{TXDL}	–0.3		+0.8	V	A
3.2	High-level voltage input		TXD	V_{TXDH}	2		V_{CC} + 0.3V	V	A
3.3	Pull-up resistor	V_{TXD} = 0V	TXD	R_{TXD}	40	70	100	kΩ	A
3.4	High-level leakage current	V_{TXD} = V_{CC}	TXD	I_{TXD}	–3		+3	µA	A
3.7	Low-level output sink current at LIN wake-up request	Fail-safe Mode V_{LIN} = V_S V_{TXD} = 0.4V	TXD	I_{TXD}	2	2.5	8	mA	A
4	EN input pin (only SBC)								
4.1	Low-level voltage input		EN	V_{ENL}	–0.3		+0.8	V	A
4.2	High-level voltage input		EN	V_{ENH}	2		V_{CC} + 0.3V	V	A
4.3	Pull-down resistor	V_{EN} = VCC	EN	R_{EN}	50	125	200	kΩ	A
4.4	Low-level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A
5	NRES open drain output pin								
5.1	Low-level output voltage	V_S ≥ 5.5V I_{NRES} = 2mA	NRES	V_{NRESL}		0.2	0.4	V	A
5.2	Undervoltage reset time	V_{VS} ≥ 5.5V C_{NRES} = 20pF	NRES	t_{Reset}	2	4	6	ms	A
5.3	Reset debounce time for falling edge	V_{VS} ≥ 5.5V C_{NRES} = 20pF	NRES	t_{res_f}	0.5		10	µs	A
5.4	Switch off leakage current	V_{NRES} = 5.5V	NRES	I_{NRES_L}	–3		+3	µA	A
8	VCC voltage regulator (3.3V)								
8.1	Output voltage VCC	4V < V_S < 18V (0mA to 50mA)	VCC	VCC_{nor}	3.234		3.366	V	A
		4.5V < V_S < 18V (0mA to 85mA)	VCC	VCC_{nor}	3.234		3.366	V	C
8.2	Output voltage V_{CC} at low V_S	3V < VS < 4V	VCC	VCC_{low}	V_{VS} – V_D		3.366	V	A
8.3	Regulator drop voltage	VS > 3V, I_{VCC} = –15mA	VCC	V_{D1}		100	150	mV	A
8.4	Regulator drop voltage	VS > 3V, I_{VCC} = –50mA	VCC	V_{D2}		300	500	mV	A
8.5	Line regulation maximum	4V < VS < 18V	VCC	VCC_{line}		0.1	0.2	%	A
8.6	Load regulation maximum	5mA < I_{VCC} < 50mA	VCC	VCC_{load}		0.1	0.5	%	A
8.7	Output current limitation	VS > 4V	VCC	I_{VCClim}		–180	–120	mA	A
8.8	Load capacity	MLC capacitor	VCC	C_{load}	1.8	2.2		µF	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.9	VCC undervoltage threshold (NRES ON)	Referred to VCC VS > 4V	VCC	$V_{VCC\_th\_uv\_down}$	2.3	2.5	2.8	V	A
	VCC undervoltage threshold (NRES OFF)	Referred to VCC VS > 4V	VCC	$V_{VCC\_th\_uv\_up}$	2.5	2.6	2.9	V	A
8.10	Hysteresis of VCC undervoltage threshold	Referred to VCC VS > 4V	VCC	$V_{VCC\_hys\_uv}$	100	200	300	mV	A
8.11	Ramp-up time VS > 4V to VCC = 3.3V	C_{VCC} = 2.2µF I_{load} = –5mA at VCC	VCC	t_{VCC}		1	1.5	ms	A
9	VCC voltage regulator (5V)								
9.1	Output voltage VCC	5.5V < V_S < 18V (0mA to 50mA)	VCC	VCC_{nor}	4.9		5.1	V	A
		6V < V_S < 18V (0mA to 85mA)	VCC	VCC_{nor}	4.9		5.1	V	C
9.2	Output voltage V_{CC} at low V_S	4V < VS < 5.5V	VCC	VCC_{low}	$V_{VS} – V_D$		5.1	V	A
9.3	Regulator drop voltage	VS > 4V, I_{VCC} = –20mA	VCC	V_{D1}		100	200	mV	A
9.4	Regulator drop voltage	VS > 4V, I_{VCC} = –50mA	VCC	V_{D2}		300	500	mV	A
9.5	Regulator drop voltage	VS > 3.3V, I_{VCC} = –15mA	VCC	V_{D3}			150	mV	A
9.6	Line regulation maximum	5.5V < VS < 18V	VCC	VCC_{line}		0.1	0.2	%	A
9.7	Load regulation maximum	5mA < I_{VCC} < 50mA	VCC	VCC_{load}		0.1	0.5	%	A
9.8	Output current limitation	VS > 5.5V	VCC	I_{VCClim}		–180	–120	mA	A
9.9	Load capacity	MLC capacitor	VCC	C_{load}	1.8	2.2		µF	D
9.10	VCC undervoltage threshold (NRES ON)	Referred to VCC VS > 4V	VCC	$V_{VCC\_th\_uv\_down}$	4.2	4.4	4.6	V	A
	VCC undervoltage threshold (NRES OFF)	Referred to VCC VS > 4V	VCC	$V_{VCC\_th\_uv\_up}$	4.3	4.6	4.8	V	A
9.11	Hysteresis of undervoltage threshold	Referred to VCC VS > 5.5V	VCC	$V_{VCC\_hys\_uv}$	100	200	300	mV	A
9.12	Ramp-up time VS > 5.5V to VCC = 5V	C_{VCC} = 2.2µF I_{load} = –5mA at VCC	VCC	t_{VCC}		1	1.5	ms	A
10	LIN bus driver (only SBC): bus load conditions: Load 1 (small): 1nF, 1kΩ; Load 2 (large): 10nF, 500Ω; C_{RXD} = 20pF, Load 3 (medium): 6.8nF, 660Ω characterized on samples 12.7 and 12.8 specifies the timing parameters for proper operation at 20kb/s and 12.9 and 12.10 at 10.4kb/s								
10.1	Driver recessive output voltage	Load1/Load2	LIN	V_{BUSrec}	$0.9 \times V_S$		V_S	V	A
10.2	Driver dominant voltage	V_{VS} = 7V R_{load} = 500Ω	LIN	$V_{\_LoSUP}$			1.2	V	A
10.3	Driver dominant voltage	V_{VS} = 18V R_{load} = 500Ω	LIN	$V_{\_HiSUP}$			2	V	A
10.4	Driver dominant voltage	V_{VS} = 7V R_{load} = 1000Ω	LIN	$V_{\_LoSUP\_1k}$	0.6			V	A
10.5	Driver dominant voltage	V_{VS} = 18V R_{load} = 1000Ω	LIN	$V_{\_HiSUP\_1k}$	0.8			V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.6	Pull-up resistor to V_S	The serial diode is mandatory	LIN	R_{LIN}	20	30	47	kΩ	A
10.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
10.8	LIN current limitation $V_{BUS} = V_{Bat\_max}$		LIN	I_{BUS_LIM}	40	120	200	mA	A
10.9	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current driver off V_{BUS} = 0V V_{Bat} = 12V	LIN	$I_{BUS\_PAS\_dom}$	–1	–0.35		mA	A
10.10	Leakage current LIN recessive	Driver off 8V < V_{Bat} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{Bat}$	LIN	$I_{BUS\_PAS\_rec}$		10	20	µA	A
10.11	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network	$GND_{Device} = V_S$ V_{Bat} = 12V 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	A
10.12	Leakage current at disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V_{Bat} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_bat}$		0.1	2	µA	A
10.13	Capacitance on pin LIN to GND		LIN	C_{LIN}			20	pF	D
11	LIN bus receiver (only SBC)								
11.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	LIN	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
11.2	Receiver dominant state	V_{EN} = 5V/3.3V	LIN	V_{BUSdom}	–27		0.4 × V_S	V	A
11.3	Receiver recessive state	V_{EN} = 5V/3.3V	LIN	V_{BUSrec}	0.6 × V_S		40	V	A
11.4	Receiver input hysteresis	$V_{hys} = V_{th\_rec} – V_{th\_dom}$	LIN	V_{BUShys}	0.028 × V_S	0.1 x V_S	0.175 × V_S	V	A
11.5	Pre-wake detection LIN high-level input voltage		LIN	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
11.6	Pre-wake detection LIN low-level input voltage	Activates the LIN receiver	LIN	V_{LINL}	–27		V_S – 3.3V	V	A
12	Internal timers (only SBC)								
12.1	Dominant time for wake-up via LIN bus	V_{LIN} = 0V	LIN	t_{bus}	50	100	150	µs	A
12.2	Time delay for mode change from fail-safe into normal mode via EN pin	V_{EN} = 5V/3.3V	EN	t_{norm}	5	15	20	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

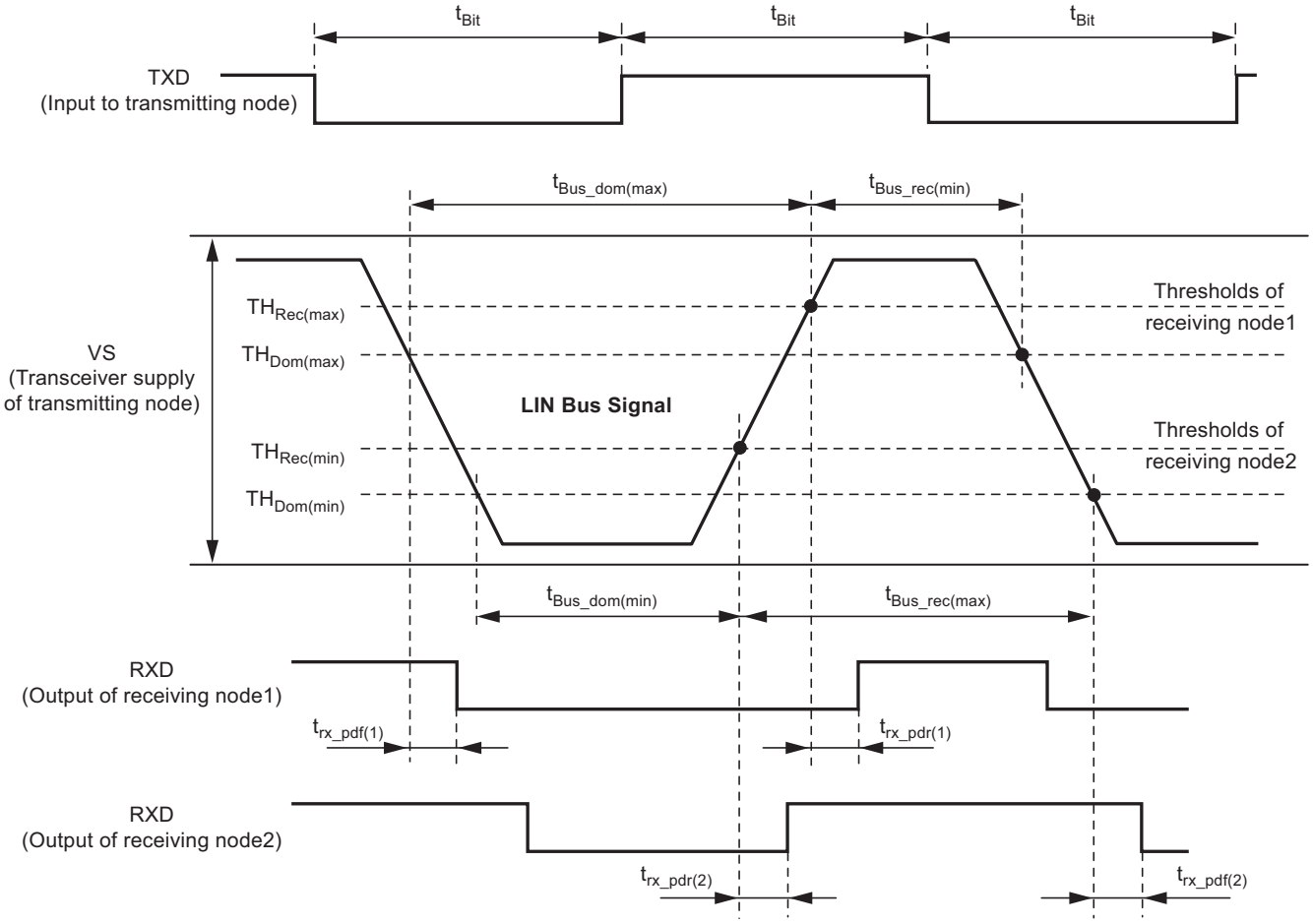
8. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
12.3	Time delay for mode change from normal mode to sleep mode via EN pin	V_{EN} = 0V	EN	t_{sleep}	5	15	20	µs	A
12.5	TXD dominant time-out time	V_{TXD} = 0V	TXD	t_{dom}	20	40	60	ms	A
12.6	Time delay for mode change from silent mode into normal mode via EN pin	V_{EN} = 5V/3.3V	EN	t_{s_n}	5	15	40	µs	A
12.7	Duty cycle 1	$TH_{Rec(max)} = 0.744 \times V_S$ $TH_{Dom(max)} = 0.581 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 50µs $D1 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D1	0.396				A
12.8	Duty cycle 2	$TH_{Rec(min)} = 0.422 \times V_S$ $TH_{Dom(min)} = 0.284 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 50µs $D2 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D2			0.581		A
12.9	Duty cycle 3	$TH_{Rec(max)} = 0.778 \times V_S$ $TH_{Dom(max)} = 0.616 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 96µs $D3 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D3	0.417				A
12.10	Duty cycle 4	$TH_{Rec(min)} = 0.389 \times V_S$ $TH_{Dom(min)} = 0.251 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 96µs $D4 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D4			0.590		A
12.11	Slope time falling and rising edge at LIN	V_S = 7.0V to 18V	LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A
13	Receiver electrical AC parameters of the LIN physical layer (only SBC) LIN receiver, RXD load conditions: C_{RXD} = 20pF								
13.1	Propagation delay of receiver	V_S = 7.0V to 18V $t_{rx\_pd} = \max(t_{rx\_pdr}, t_{rx\_pdf})$	RXD	t_{rx_pd}			6	µs	A
13.2	Symmetry of receiver propagation delay rising edge minus falling edge	V_S = 7.0V to 18V $t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$	RXD	t_{rx_sym}	–2		+2	µs	A

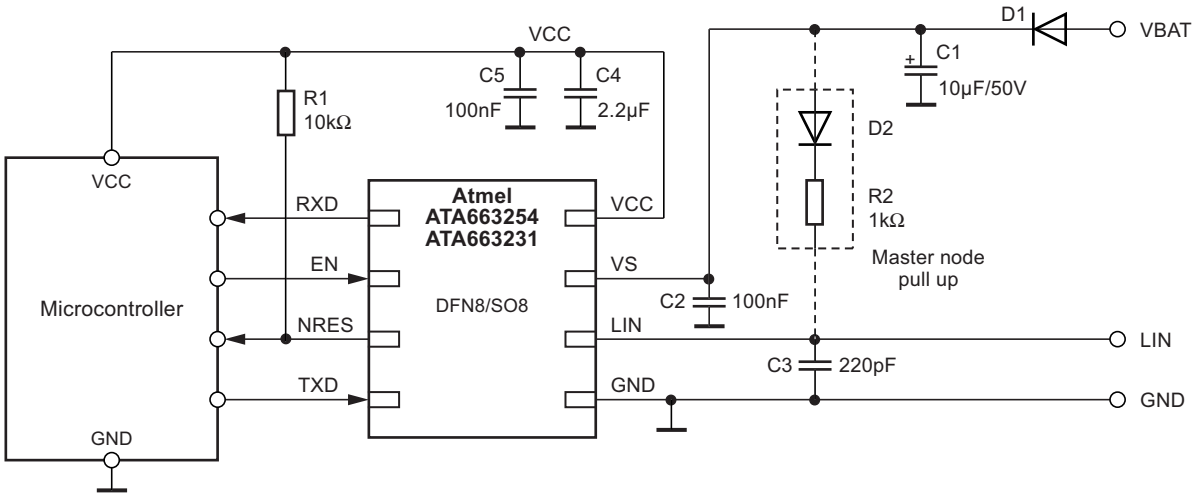
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 8-1. Definition of Bus Timing Characteristics



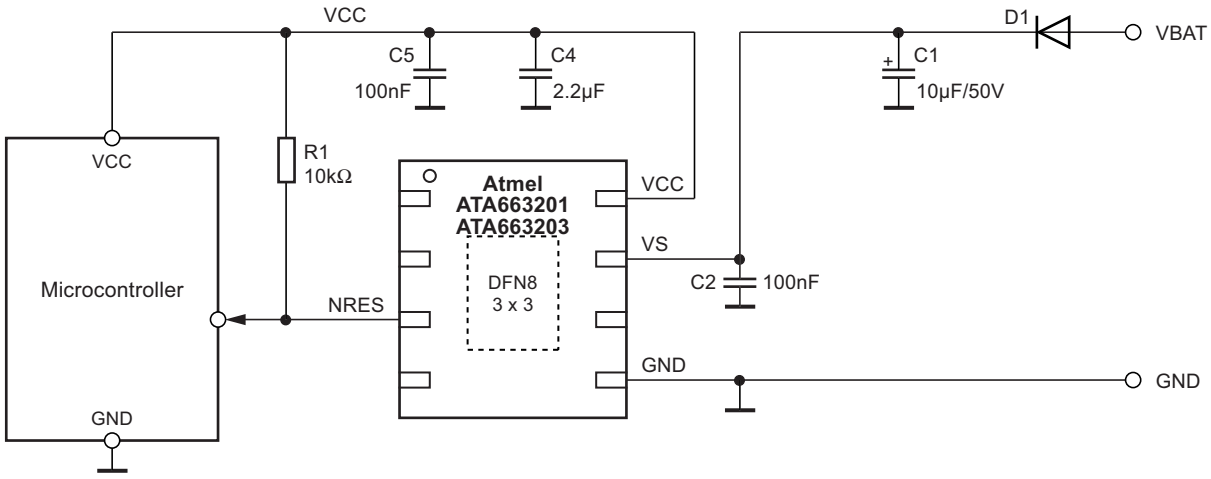
9. Application Circuits

Figure 9-1. Typical Application Circuit SBC



Note: Heat slug must always be connected to GND (for DFN8 package).

Figure 9-2. Typical Application Circuit Voltage Regulator



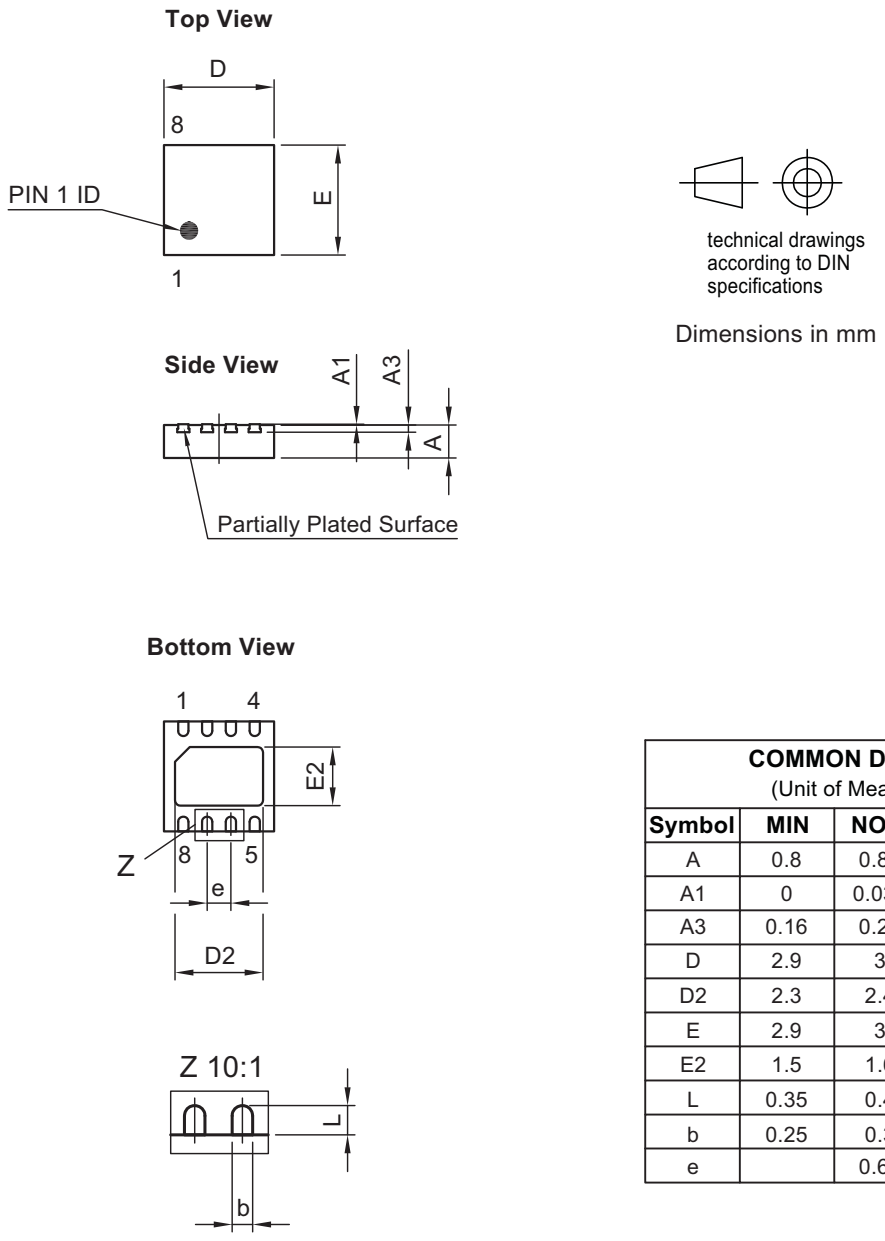
Note: Heat slug must always be connected to GND.

10. Ordering Information

Extended Type Number	Package	Remarks
ATA663231-GBQW	DFN8	3.3V LIN system basis chip, Pb-free, 6k, taped and reeled
ATA663254-GBQW	DFN8	5V LIN system basis chip, Pb-free, 6k, taped and reeled
ATA663201-GBQW	DFN8	3.3V voltage regulator, Pb-free, 6k, taped and reeled
ATA663203-GBQW	DFN8	5V voltage regulator, Pb-free, 6k, taped and reeled
ATA663254-GAQW	SO8	5V LIN system basis chip, Pb-free, 4k, taped and reeled

11. Package Information

Figure 11-1. DFN8

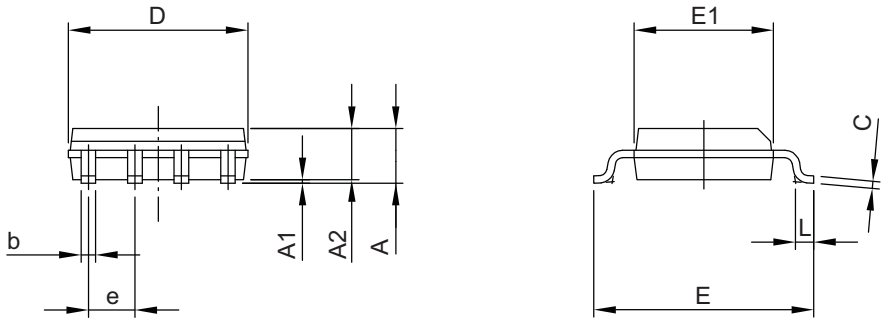


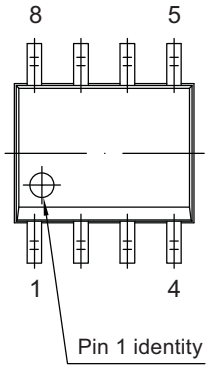
COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A3	0.16	0.21	0.26	
D	2.9	3	3.1	
D2	2.3	2.4	2.5	
E	2.9	3	3.1	
E2	1.5	1.6	1.7	
L	0.35	0.4	0.45	
b	0.25	0.3	0.35	
e		0.65		

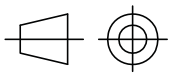
10/11/13

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Package: VDFN_3x3_8L** Exposed pad 2.4x1.6		6.543-5165.03-4	1

Figure 11-2. SO8







technical drawings
according to DIN
specifications

Dimensions in mm

COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	1.5	1.65	1.8	
A1	0.1	0.15	0.25	
A2	1.4	1.47	1.55	
D	4.8	4.9	5	
E	5.8	6	6.2	
E1	3.8	3.9	4	
L	0.4	0.65	0.9	
C	0.15	0.2	0.25	
b	0.3	0.4	0.5	
e		1.27 BSC		

05/08/14

Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**TITLE** **Package: SO8**	**GPC**	**DRAWING NO.** 6.543-5185.01-4	**REV.** 1

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9337G-AUTO-09/16	• ATA663201 3.3V voltage regulator added
9337F-AUTO-02/16	• Features on page 1 updated • Section 2 “Pin Configuration” on page 4 updated • Section 4.5 “Voltage Regulator” on pages 15 to 16 updated • Section 7 “Thermal Characteristics SO8” on page 18 added • Section 9 “Application Circuits” on page 25 updated • Section 10 “Ordering Information” on page 25 updated • Figure 11-2 “SO8” on page 27 added
9337E-AUTO-12/15	• Section 4.2 “Operating Modes” on page 7: Note 1 added below Figure 4-1 • Figure 4-11 “Voltage Regulator: Supply Voltage Ramp-up and Ramp-down” on page 15: Parameter names updated
9337D-AUTO-07/14	• Figure 1- 2 “Block Diagram Voltage Regulator” on page 3 added • ATA663203 pin configuration on page 4 added • Figure 4-3 “Voltage Regulator Operating Modes” on page 8 added • Section 4.2.5 “Active Mode (Voltage Regulator only)” on page 10 added • Figure 8-2 “Typical Application Circuit Voltage Regulator” on page 23 added • Section 9 “Ordering Information” on page 24 updated

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