

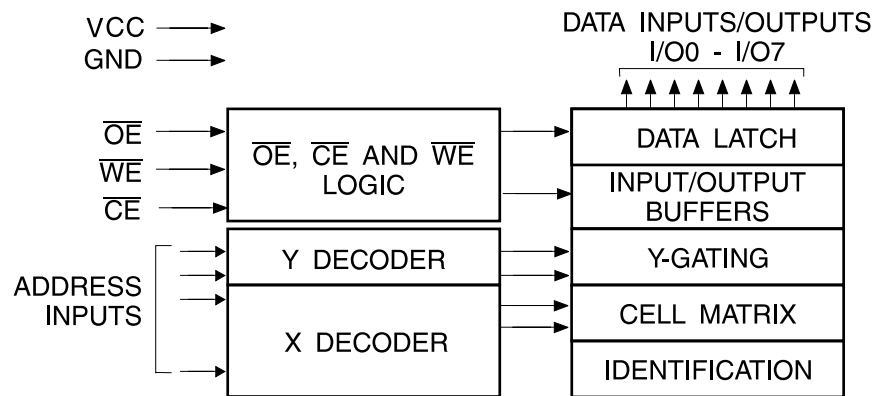
The AT28C64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/ $\overline{\text{BUSY}}$  (unless pin 1 is N.C.) and  $\overline{\text{DATA}}$  Polling of I/O<sub>7</sub>. Once the end of a write

cycle has been detected, a new access for a read or write can begin.

The CMOS technology offers fast access times of 120 ns at low power dissipation. When the chip is deselected the standby current is less than 100  $\mu\text{A}$ .

Atmel's AT28C64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of EEPROM are available for device identification or tracking.

## Block Diagram



## Absolute Maximum Ratings\*

Temperature under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground .....	-0.6V to +6.25V
All Output Voltages with Respect to Ground .....	-0.6V to $V_{\text{CC}} + 0.6\text{V}$
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground .....	-0.6V to +13.5V

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

## Device Operation

**READ:** The AT28C64 is accessed like a Static RAM. When  $\overline{CE}$  and  $\overline{OE}$  are low and  $\overline{WE}$  is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever  $\overline{CE}$  or  $\overline{OE}$  is high. This dual line control gives designers increased flexibility in preventing bus contention.

**BYTE WRITE:** Writing data into the AT28C64 is similar to writing into a Static RAM. A low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{OE}$  high and  $\overline{CE}$  or  $\overline{WE}$  low (respectively) initiates a byte write. The address location is latched on the falling edge of  $\overline{WE}$  (or  $\overline{CE}$ ); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of  $t_{WC}$ , a read operation will effectively be a polling operation.

**FAST BYTE WRITE:** The AT28C64E offers a byte write time of 200  $\mu$ s maximum. This feature allows the entire device to be rewritten in 1.6 seconds.

**READY/ $\overline{BUSY}$ :** Pin 1 is an open drain RDY/ $\overline{BUSY}$  output that can be used to detect the end of a write cycle. RDY/ $\overline{BUSY}$  is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the

same RDY/ $\overline{BUSY}$  line. The RDY/ $\overline{BUSY}$  pin is not connected for the AT28C64X.

**DATA POLLING:** The AT28C64 provides  $\overline{DATA}$  Polling to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O<sub>7</sub> (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

**WRITE PROTECTION:** Inadvertent writes to the device are protected against in the following ways: (a)  $V_{CC}$  sense – if  $V_{CC}$  is below 3.8V (typical) the write function is inhibited; (b)  $V_{CC}$  power on delay – once  $V_{CC}$  has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit – holding any one of  $\overline{OE}$  low,  $\overline{CE}$  high or  $\overline{WE}$  high inhibits byte write cycles.

**CHIP CLEAR:** The contents of the entire memory of the AT28C64 may be set to the high state by the CHIP CLEAR operation. By setting  $\overline{CE}$  low and  $\overline{OE}$  to 12 volts, the chip is cleared when a 10 msec low pulse is applied to  $\overline{WE}$ .

**DEVICE IDENTIFICATION:** An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to  $12 \pm 0.5V$  and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.



## DC and AC Operating Range

		AT28C64-12	AT28C64-15	AT28C64-20	AT28C64-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V <sub>CC</sub> Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

## Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Write <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Standby/Write Inhibit	V <sub>IH</sub>	X <sup>(1)</sup>	X	High Z
Write Inhibit	X	X	V <sub>IH</sub>	
Write Inhibit	X	V <sub>IL</sub>	X	
Output Disable	X	V <sub>IH</sub>	X	High Z
Chip Erase	V <sub>IL</sub>	V <sub>H</sub> <sup>(3)</sup>	V <sub>IL</sub>	High Z

- Notes:
1. X can be V<sub>IL</sub> or V<sub>IH</sub>.
  2. Refer to AC programming waveforms.
  3. V<sub>H</sub> = 12.0V ± 0.5V.

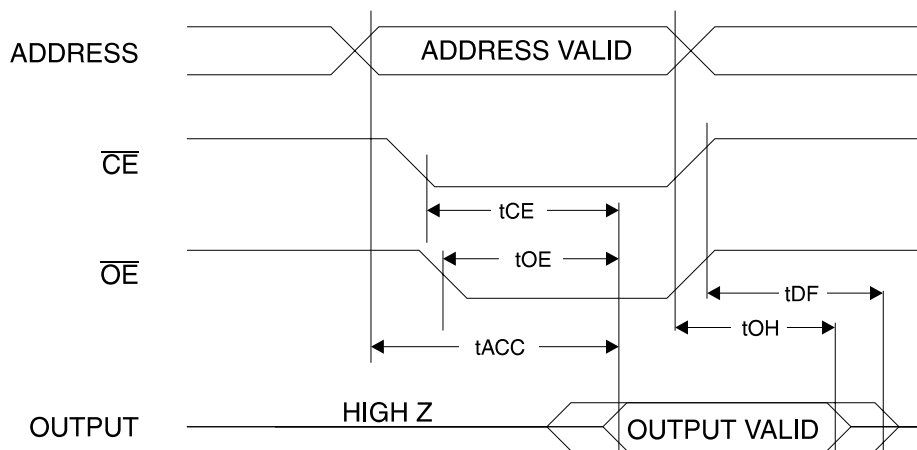
## DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> + 1V		10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to V <sub>CC</sub>		10	μA
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V <sub>CC</sub> + 1.0V		100	μA
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current TTL	$\overline{CE} = 2.0V$ to V <sub>CC</sub> + 1.0V	Com.	2	mA
			Ind.	3	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current AC	f = 5 MHz; I <sub>OUT</sub> = 0 mA $\overline{CE} = V_{IL}$	Com.	30	mA
			Ind.	45	mA
V <sub>IL</sub>	Input Low Voltage			0.8	V
V <sub>IH</sub>	Input High Voltage		2.0		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA = 4.0 mA for RDY/ $\overline{BUSY}$		0.45	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V

## AC Read Characteristics

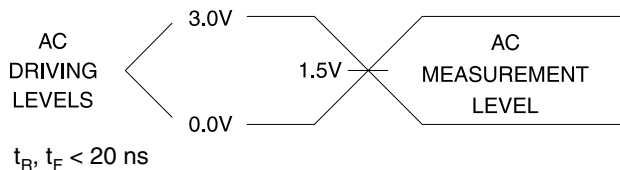
Symbol	Parameter	AT28C64-12		AT28C64-15		AT28C64-20		AT28C64-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{ACC}$	Address to Output Delay		120		150		200		250	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		120		150		200		250	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	10	60	10	70	10	80	10	100	ns
$t_{DF}^{(3)(4)}$	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	45	0	50	0	55	0	60	ns
$t_{OH}$	Output Hold from $\overline{OE}$ , $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

## AC Read Waveforms<sup>(1)(2)(3)(4)</sup>

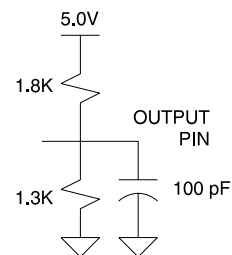


- Notes:
- $\overline{CE}$  may be delayed up to  $t_{ACC} - t_{CE}$  after the address transition without impact on  $t_{ACC}$ .
  - $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$  or by  $t_{ACC} - t_{OE}$  after an address change without impact on  $t_{ACC}$ .
  - $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$  whichever occurs first ( $C_L = 5 \text{ pF}$ ).
  - This parameter is characterized and is not 100% tested.

## Input Test Waveforms and Measurement Level



## Output Test Load



## Pin Capacitance

$f = 1 \text{ MHz}$ ,  $T = 25^\circ\text{C}^{(1)}$

Symbol	Typ	Max	Units	Conditions
$C_{IN}$	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

Note: 1. This parameter is characterized and is not 100% tested.

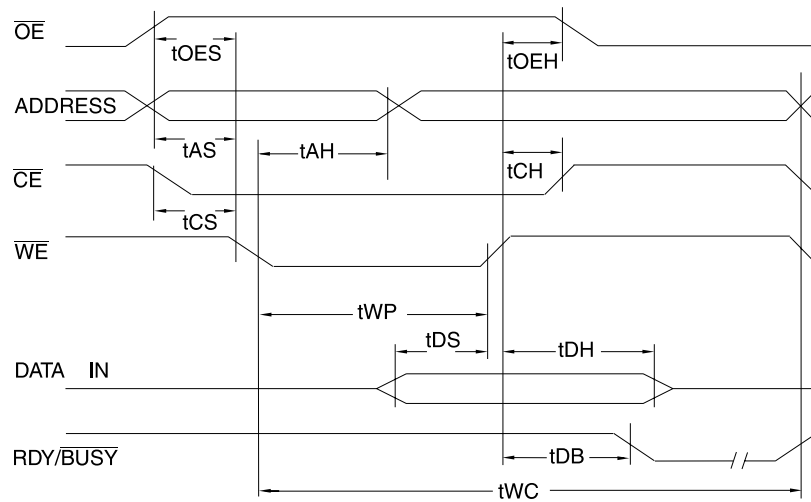


## AC Write Characteristics

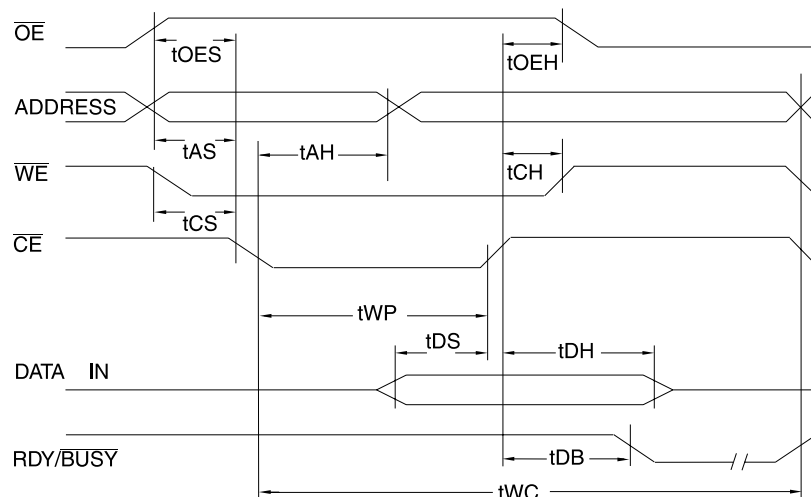
Symbol	Parameter	Min	Max	Units
$t_{AS}, t_{OES}$	Address, $\overline{OE}$ Setup Time	10		ns
$t_{AH}$	Address Hold Time	50		ns
$t_{WP}$	Write Pulse Width ( $\overline{WE}$ or $\overline{CE}$ )	100	1000	ns
$t_{DS}$	Data Setup Time	50		ns
$t_{DH}, t_{OEH}$	Data, $\overline{OE}$ Hold Time	10		ns
$t_{CS}, t_{CH}$	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Setup and Hold Time	0		ns
$t_{DB}$	Time to Device Busy		50	ns
$t_{WC}$	Write Cycle Time (option available)	AT28C64	1	ms
		AT28C64E	200	$\mu$ s

## AC Write Waveforms

### $\overline{WE}$ Controlled



### $\overline{CE}$ Controlled

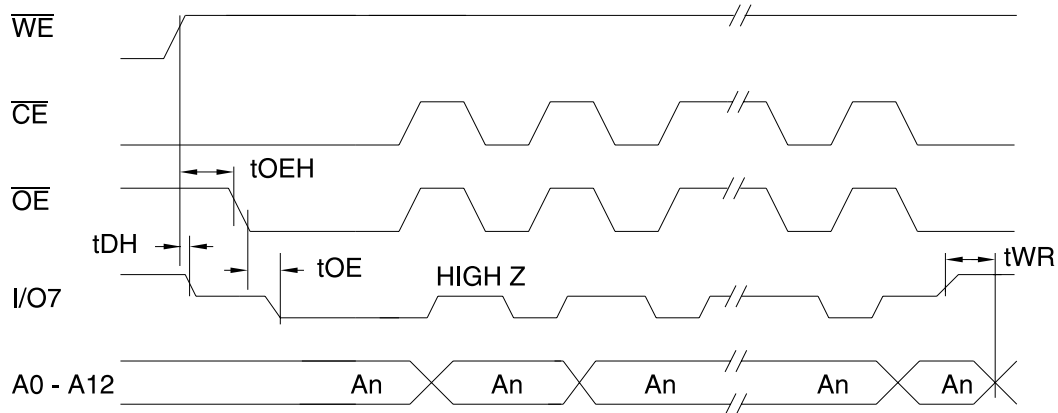


## Data Polling Characteristics<sup>(1)</sup>

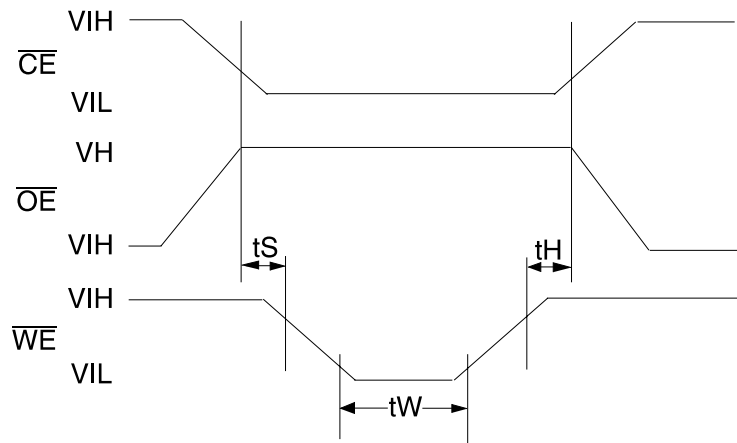
Symbol	Parameter	Min	Typ	Max	Units
$t_{DH}$	Data Hold Time	10			ns
$t_{OE\bar{H}}$	$\bar{O}\bar{E}$ Hold Time	10			ns
$t_{OE}$	$\bar{O}\bar{E}$ to Output Delay <sup>(2)</sup>				ns
$t_{WR}$	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.  
 2. See "AC Read Characteristics".

## Data Polling Waveforms

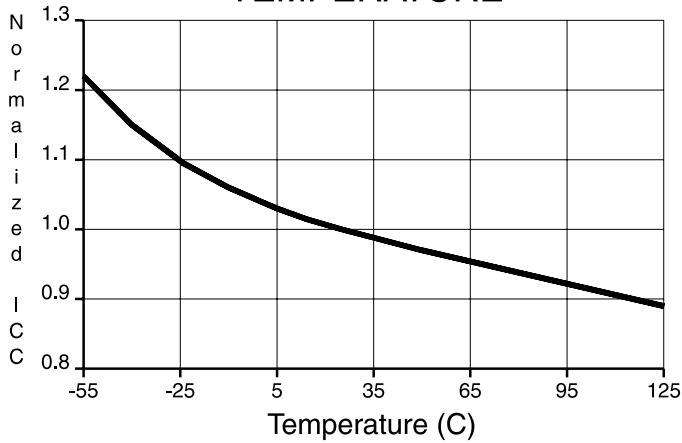


## Chip Erase Waveforms

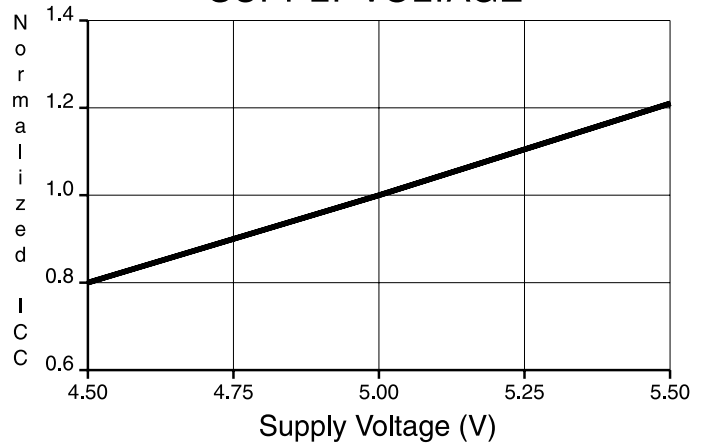


$t_S = t_H = 1 \mu\text{sec (min.)}$   
 $t_W = 10 \text{ msec (min.)}$   
 $V_H = 12.0 \pm 0.5V$

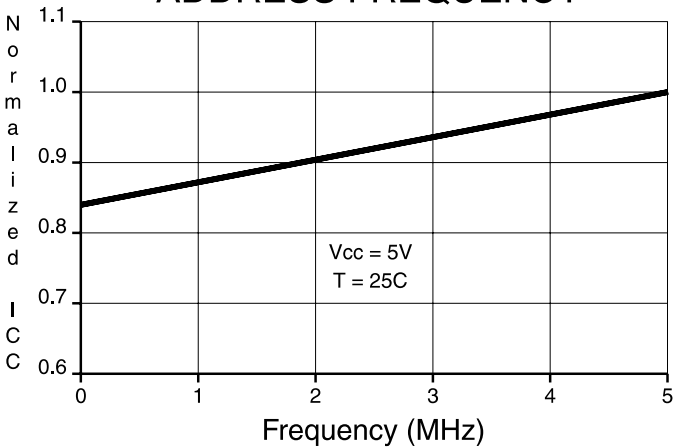
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



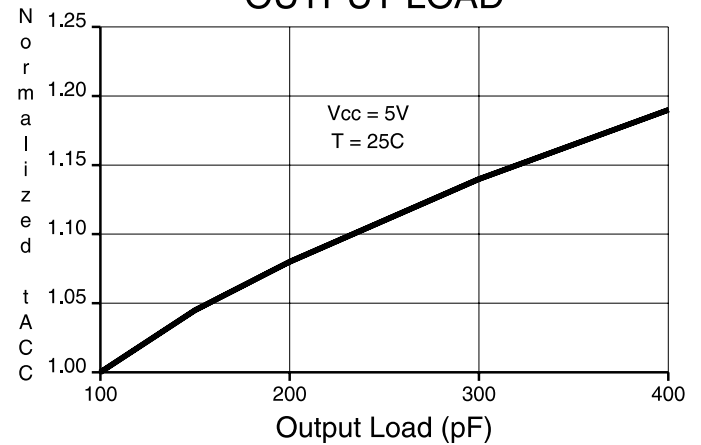
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



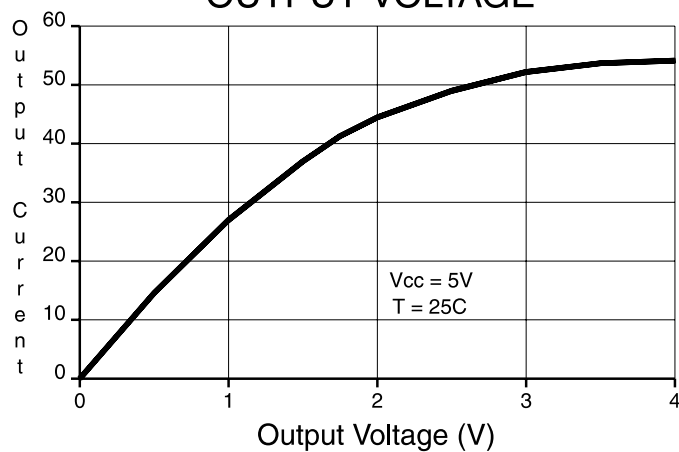
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



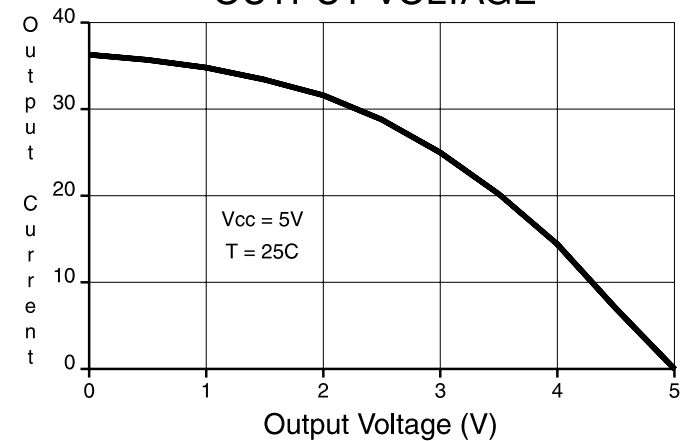
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



## AT28C64 Ordering Information

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	30	0.1	AT28C64-12JC AT28C64-12PC AT28C64-12SC AT28C64-12TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64-12JI AT28C64-12PI AT28C64-12SI AT28C64-12TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
150	30	0.1	AT28C64-15JC AT28C64-15PC AT28C64-15SC AT28C64-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64-15JI AT28C64-15PI AT28C64-15SI AT28C64-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	30	0.1	AT28C64-20JC AT28C64-20PC AT28C64-20SC AT28C64-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64-20JI AT28C64-20PI AT28C64-20SI AT28C64-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	30	0.1	AT28C64-25JC AT28C64-25PC AT28C64-25SC AT28C64-25TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64-25JI AT28C64-25PI AT28C64-25SI AT28C64-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Package Type	
<b>32J</b>	32-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>28P6</b>	28-lead, 0.600" Wide, Plastic Dull Inline Package (PDIP)
<b>28S</b>	28-lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
<b>28T</b>	28-lead, Plastic Thin Small Outline Package (TSOP)
Options	
<b>Blank</b>	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
<b>E</b>	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 μs







## AT28C64X Ordering Information

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C64X-15JC AT28C64X-15PC AT28C64X-15SC AT28C64X-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64X-15JI AT28C64X-15PI AT28C64X-15SI AT28C64X-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	30	0.1	AT28C64X-20JC AT28C64X-20PC AT28C64X-20SC AT28C64X-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64X-20JI AT28C64X-20PI AT28C64X-20SI AT28C64X-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	30	0.1	AT28C64X-25JC AT28C64X-25PC AT28C64X-25SC AT28C64X-25TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64X-25JI AT28C64X-25PI AT28C64X-25SI AT28C64X-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

## Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C64 X	12	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64 X	15	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64 X	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64 X	25	JC, JI, PC, PI, SC, SI, TC, TI

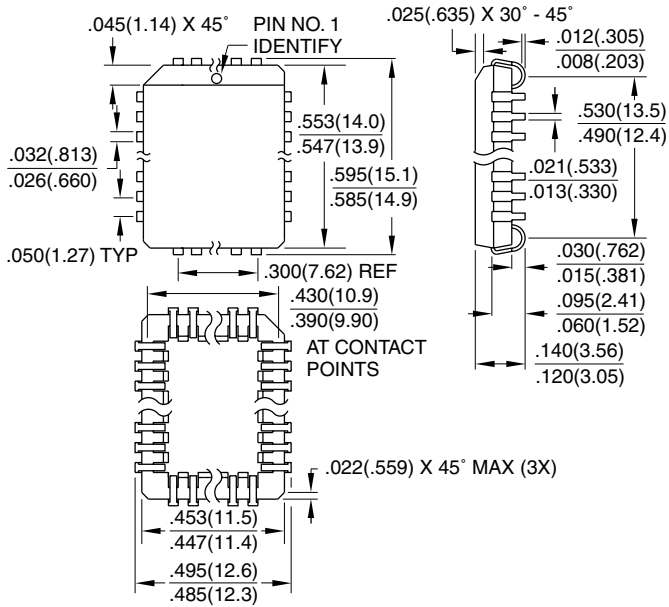
## Die Products

Reference Section: Parallel EEPROM Die Products

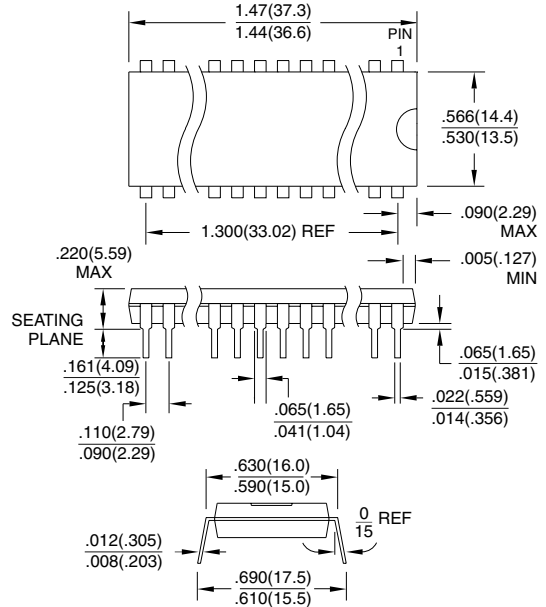
Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28P6	28-lead, 0.600" Wide, Plastic Dull Inline Package (PDIP)
28S	28-lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)

## Packaging Information

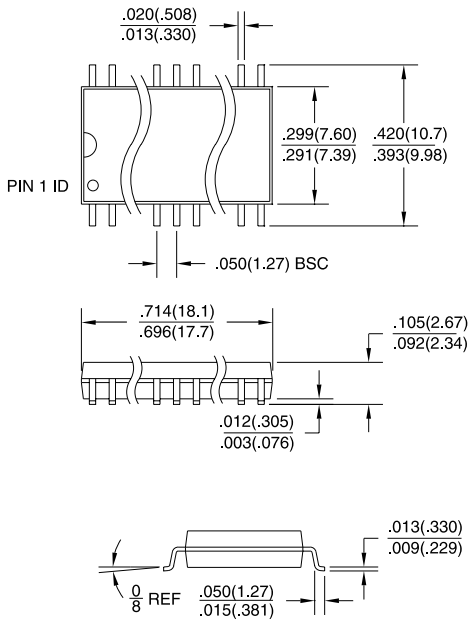
**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)  
 Dimensions in Inches and (Millimeters)  
 JEDEC STANDARD MS-016 AE



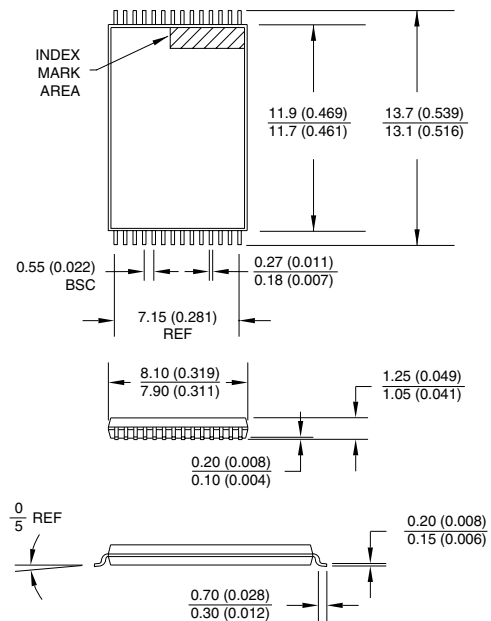
**28P6**, 28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)  
 Dimensions in Inches and (Millimeters)  
 JEDEC STANDARD MS-011 AB



**28S**, 28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)  
 Dimensions in Inches and (Millimeters)



**28T**, 28-lead, Plastic Thin Small Outline Package (TSOP)  
 Dimensions in Millimeters and (Inches)\*



\*Controlling dimension: millimeters



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