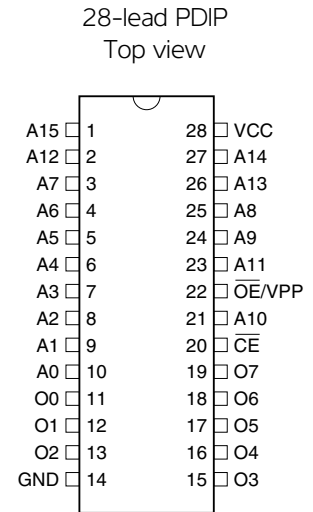
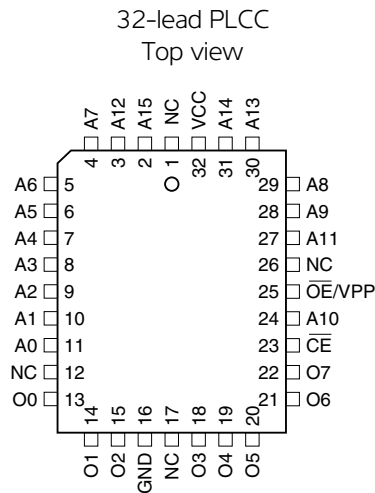


2. Pin configurations

Pin name	Function
A0 - A15	Addresses
O0 - O7	Outputs
\overline{CE}	Chip enable
\overline{OE}/VPP	Output enable/ Program supply
NC	No connect

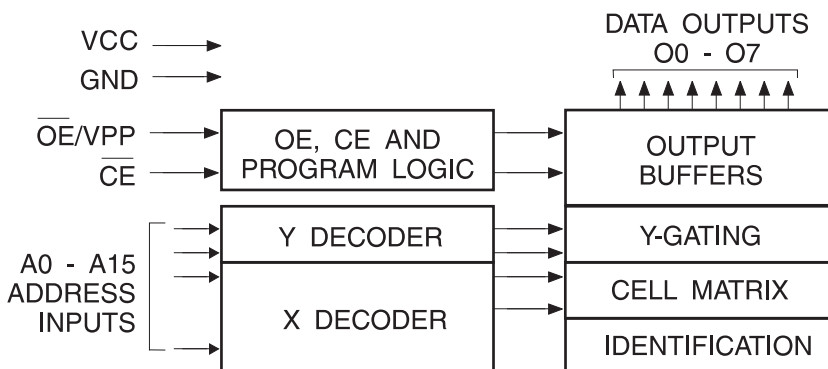


Note: PLCC package pins 1 and 17 are don't connect

3. System considerations

Switching between active and standby conditions via the chip enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device nonconformance. At a minimum, a 0.1 μ F, high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μ F bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Figure 3-1. Block diagram



4. Absolute maximum ratings*

Temperature under bias	-55°C to + 125°C
Storage temperature	-65°C to + 150°C
Voltage on any pin with respect to ground	-2.0V to + 7.0V ⁽¹⁾
Voltage on A9 with respect to ground	-2.0V to + 14.0V ⁽¹⁾
V _{pp} supply voltage with respect to ground	-2.0V to + 14.0V ⁽¹⁾

*NOTICE: Stresses beyond those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to +7.0V for pulses of less than 20ns.

5. DC and AC characteristics

Table 5-1. Operating modes

Mode/Pin	\overline{CE}	\overline{OE}/V_{pp}	Ai	Outputs
Read	V _{IL}	V _{IL}	Ai	D _{OUT}
Output disable	V _{IL}	V _{IH}	X ⁽¹⁾	High Z
Standby	V _{IH}	X ⁽¹⁾	X	High Z
Rapid program ⁽²⁾	V _{IL}	V _{PP}	Ai	D _{IN}
PGM inhibit	V _{IH}	V _{PP}	X ⁽¹⁾	High Z
Product identification ⁽⁴⁾	V _{IL}	V _{IL}	A9 = V _H ⁽³⁾ A0 = V _{IH} or V _{IL} A1 - A15 = V _{IL}	Identification code

Notes: 1. X can be V_{IL} or V_{IH}.
 2. Refer to programming characteristics.
 3. V_H = 12.0 ± 0.5V.
 4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the manufacturer's identification byte and high (V_{IH}) to select the device code byte.

Table 5-2. DC and AC operating conditions for read operation

		Atmel AT27C512R	
		-45	-70
Operating temp. (case)	Ind.	-40°C - 85°C	-40°C - 85°C
	Auto.		-40°C - 125°C
V _{CC} supply		5V ± 10%	5V ± 10%

Table 5-3. DC and operating characteristics for read operation

Symbol	Parameter	Condition	Min	Max	Units	
I_{LI}	Input load current	$V_{IN} = 0V$ to V_{CC}	Ind.		± 1	μA
			Auto.		± 5	μA
I_{LO}	Output leakage current	$V_{OUT} = 0V$ to V_{CC}	Ind.		± 5	μA
			Auto.		± 10	μA
I_{SB}	$V_{CC}^{(1)}$ standby current	I_{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA	
		I_{SB2} (TTL), $\overline{CE} = 2.0$ to $V_{CC} + 0.5V$		1	mA	
I_{CC}	V_{CC} active current	$f = 5MHz$, $I_{OUT} = 0mA$, $\overline{CE} = V_{IL}$		20	mA	
V_{IL}	Input low voltage		-0.6	0.8	V	
V_{IH}	Input high voltage		2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$		0.4	V	
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4		V	

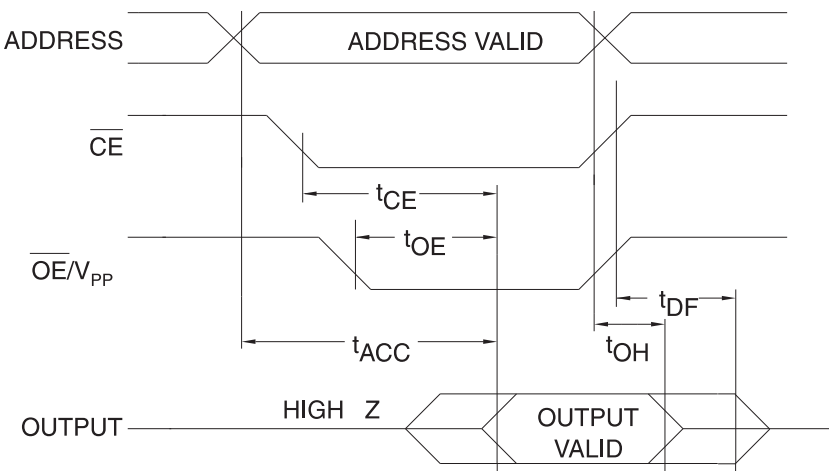
Note: 1. V_{CC} must be applied simultaneously with or before \overline{OE}/V_{pp} , and removed simultaneously with or after \overline{OE}/V_{pp} .

Table 5-4. AC characteristics for read operation

Symbol	Parameter	Condition	Atmel AT27C512R				Units
			-45		-70		
			Min	Max	Min	Max	
$t_{ACC}^{(1)}$	Address to output delay	$\overline{CE} = \overline{OE}/V_{pp} = V_{IL}$		45		70	ns
$t_{CE}^{(1)}$	\overline{CE} to output delay	$\overline{OE}/V_{pp} = V_{IL}$		45		70	ns
$t_{OE}^{(1)}$	\overline{OE}/V_{pp} to output delay	$\overline{CE} = V_{IL}$		20		30	ns
$t_{DF}^{(1)}$	\overline{OE}/V_{pp} or \overline{CE} high to output float, whichever occurred first			20		25	ns
t_{OH}	Output hold from address, \overline{CE} or \overline{OE}/V_{pp} , whichever occurred first		7		7		ns

Note: 1. See AC waveforms for read operation.

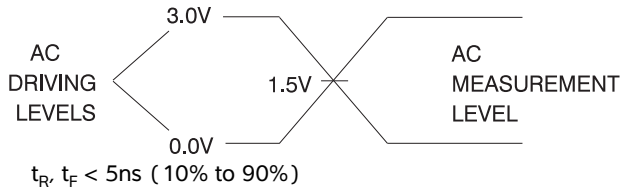
Figure 5-1. AC waveforms for read operation⁽¹⁾



- Notes:
1. Timing measurement reference level is 1.5V for -45 devices. Input AC drive levels are $V_{IL} = 0.0V$ and $V_{IH} = 3.0V$. Timing measurement reference levels for all other speed grades are $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$. Input AC drive levels are $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$.
 2. \overline{OE}/V_{pp} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .
 3. \overline{OE}/V_{pp} may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC} .
 4. This parameter is only sampled, and is not 100% tested.
 5. Output float is defined as the point when data is no longer driven.

Figure 5-2. Input test waveforms and measurement levels

For -45 devices only:



For -70 devices:

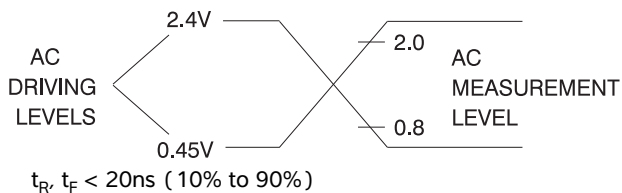
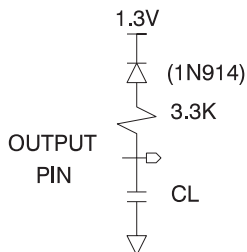


Figure 5-3. Output test load



Note: 1. $C_L = 100\text{pF}$ including jig capacitance, except for the -45 devices, where $C_L = 30\text{pF}$.

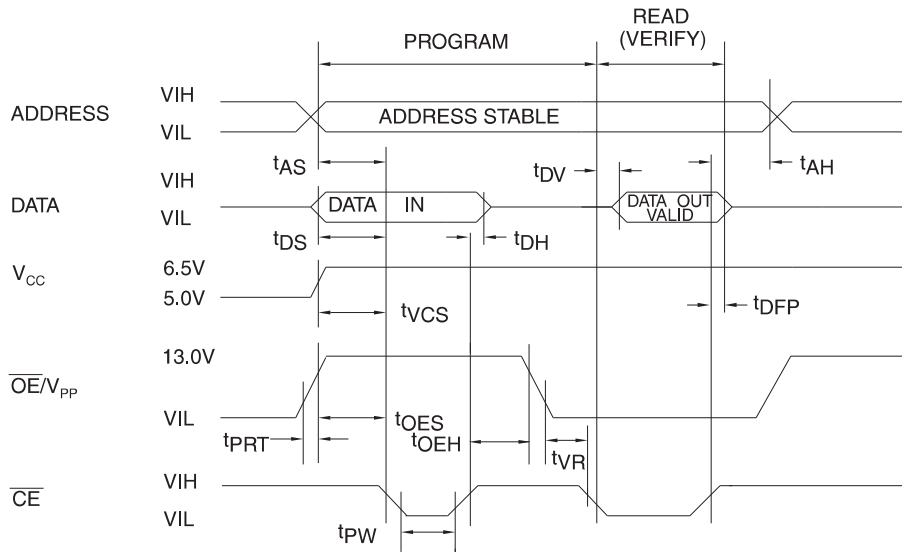
Table 5-5. Pin capacitance

$f = 1\text{MHz}$, $T = 25^\circ\text{C}$ ⁽¹⁾

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0\text{V}$
C_{OUT}	8	12	pF	$V_{OUT} = 0\text{V}$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled, and is not 100% tested.

Figure 5-4. Programming Waveforms ⁽¹⁾



- Notes:
1. The input timing reference is 0.8V for V_{IL} and 2.0V for V_{IH} .
 2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

Table 5-6. DC programming characteristics

 $T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $\overline{\text{OE}}/V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test conditions	Limits		Units
			Min	Max	
I_{LI}	Input load current	$V_{IN} = V_{IL}, V_{IH}$		± 10	μA
V_{IL}	Input low level		-0.6	0.8	V
V_{IH}	Input high level		2.0	$V_{CC} + 1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1\text{mA}$		0.4	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu\text{A}$	2.4		V
I_{CC2}	V_{CC} supply current (program and verify)			25	mA
I_{PP2}	$\overline{\text{OE}}/V_{PP}$ current	$\overline{\text{CE}} = V_{IL}$		25	mA
V_{ID}	A9 product identification voltage		11.5	12.5	V

Table 5-7. AC programming characteristics

 $T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $\overline{\text{OE}}/V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test conditions ⁽¹⁾	Limits		Units
			Min	Max	
t_{AS}	Address setup time	Input rise and fall times (10% to 90%) 20ns	2		μs
t_{OES}	$\overline{\text{OE}}/V_{PP}$ setup time		2		μs
t_{OEH}	$\overline{\text{OE}}/V_{PP}$ hold time		2		μs
t_{DS}	Data setup time		2		μs
t_{AH}	Address hold time	Input pulse levels 0.45V to 2.4V	0		μs
t_{DH}	Data hold time		2		μs
t_{DFP}	$\overline{\text{CE}}$ high to output float delay ⁽²⁾	Input timing reference level	0	130	ns
t_{VCS}	V_{CC} setup time	0.8V to 2.0V	2		μs
t_{PW}	$\overline{\text{CE}}$ program pulse width ⁽³⁾	Output timing reference level 0.8V to 2.0V	95	105	μs
t_{DV}	Data valid from $\overline{\text{CE}}$ ⁽²⁾			1	μs
t_{VR}	$\overline{\text{OE}}/V_{PP}$ recovery time		2		μs
t_{PRT}	$\overline{\text{OE}}/V_{PP}$ pulse rise time during programming		50		ns

- Notes:
- V_{CC} must be applied simultaneously with or before $\overline{\text{OE}}/V_{PP}$ and removed simultaneously with or after $\overline{\text{OE}}/V_{PP}$.
 - This parameter is only sampled, and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.
 - Program pulse width tolerance is $100\mu\text{sec} \pm 5\%$.

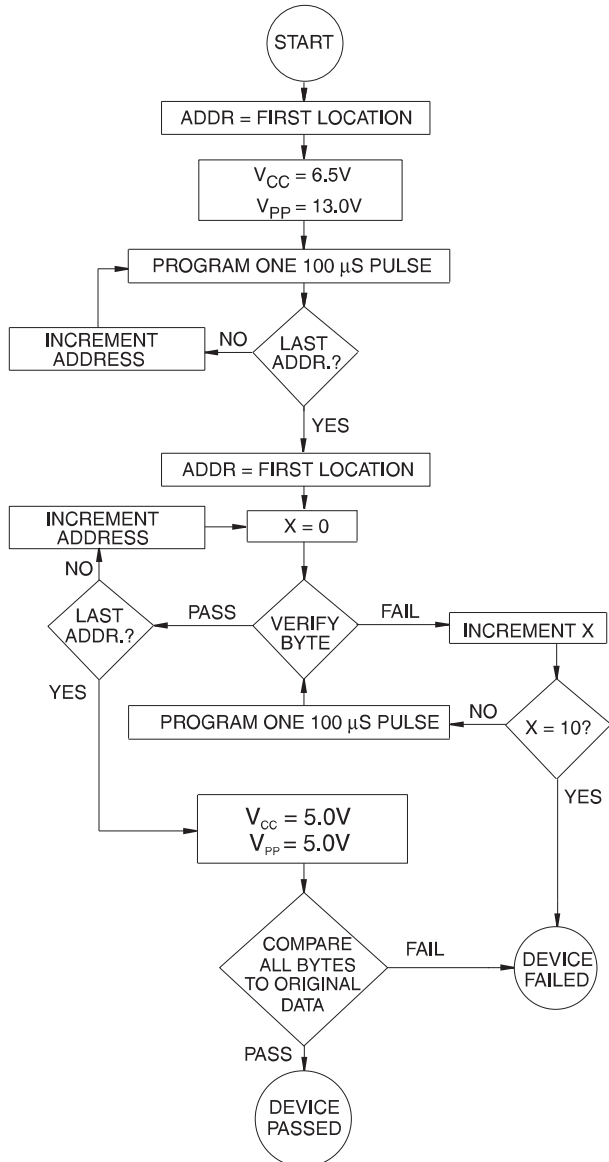
Table 5-8. The Atmel AT27C512R integrated product identification code

Codes	Pins									Hex data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device type	1	0	0	0	0	1	1	0	1	0D

6. Rapid programming algorithm

A $100\mu\text{s}$ $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{\text{OE}}/V_{\text{pp}}$ is raised to 13.0V. Each address is first programmed with one $100\mu\text{s}$ $\overline{\text{CE}}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive $100\mu\text{s}$ pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{\text{OE}}/V_{\text{pp}}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

Figure 6-1. Rapid programming algorithm



7. Ordering information

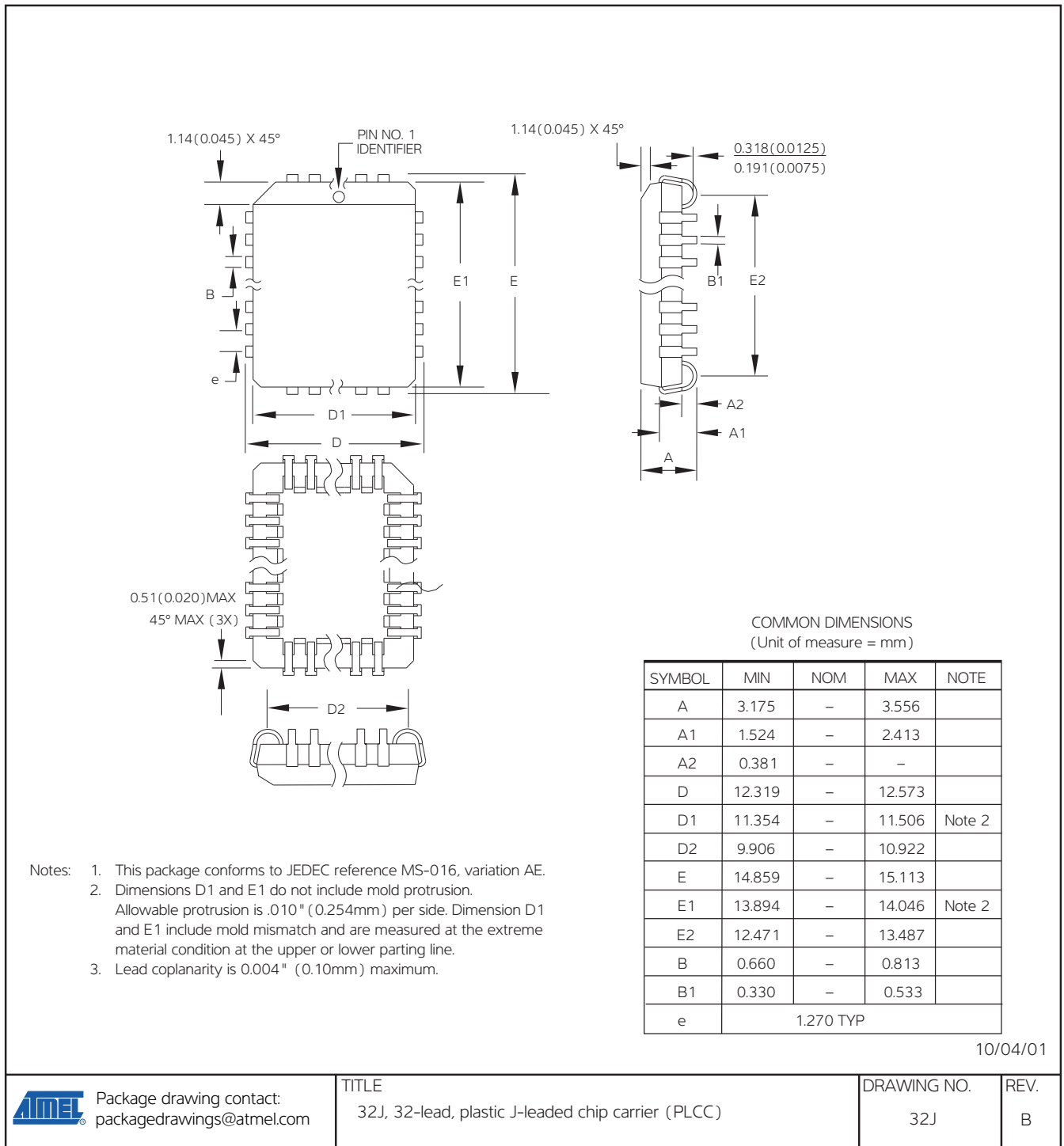
Green package (Pb/halide-free)

t _{ACC} (ns)	I _{CC} (mA)		Atmel ordering code	Package	Lead finish	Operation range
	Active	Standby				
45	20	0.1	AT27C512R-45JU	32J	Matte tin	Industrial (-40°C to 85°C)
			AT27C512R-45PU	28P6	Matte tin	
70	20	0.1	AT27C512R-70JU	32J	Matte tin	Industrial (-40°C to 85°C)
			AT27C512R-70PU	28P6	Matte tin	

Package type	
32J	32-lead, plastic, J-leaded chip carrier (PLCC)
28P6	28-lead, 0.600" wide, plastic, dual inline package (PDIP)

8. Packaging information

32J – PLCC



10/04/01



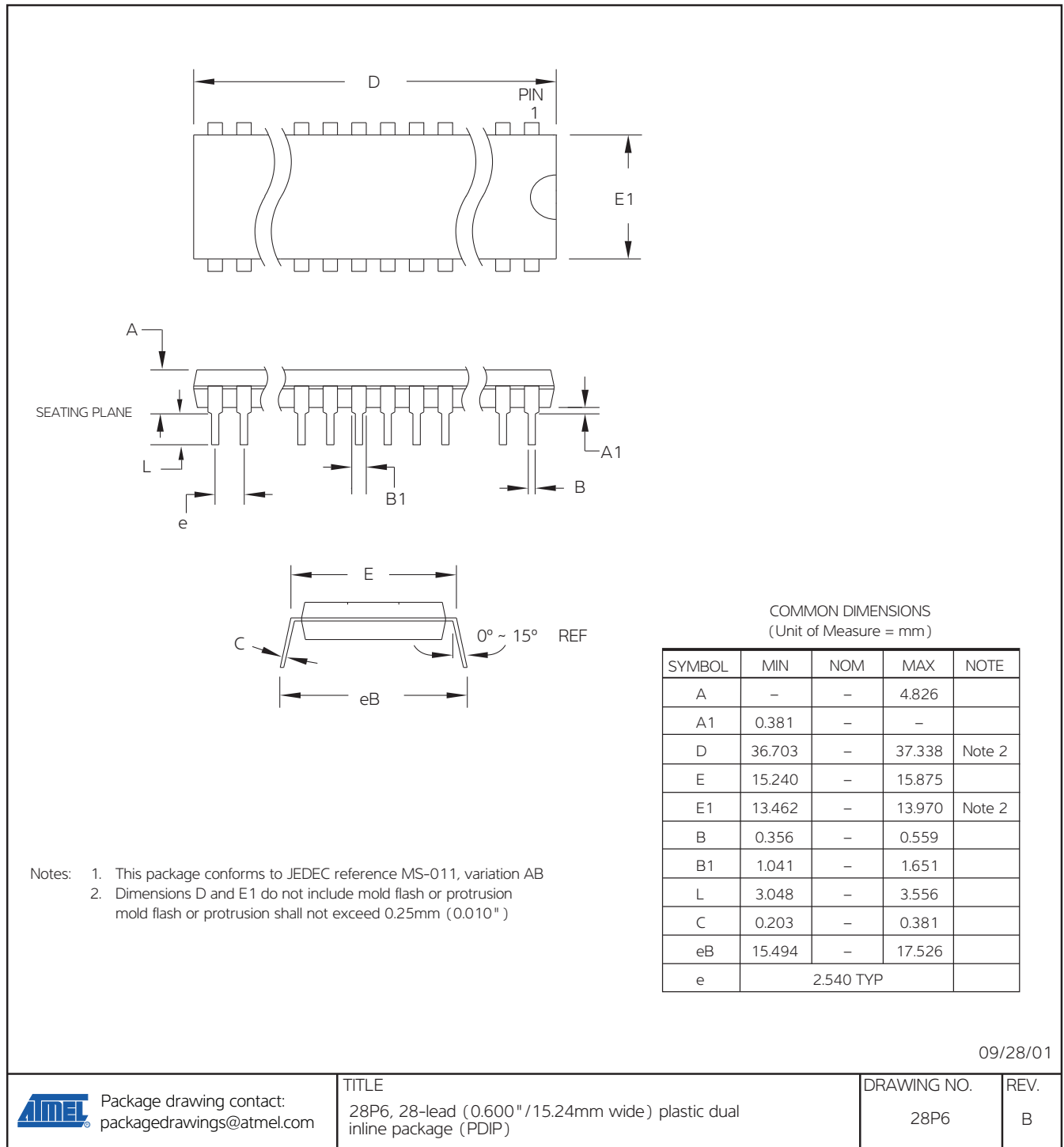
Package drawing contact:
packagedrawings@atmel.com

TITLE
32J, 32-lead, plastic J-leaded chip carrier (PLCC)

DRAWING NO.
32J

REV.
B

28P6 – PDIP





9. Revision history

Doc. rev.	Date	Comments
0015Q	10/2011	Correct pinout note
0015P	04/2011	Remove TSOP and SOIC packages Add lead finish to ordering information
0015O	12/2007	



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