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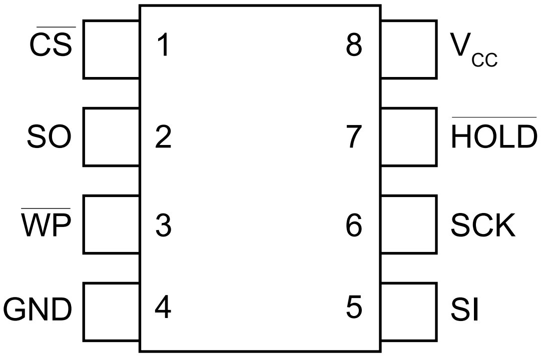
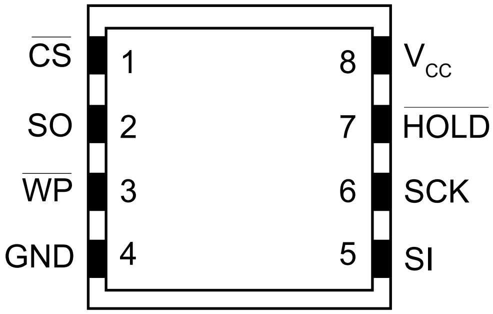
1. Package Types (not to scale)

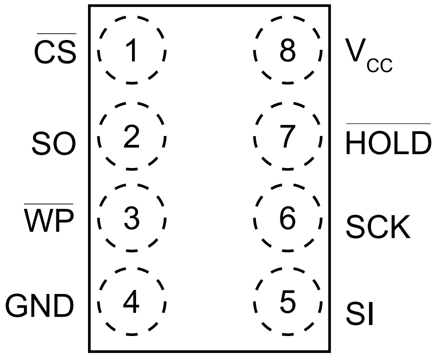
8-Lead SOIC/TSSOP
(Top View)



8-Pad UDFN/XDFN
(Top View)



8-Ball VFBGA
(Top View)



2. Pin Description

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	8-Lead SOIC	8-Lead TSSOP	8-Pad UDFN(1)	8-Pad XDFN	8-Ball VFBGA	Function
$\overline{\text{CS}}$	1	1	1	1	1	Chip Select
SO	2	2	2	2	2	Serial Data Output
$\overline{\text{WP}}$(2)	3	3	3	3	3	Write-Protect
GND	4	4	4	4	4	Ground
SI	5	5	5	5	5	Serial Data Input
SCK	6	6	6	6	6	Serial Data Clock
$\overline{\text{HOLD}}$(2)	7	7	7	7	7	Suspends Serial Input
V_{CC}	8	8	8	8	8	Device Power Supply

Note:

1. The exposed pad on this package can be connected to GND or left floating.
2. The Write-Protect ($\overline{\text{WP}}$) and Hold ($\overline{\text{HOLD}}$) pins should be driven high or low as appropriate.

2.1 Chip Select ($\overline{\text{CS}}$)

The AT25320B/AT25640B is selected when the $\overline{\text{CS}}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the Serial Output (SO) pin will remain in a high-impedance state.

To ensure robust operation, the Chip Select ($\overline{\text{CS}}$) pin should follow V_{CC} upon power-up. It is therefore recommended to connect $\overline{\text{CS}}$ to V_{CC} using a pull-up resistor (less than or equal to 10 kΩ). After power-up, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

2.2 Serial Data Output (SO)

The Serial Data Output (SO) pin is used to transfer data out of the AT25320B/AT25640B. During a read sequence, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Write-Protect ($\overline{\text{WP}}$)

The Write-Protect ($\overline{\text{WP}}$) pin will allow normal read/write operations when held high. When the $\overline{\text{WP}}$ pin is brought low and WPEN bit is set to a logic '`1`', all write operations to the STATUS register are inhibited. $\overline{\text{WP}}$ going low while $\overline{\text{CS}}$ is still low will interrupt a write operation to the STATUS register. If the internal write cycle has already been initiated, $\overline{\text{WP}}$ going low will have no effect on any write operation to the STATUS register. The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the STATUS register is set to a logic '`0`'. This will allow the user to install the AT25320B/AT25640B in a system with the $\overline{\text{WP}}$ pin tied to ground and still be able to write to the STATUS register. All $\overline{\text{WP}}$ pin functions are enabled when the WPEN bit is set to a logic '`1`'.

2.4 Ground (GND)

The ground reference for the power supply. The Ground (GND) pin should be connected to the system ground.

2.5 Serial Data Input (SI)

The Serial Data Input (SI) pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

2.6 Serial Data Clock (SCK)

The Serial Data Clock (SCK) pin is used to synchronize the communication between a master and the AT25320B/AT25640B. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.7 Suspends Serial Input ($\overline{\text{HOLD}}$)

The $\overline{\text{HOLD}}$ pin is used in conjunction with the $\overline{\text{CS}}$ pin to pause the AT25320B/AT25640B. When the device is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{\text{HOLD}}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{\text{HOLD}}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{\text{HOLD}}$). Inputs to the SI pin will be ignored while the SO pin is in the high-impedance state.

2.8 Device Power Supply (V_{CC})

The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

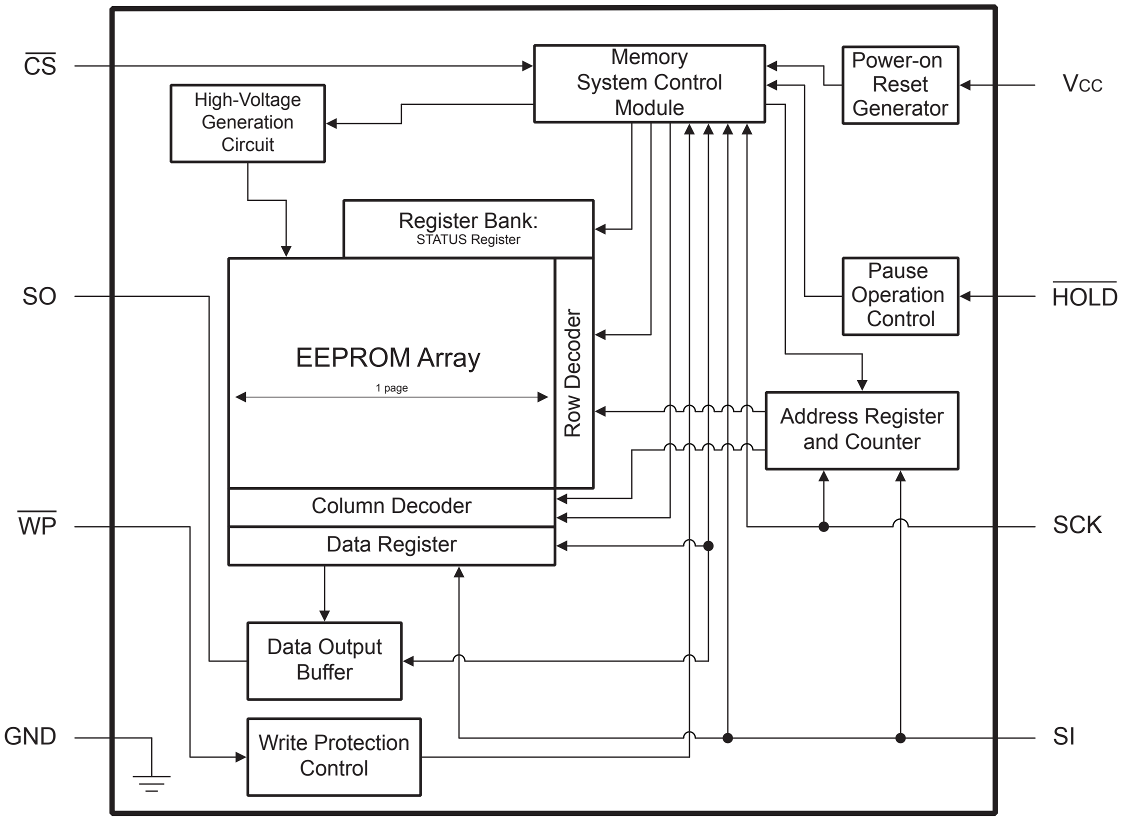
3. Description

The AT25320B/AT25640B provides 32,768/65,536 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 4,096/8,192 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

The AT25320B/AT25640B is enabled through the Chip Select ($\overline{\text{CS}}$) pin and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO) and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate erase cycle is required before write.

Block write protection is enabled by programming the STATUS register with one of four blocks of write protection. Separate Program Enable and Program Disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{\text{WP}}$ pin to protect against inadvertent write attempts to the STATUS register. The $\overline{\text{HOLD}}$ pin may be used to suspend any serial communication without resetting the serial sequence.

3.1 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Operating temperature	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
V_{CC}	6.25V
DC output current	5.0 mA
ESD protection	2 kV

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

AT25320B/AT25640B		
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low Voltage Grade	1.8V to 5.5V

4.3 DC Characteristics

Table 4-2. DC Characteristics (1)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Conditions
Supply Voltage	V_{CC1}	1.8	—	5.5	V	
Supply Voltage	V_{CC2}	2.5	—	5.5	V	
Supply Voltage	V_{CC3}	4.5	—	5.5	V	
Supply Current	I_{CC1}	—	7.5	10.0	mA	V_{CC} = 5.0V at 20 MHz, SO = Open, Read
Supply Current	I_{CC2}	—	4.0	10.0	mA	V_{CC} = 5.0V at 20 MHz, SO = Open, Read, Write
Supply Current	I_{CC3}	—	4.0	6.0	mA	V_{CC} = 5.0V at 5 MHz, SO = Open, Read, Write
Standby Current	I_{SB1}	—	<0.1	6.0(2)	µA	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}

Parameter	Symbol	Minimum	Typical	Maximum	Units	Conditions	
Standby Current	I_{SB2}	—	0.3	7.0(2)	µA	V_{CC} = 2.5V, $\overline{CS}$ = V_{CC}	
Standby Current	I_{SB3}	—	2.0	10.0(2)	µA	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}	
Input Leakage	I_{IL}	-3.0	—	3.0	µA	V_{IN} = 0V to V_{CC}	
Output Leakage	I_{OL}	-3.0	—	3.0	µA	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to +70°C	
Input Low-Voltage	V_{IL}(3)	-0.6	—	V_{CC} x 0.3	V		
Input High-Voltage	V_{IH}(3)	V_{CC} x 0.7	—	V_{CC} + 0.5	V		
Output Low-Voltage	V_{OL1}	—	—	0.4	V	3.6V ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0 mA
Output High-Voltage	V_{OH1}	V_{CC} - 0.8	—	—	V	3.6V ≤ V_{CC} ≤ 5.5V	I_{OH} = -1.6 mA
Output Low-Voltage	V_{OL2}	—	—	0.2	V	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA
Output High-Voltage	V_{OH2}	V_{CC} - 0.2	—	—	V	1.8V ≤ V_{CC} ≤ 3.6V	I_{OH} = -100 µA

Note:

1. Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).
2. Worst case measured at 85°C.
3. V_{IL} min and V_{IH} max are reference only and are not tested.

4.4 AC Characteristics

Table 4-3. AC Characteristics(1)

Parameter	Symbol	Minimum	Maximum	Units	Conditions
SCK Clock Frequency	f_{SCK}	0	20	MHz	V_{CC} = 4.5V to 5.5V
		0	10	MHz	V_{CC} = 2.5V to 5.5V
		0	5	MHz	V_{CC} = 1.8V to 5.5V
Input Rise Time	t_{RI}	—	2	µs	V_{CC} = 4.5V to 5.5V
		—	2	µs	V_{CC} = 2.5V to 5.5V
		—	2	µs	V_{CC} = 1.8V to 5.5V
Input Fall Time	t_{FI}	—	2	µs	V_{CC} = 4.5V to 5.5V
		—	2	µs	V_{CC} = 2.5V to 5.5V

Parameter	Symbol	Minimum	Maximum	Units	Conditions
		—	2	µs	V_{CC} = 1.8V to 5.5V
SCK High Time	t_{WH}	20	—	ns	V_{CC} = 4.5V to 5.5V
		40	—	ns	V_{CC} = 2.5V to 5.5V
		80	—	ns	V_{CC} = 1.8V to 5.5V
SCK Low Time	t_{WL}	20	—	ns	V_{CC} = 4.5V to 5.5V
		40	—	ns	V_{CC} = 2.5V to 5.5V
		80	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{\text{CS}}$ High Time	t_{CS}	25	—	ns	V_{CC} = 4.5V to 5.5V
		50	—	ns	V_{CC} = 2.5V to 5.5V
		100	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{\text{CS}}$ Setup Time	t_{CSS}	25	—	ns	V_{CC} = 4.5V to 5.5V
		50	—	ns	V_{CC} = 2.5V to 5.5V
		100	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{\text{CS}}$ Hold Time	t_{CSH}	25	—	ns	V_{CC} = 4.5V to 5.5V
		50	—	ns	V_{CC} = 2.5V to 5.5V
		100	—	ns	V_{CC} = 1.8V to 5.5V
Data In Setup Time	t_{SU}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.8V to 5.5V
Data In Hold Time	t_H	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{\text{HOLD}}$ Setup Time	t_{HD}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{\text{HOLD}}$ Hold Time	t_{CD}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.8V to 5.5V
Output Valid	t_V	0	20	ns	V_{CC} = 4.5V to 5.5V
		0	40	ns	V_{CC} = 2.5V to 5.5V
		0	80	ns	V_{CC} = 1.8V to 5.5V
Output Hold Time	t_{HO}	0	—	ns	V_{CC} = 4.5V to 5.5V

Parameter	Symbol	Minimum	Maximum	Units	Conditions
		0	—	ns	V_{CC} = 2.5V to 5.5V
		0	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{\text{HOLD}}$ to Output Low Z	t_{LZ}	0	25	ns	V_{CC} = 4.5V to 5.5V
		0	50	ns	V_{CC} = 2.5V to 5.5V
		0	100	ns	V_{CC} = 1.8V to 5.5V
$\overline{\text{HOLD}}$ to Output High Z	t_{HZ}	—	40	ns	V_{CC} = 4.5V to 5.5V
		—	80	ns	V_{CC} = 2.5V to 5.5V
		—	200	ns	V_{CC} = 1.8V to 5.5V
Output Disable Time	t_{DIS}	—	40	ns	V_{CC} = 4.5V to 5.5V
		—	80	ns	V_{CC} = 2.5V to 5.5V
		—	200	ns	V_{CC} = 1.8V to 5.5V
Write Cycle Time	t_{WC}	—	5	ms	V_{CC} = 4.5V to 5.5V
		—	5	ms	V_{CC} = 2.5V to 5.5V
		—	5	ms	V_{CC} = 1.8V to 5.5V

Note:

1. Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = As Specified, C_L = 1 TTL Gate and 30 pF (unless otherwise noted).

4.5 Electrical Specifications

4.5.1 Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT25320B/AT25640B should monotonically rise from GND to the minimum V_{CC} level as specified in Table 4-1 with a slew rate no faster than 0.1 V/µs.

4.5.1.1 Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT25320B/AT25640B includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any instructions until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once the V_{CC} is greater than or equal to the minimum V_{CC} level, the bus master must wait at least t_{PUP} before sending the first instruction to the device. See Table 4-4 for the values associated with these power-up parameters.

Table 4-4. Power-Up Conditions(1)

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept instructions.	100	—	μs
V_{POR}	Power-on Reset Threshold Voltage.	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles.	500	—	ms

Note:

1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT25320B/AT25640B drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the V_{CC} pin to GND in less than 1 ms, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

4.5.2 Pin Capacitance

Table 4-5. Pin Capacitance(1,2)

Symbol	Test Conditions	Max.	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note:

1. This parameter is characterized and is not 100% tested.
2. Applicable over recommended operating range from: T_A = 25°C, f_{SCK} = 1.0 MHz, V_{CC} = 5.0V (unless otherwise noted).

4.5.3 EEPROM Cell Performance Characteristics

Table 4-6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance(1)	T_A = 25°C,V_{CC}= 3.3V, Page Mode	1,000,000	—	Write Cycles
Data Retention(1)	T_A = 55°C	100	—	Years

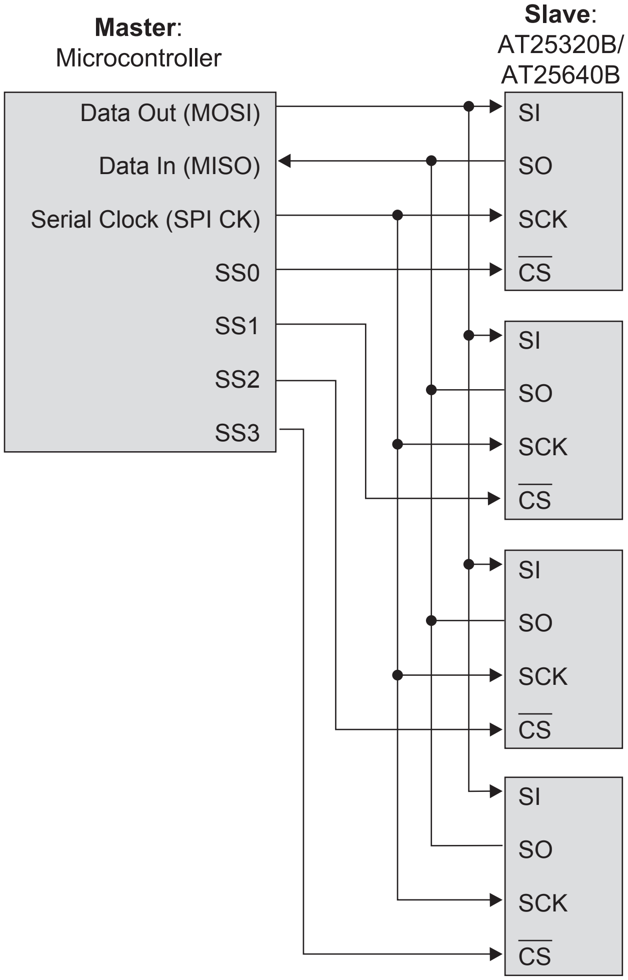
Note:

1. Performance is determined through characterization and the qualification process.

5. Serial Interface Description

Master:	The device that generates the serial clock.
Slave:	Because the Serial Clock (SCK) pin is always an input, the AT25320B/AT25640B always operates as a slave.
Transmitter/ receiver:	The AT25320B/AT25640B has separate pins designated for data transmission (SO) and reception (SI).
MSb:	The Most Significant bit (MSb) is the first bit transmitted and received.
Serial Opcode:	After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the opcode that defines the operations to be performed.
Invalid Opcode:	If an invalid opcode is received, no data will be shifted into the AT25320B/AT25640B, and the Serial Output (SO) pin will remain in a high-impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

Figure 5-1. SPI Serial Interface



6. Functional Description

The AT25320B/AT25640B is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

The AT25320B/AT25640B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 6-1. All instructions, addresses and data are transferred with the MSb first and start with a high-to-low $\overline{\text{CS}}$ transition.

Table 6-1. Instruction Set

Instruction Name	Instruction Format	Operation
`WREN`	`0000 X110`	Set Write Enable Latch
`WRDI`	`0000 X100`	Reset Write Enable Latch
`RDSR`	`0000 X101`	Read STATUS Register
`WRSR`	`0000 X001`	Write STATUS Register
`READ`	`0000 X011`	Read Data from Memory Array
`WRITE`	`0000 X010`	Write Data to Memory Array

Write Enable (WREN): The device will power-up in the Write Disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

Write Disable (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The `WRDI` instruction is independent of the status of the $\overline{\text{WP}}$ pin.

Read STATUS Register (RDSR): The Read STATUS Register instruction provides access to the STATUS register. The $\overline{\text{Ready}}$/Busy and Write Enable status of the device can be determined by the `RDSR` instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the `WRSR` instruction.

Table 6-2. STATUS Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{\text{RDY}}$

Table 6-3. Read STATUS Register Bit Definition

Bit	Definition
Bit 0 ($\overline{\text{RDY}}$)	Bit 0 = `0` ($\overline{\text{RDY}}$) indicates the device is READY. Bit 0 = `1` indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1= `0` indicates the device is not write enabled. Bit 1 = `1` indicates the device is write enabled.
Bit 2 (BP0)	See Table 6-4.
Bit 3 (BP1)	See Table 6-4.

Bit	Definition
Bits 4 – 6 are zeros when device is not in an internal write cycle.	
Bit 7 (WPEN)	See Table 6-5.
Bits 0 – 7 are ones during an internal write cycle.	

Write STATUS Register (WRSR): The `WRSR` instruction allows the user to select one of four levels of protection. The AT25320B/AT25640B is divided into four array segments. One-quarter, one-half or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read-only. The Block Write Protection levels and corresponding STATUS register control bits are shown in Table 6-4.

The three bits BP0, BP1 and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., `WREN`, t_{WC}, `RDSR`).

Table 6-4. Block Write-Protect Bits

Level	STATUS Register Bits		Array Addresses Protected	
	BP1	BP0	AT25320B	AT25640B
0	0	0	None	None
1(1/4)	0	1	0C00-0FFF	1800-1FFF
2(1/2)	1	0	0800-0FFF	1000-1FFF
3(All)	1	1	0000-0FFF	0000-1FFF

The `WRSR` instruction also allows the user to enable or disable the Write-Protect ($\overline{\text{WP}}$) pin through the use of the Write-Protect Enable (WPEN) bit. Hardware Write Protection is enabled when the $\overline{\text{WP}}$ pin is low and the WPEN bit is set to a logic '`1`'. Hardware Write Protection is disabled when either the $\overline{\text{WP}}$ pin is high or the WPEN bit is set to a logic '`0`'. When the device is Hardware Write-Protected, writes to the STATUS register, including the Block Protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory that are not block-protected.

Note: When the WPEN bit is Hardware Write-Protected, it cannot be set back to a logic '`0`' as long as the $\overline{\text{WP}}$ pin is held low.

Table 6-5. WPEN Operation

WPEN	$\overline{\text{WP}}$	WEN	Protected Blocks	Unprotected Blocks	STATUS Register
0	x	0	Protected	Protected	Protected
0	x	1	Protected	Writeable	Writeable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writeable	Protected
x	High	0	Protected	Protected	Protected
x	High	1	Protected	Writeable	Writeable

Read Sequence (READ): Reading the AT25320B/AT25640B via the Serial Output (SO) pin requires the following sequence. After the $\overline{\text{CS}}$ line is pulled low to select a device, the `READ` instruction is transmitted via the SI line followed by the byte address to be read (A15 – A0, see Table 6-6). Upon completion, any data on the SI line will be ignored. The data (D7 – D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{\text{CS}}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous read cycle.

Write Sequence (WRITE): In order to program the AT25320B/AT25640B, two separate instructions must be executed. First, the device ***must be write enabled*** via the `WREN` instruction. Then a `WRITE` instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection level. During an internal write cycle, all instructions will be ignored except the `RDSR` instruction.

A `WRITE` instruction requires the following sequence. After the $\overline{\text{CS}}$ line is pulled low to select the device, the `WRITE` instruction is transmitted via the SI line followed by the byte address (A15 – A0) and the data (D7 – D0) to be programmed (see Table 6-6). Programming will start after the $\overline{\text{CS}}$ pin is brought high. The low-to-high transition of the $\overline{\text{CS}}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSb) data bit.

The $\overline{\text{Ready}}$/Busy status of the device can be determined by initiating a Read STATUS Register (`RDSR`) instruction. If Bit 0 = `1`, the write cycle is still in progress. If Bit 0 = `0`, the write cycle has ended. Only the `RDSR` instruction is enabled during the write programming cycle.

The AT25320B/AT25640B is capable of a 32-byte page write operation. After each byte of data is received, the five low-order address bits are internally incremented by one; the high-order bits of the address will remain constant. If more than 32 bytes of data are transmitted, the address counter will rollover and the previously written data will be overwritten. The AT25320B/AT25640B is automatically returned to the write disable state at the completion of a write cycle.

Note: If the device is not write enabled, the device will ignore the `WRITE` instruction and will return to the Standby state, when $\overline{\text{CS}}$ is brought high. A new $\overline{\text{CS}}$ falling edge is required to reinitiate the serial communication.

Table 6-6. Address Key

Address	AT25320B	AT25640B
A_N	A_{11}–A_0	A_{12}–A_0
Don’t Care Bits	A_{15}–A_{12}	A_{15}–A_{13}

7. Timing Diagrams

Figure 7-1. Synchronous Data Timing (for Mode 0)

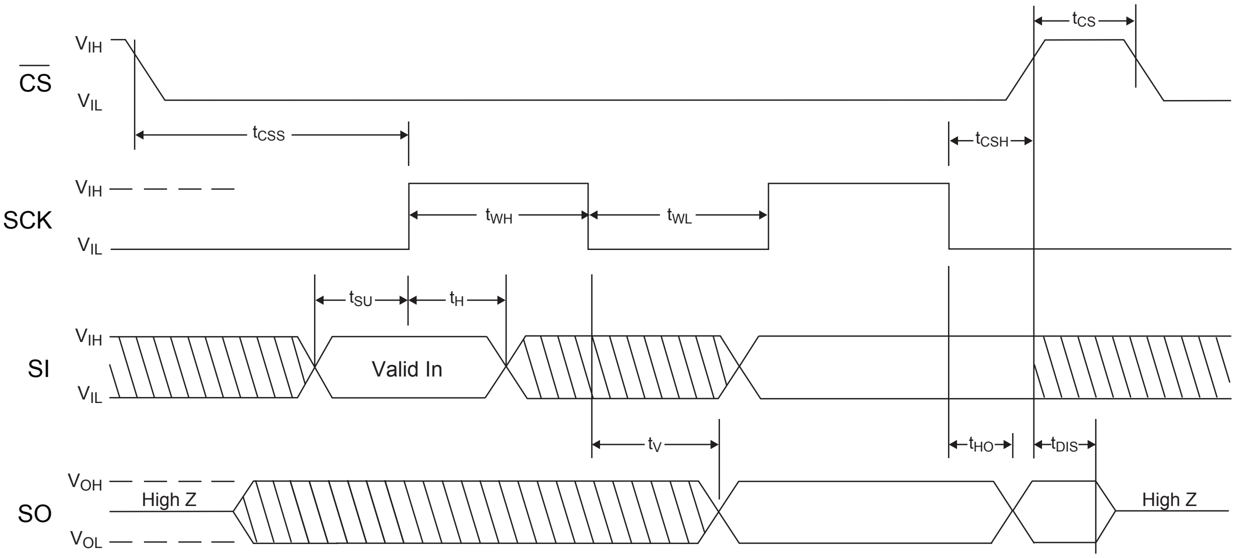


Figure 7-2. WREN Timing

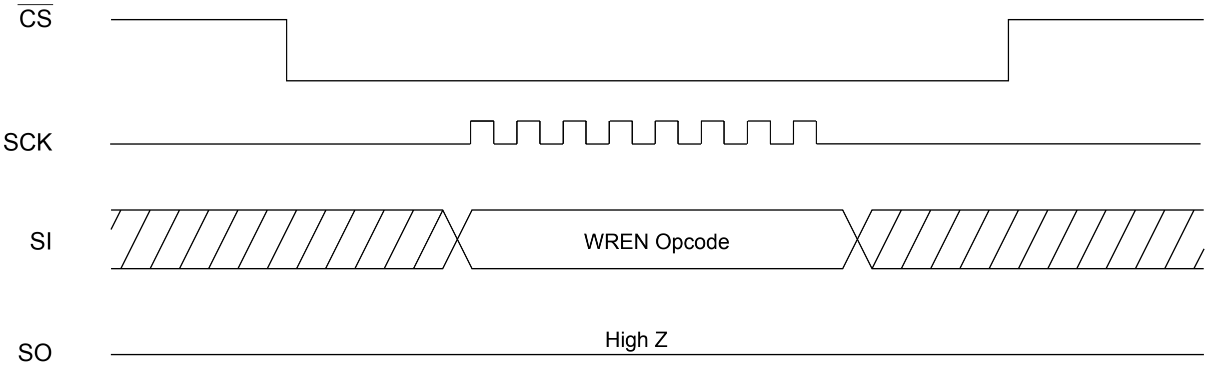


Figure 7-3. WRDI Timing

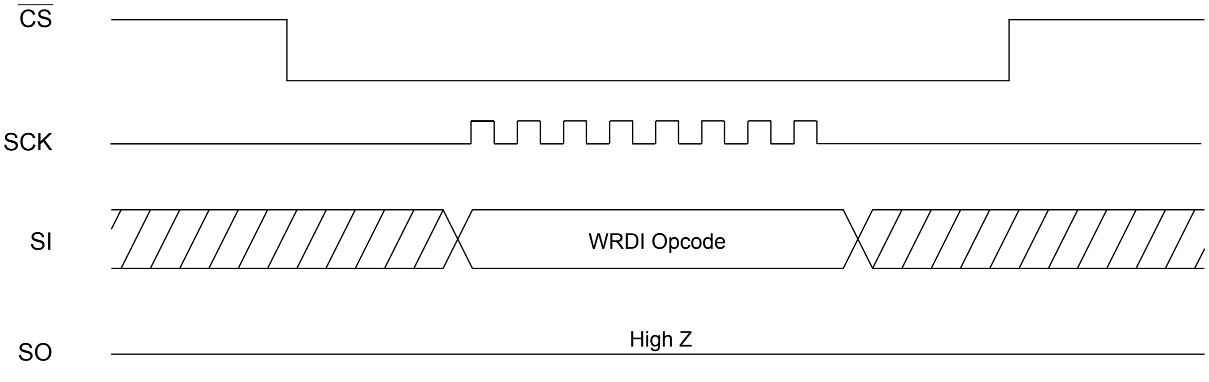


Figure 7-4. RDSR Timing

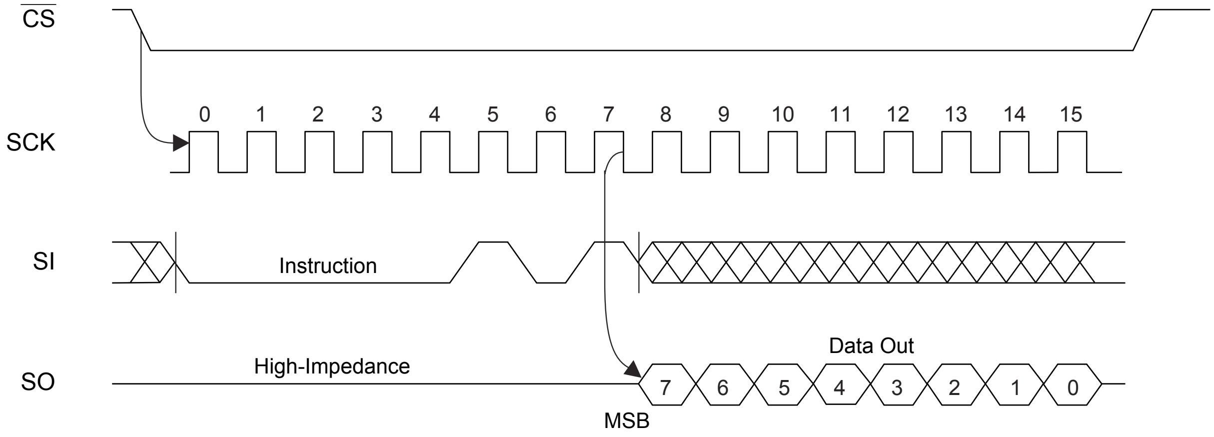
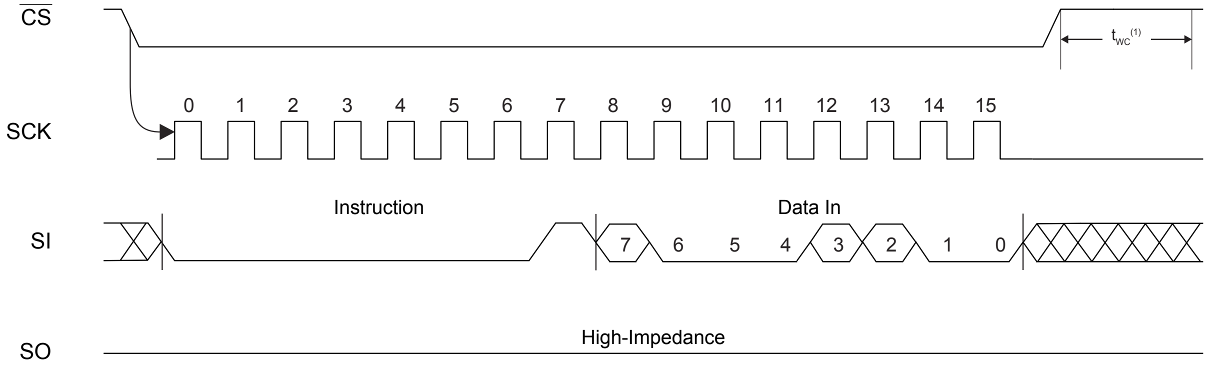


Figure 7-5. WRSR Timing



Note: This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of $\overline{CS}$ after a valid sequence.

Figure 7-6. Read Timing

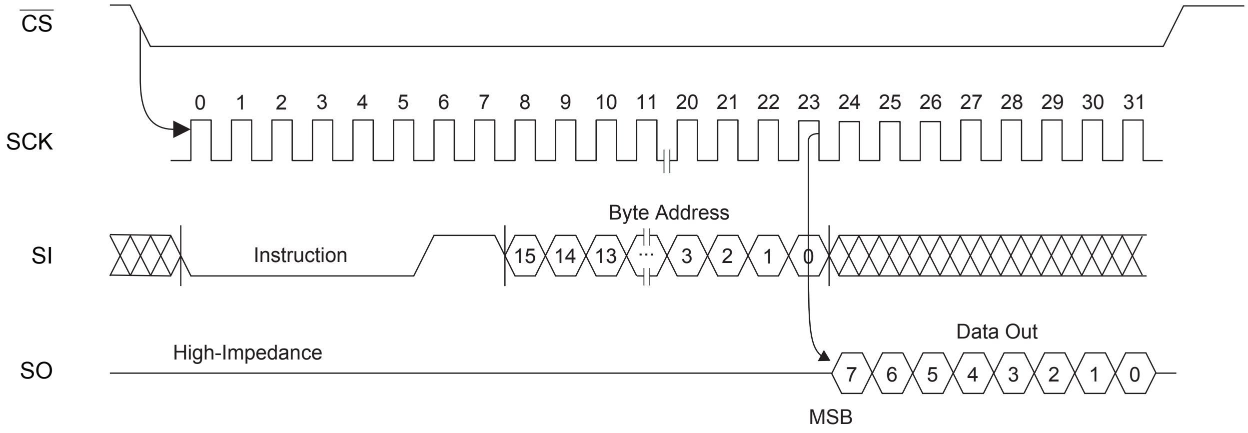
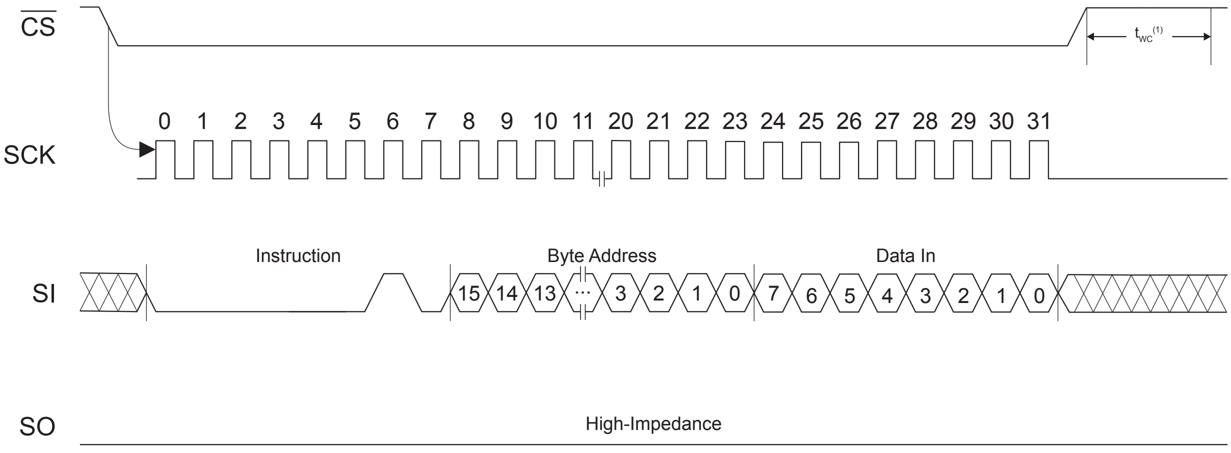
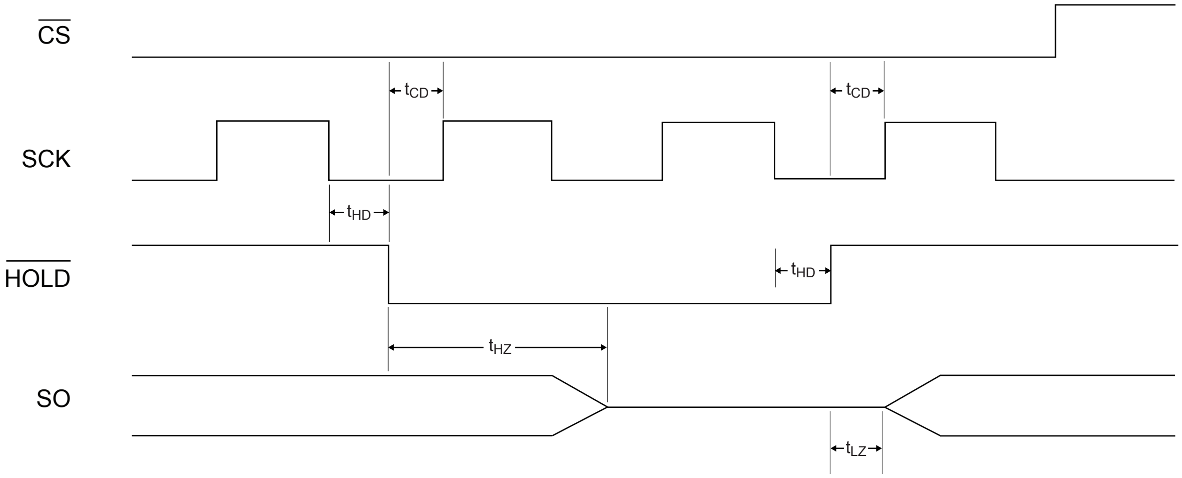


Figure 7-7. Write Timing



Note: This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of $\overline{\text{CS}}$ after a valid sequence.

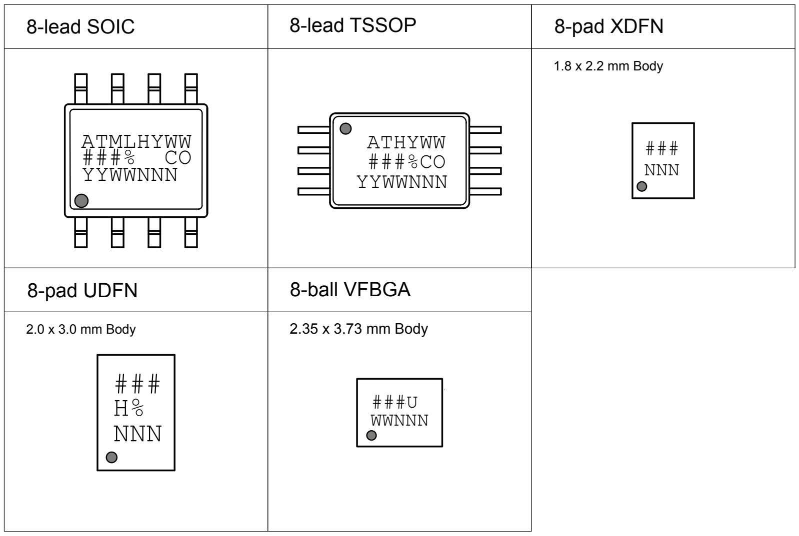
Figure 7-8. $\overline{\text{HOLD}}$ Timing



8. Packaging Information

8.1 Package Marking Information

AT25320B and AT25640B: Package Marking Information



Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

Catalog Number Truncation

AT25320B	Truncation Code ###: 5BB
AT25640B	Truncation Code ###: 5CB

Date Codes					**Voltages**
YY = Year		Y = Year		WW = Work Week of Assembly	% = Minimum Voltage
16: 2016	20: 2020	6: 2016	0: 2020	02: Week 2	L: 1.8V min
17: 2017	21: 2021	7: 2017	1: 2021	04: Week 4	
18: 2018	22: 2022	8: 2018	2: 2022	...	
19: 2019	23: 2023	9: 2019	3: 2023	52: Week 52	

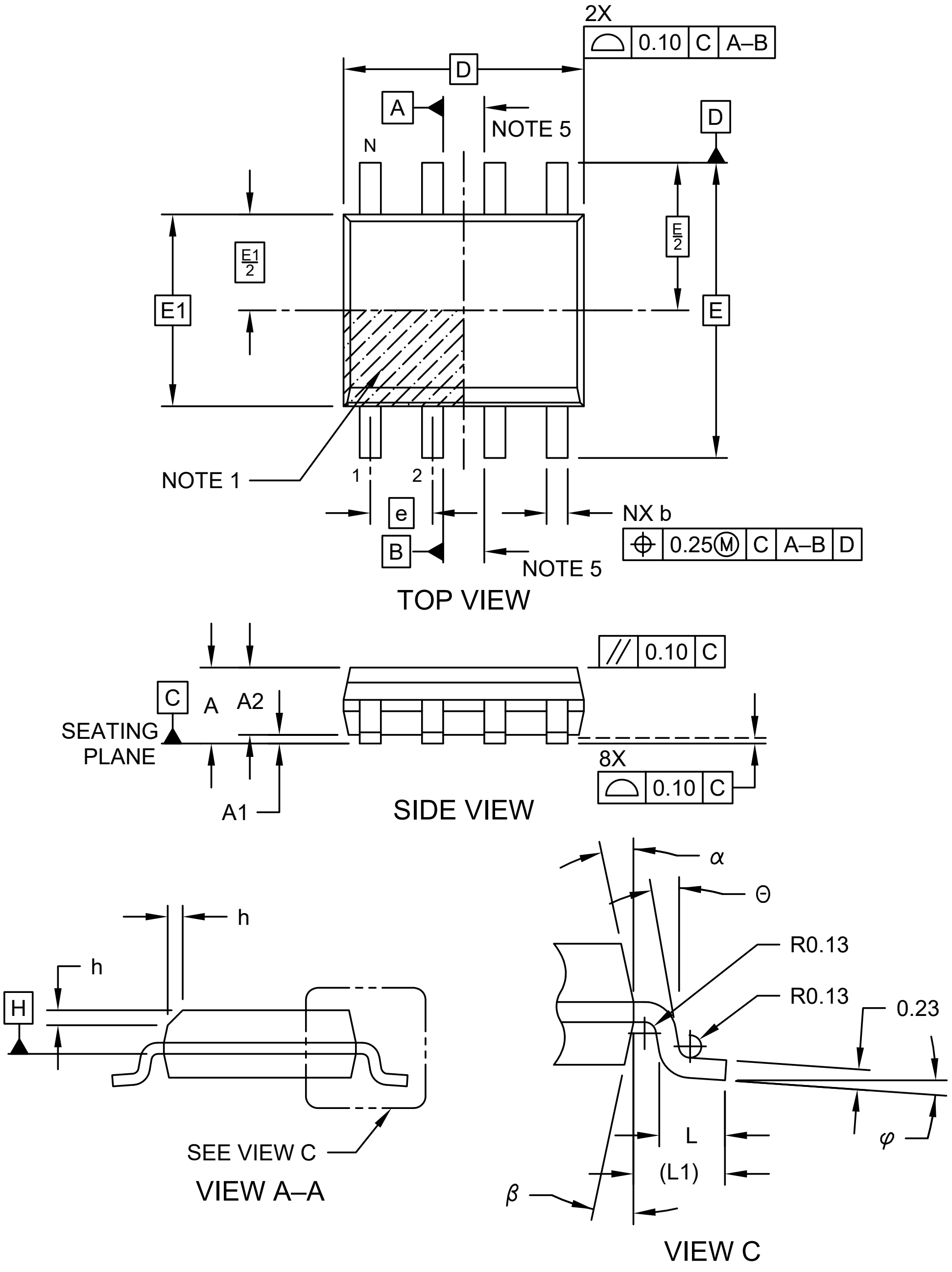
Country of Origin	**Device Grade**	**Atmel Truncation**
CO = Country of Origin	H or U: Industrial Grade	AT: Atmel ATM: Atmel ATML: Atmel

Lot Number or Trace Code

NNN = Alphanumeric Trace Code (2 Characters for Small Packages)

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

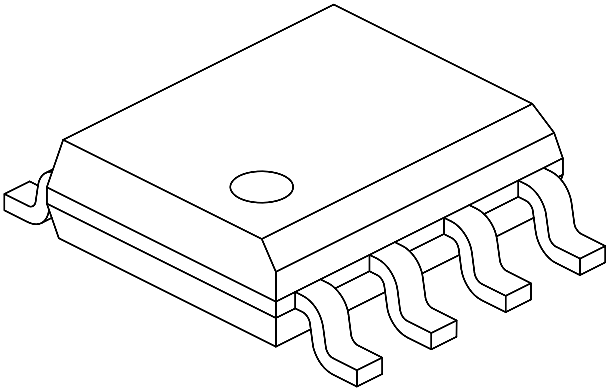
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

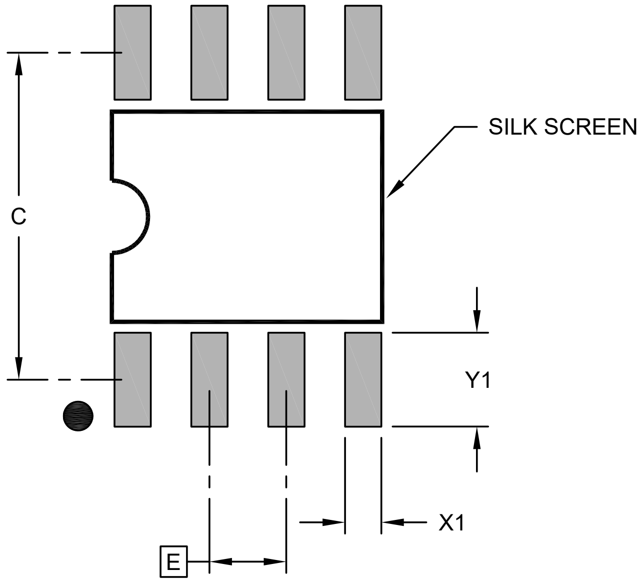
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

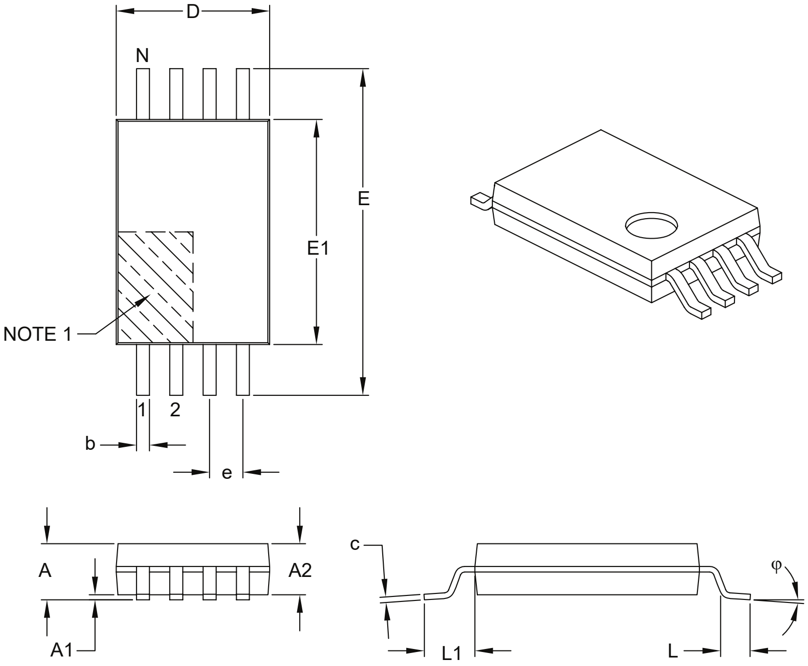
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

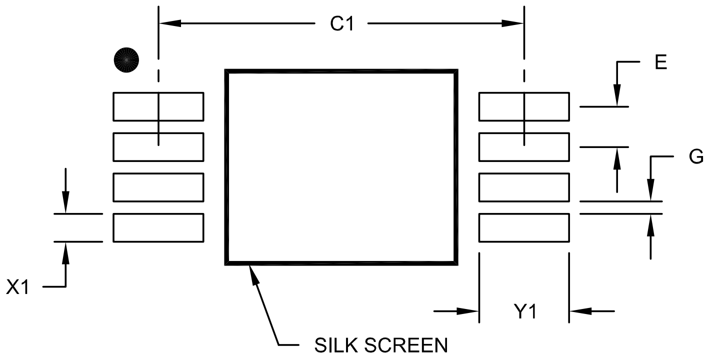
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

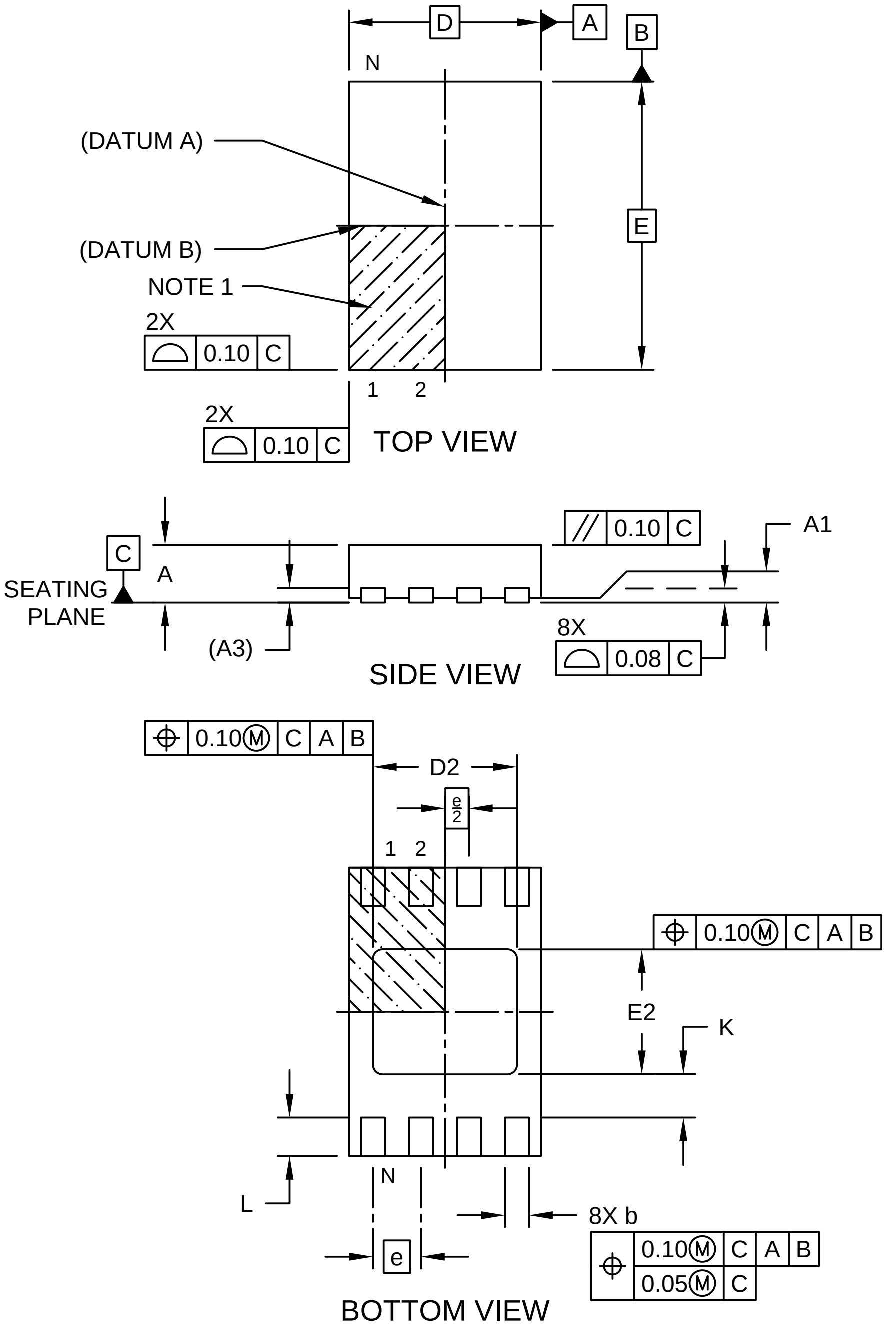
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy YNZ Package

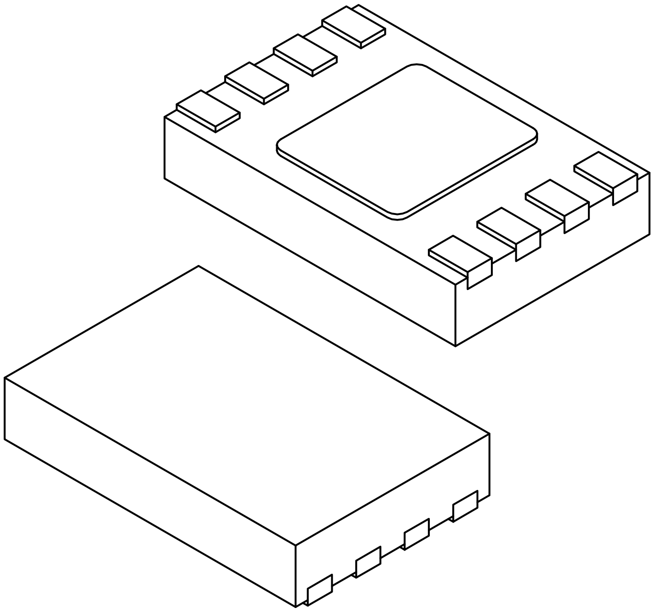
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21355-Q4B Rev A Sheet 1 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy YNZ Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

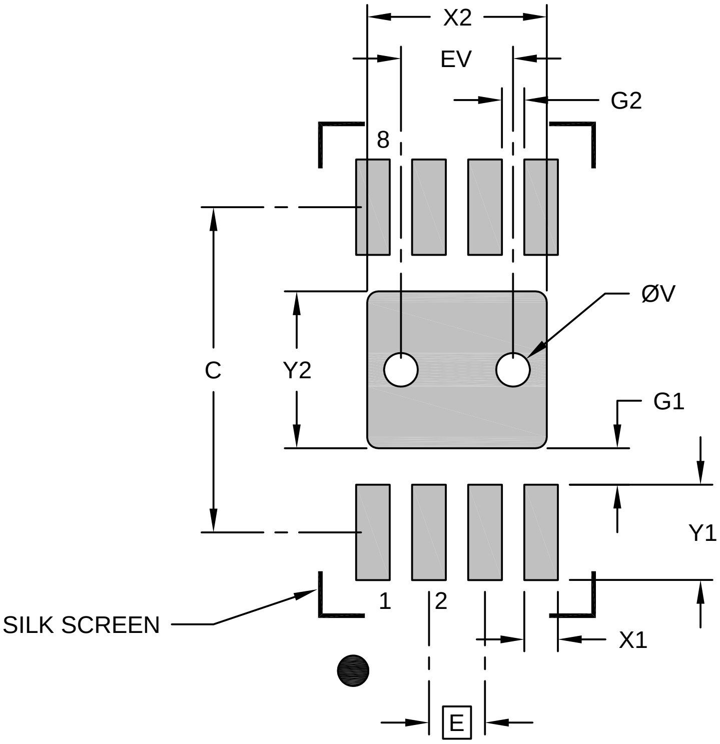
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev A Sheet 2 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy YNZ Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

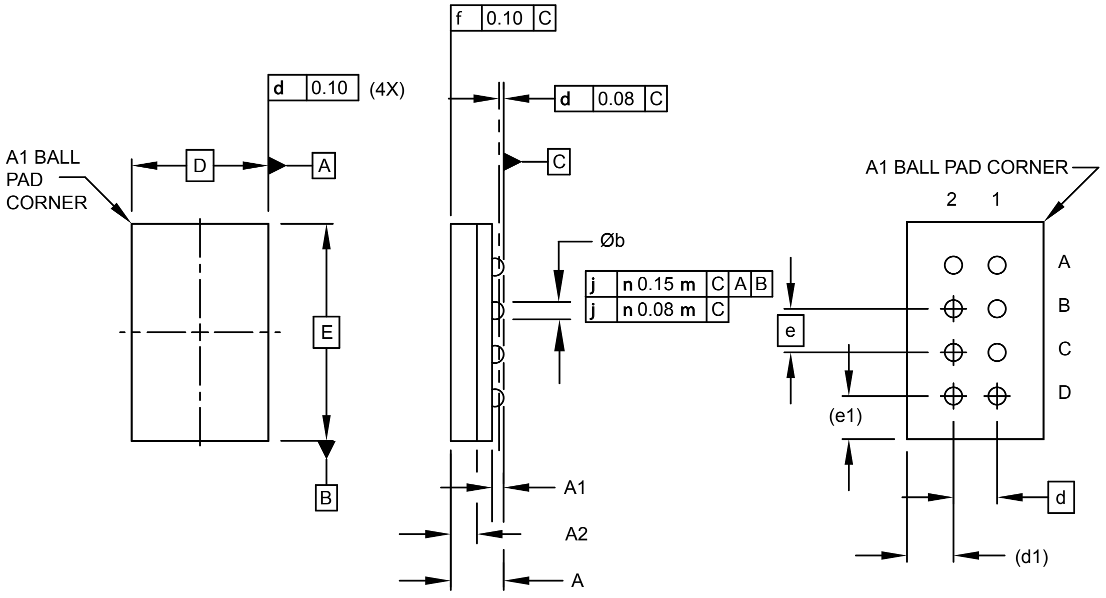
	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.33		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-21355-Q4B Rev A



TOP VIEW

SIDE VIEW

BOTTOM VIEW

8 SOLDER BALLS

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.81	0.91	1.00	
A1	0.15	0.20	0.25	
A2	0.40	0.45	0.50	
b	0.25	0.30	0.35	
D		2.35 BSC		
E		3.73 BSC		
e		0.75 BSC		
e1		0.74 REF		
d		0.75 BSC		
d1		0.80 REF		

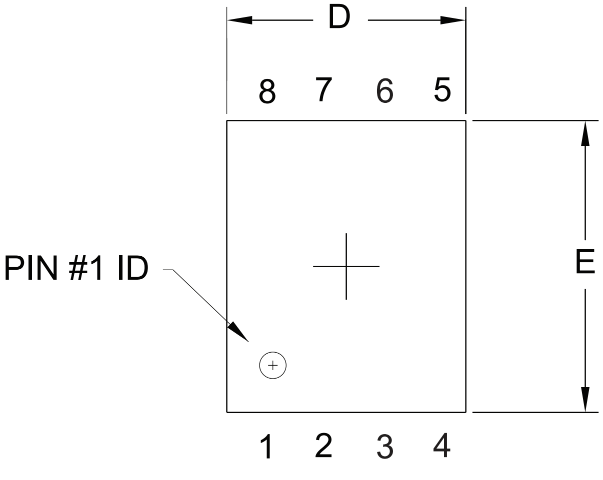
Notes:

1. This drawing is for general
2. Dimension 'b' is measured at the maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

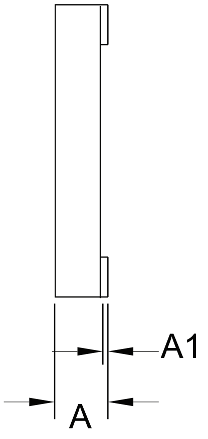
6/11/13

	TITLE	GPC	DRAWING NO.	REV.
	8U2-1, 8-ball, 2.35 x 3.73 mm Body, 0.75 mm pitch, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)	GWW	8U2-1	G

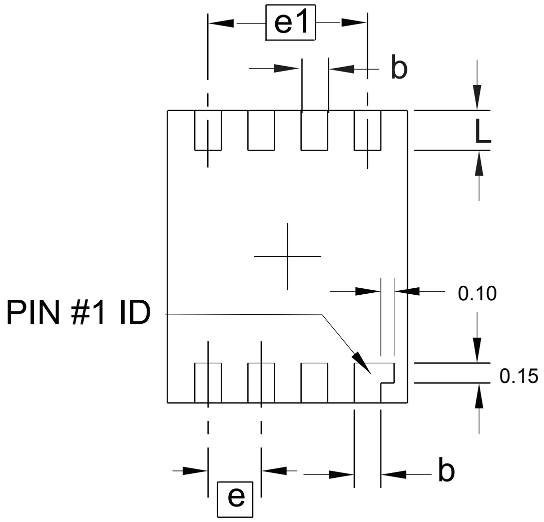
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



Top View



Side View



End View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.40	
A1	0.00	–	0.05	
D	1.70	1.80	1.90	
E	2.10	2.20	2.30	
b	0.15	0.20	0.25	
e	0.40 TYP			
e1	1.20 REF			
L	0.26	0.30	0.35	

9/10/2012

	TITLE	GPC	DRAWING NO.	REV.
	8ME1, 8-pad (1.80mm x 2.20mm body) Extra Thin DFN (XDFN)	DTP	8ME1	B

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

9. Revision History

Atmel Document 8535 Revision A (April 2008)
Initial document release.

Atmel Document 8535 Revision B (July 2008)
Modified ‘Endurance’ parameter on page 6.

Atmel Document 8535 Revision C (May 2009)
Added Part Marking information; changed to Preliminary status.

Atmel Document 8535 Revision D (August 2009)
Changed Catalog Numbering. Added new Part Marking Information.

Atmel Document 8535 Revision E (April 2010)
Updated Ordering Code Detail, Ordering Information, template.

Atmel Document 8535 Revision F (June 2010)
Updated 8A2 and 8S1 package drawings. Remove Preliminary.

Atmel Document 8535 Revision G (November 2012)
Updated part markings to single page part marking. Updated package drawings. Replaced 8A2 package with 8X package. Update template and Atmel logos.

Atmel Document 8535 Revision H (January 2015)
Added the UDFN Expanded Quantity Option. Updated the 8X, 8MA2, and 8ME1 package outline drawings and the ordering information.

Revision A (June 2018)
Updated to the Microchip template. Microchip DS20005993A replaces Atmel document 8535. Updated Part Marking Information. Added ESD rating. Removed lead finish designation. Added POR recommendations section. Updated trace code format in package markings. Updated section content throughout for clarification. Updated the SOIC, TSSOP, and UDFN package drawings to the Microchip equivalents.

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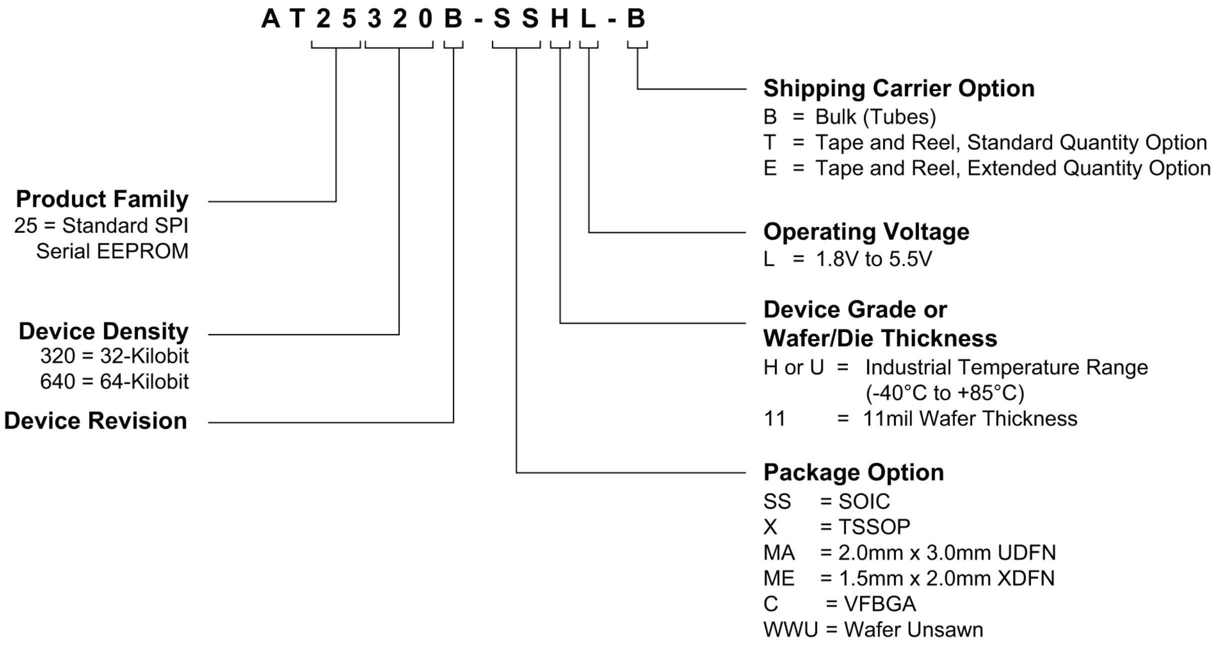

A T 2 5 3 2 0 B - S S H L - B

Shipping Carrier Option
B = Bulk (Tubes)
T = Tape and Reel, Standard Quantity Option
E = Tape and Reel, Extended Quantity Option

Product Family
25 = Standard SPI Serial EEPROM

Operating Voltage
L = 1.8V to 5.5V

Device Grade or Wafer/Die Thickness
H or U = Industrial Temperature Range (-40°C to +85°C)
11 = 11mil Wafer Thickness

Device Density
320 = 32-Kilobit
640 = 64-Kilobit

Device Revision

Package Option
SS = SOIC
X = TSSOP
MA = 2.0mm x 3.0mm UDFN
ME = 1.5mm x 2.0mm XDFN
C = VFBGA
WWU = Wafer Unsawn

Examples:

Device	Package	Package Drawing Code	Package Option	Shipping Carrier Option	Device Grade
AT25320B-SSHL-B	SOIC	SN	SS	Bulk (Tubes)	Industrial Temperature (-40°C to 85°C)
AT25320B-SSHL-T	SOIC	SN	SS	Tape and Reel	
AT25640B-SSHL-T	SOIC	SN	SS	Tape and Reel	
AT25320B-XHL-B	TSSOP	ST	X	Bulk (Tubes)	
AT25640B-XHL-T	TSSOP	ST	X	Tape and Reel	
AT25320B-MAHL-E	UDFN	Q4B	MA	Tape and Reel	
AT25640B-MAHL-T	UDFN	Q4B	MA	Tape and Reel	
AT25640B-MAHL-E	UDFN	Q4B	MA	Tape and Reel	
AT25640B-CUL-T	VFBGA	8U2-1	C	Tape and Reel	
AT25320B-MEHL-T	XDFN	8ME1	ME	Tape and Reel	

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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