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REVISION HISTORY

2/12—Rev. A to Rev. B

Created Hyperlink for Safety and Regulatory Approvals Entry in Features Section 1
Change to Printed Circuit Board (PCB) Layout Section 8

1/10—Revision A: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Quiescent Supply Current per Channel	$I_{DDI (Q)}$		0.4	0.7	mA	
Output Quiescent Supply Current per Channel	$I_{DDO (Q)}$		0.3	0.5	mA	
Total Supply Current, Five Channels[1]						
V_{DD1} Supply Current, Quiescent	$I_{DD1 (Q)}$		2.0	3.5	mA	$V_{IA} = V_{IB} = V_{IC} = V_{ID} = V_{IE}$ = 0 V
V_{DD2} Supply Current, Quiescent	$I_{DD2 (Q)}$		1.5	2.5	mA	$V_{IA} = V_{IB} = V_{IC} = V_{ID} = V_{IE}$ = 0 V
V_{DD1} Supply Current, 10 Mbps Data Rate	$I_{DD1 (10)}$		7.7	10	mA	5 MHz logic signal frequency
V_{DD2} Supply Current, 10 Mbps Data Rate	$I_{DD2 (10)}$		3.3	4.0	mA	5 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{IE}	−10	+1	+10	μA	V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{IE} ≥ 0 V
Logic High Input Threshold	V_{IH}			2.0	V	
Logic Low Input Threshold	V_{IL}	0.8			V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}, V_{OEH}	V_{DD2} − 0.4	4.8		V	I_{Ox} = −4 mA, $V_{Ix} = V_{IH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}, V_{OEL}		0.2	0.4	V	I_{Ox} = +4 mA, $V_{Ix} = V_{IL}$
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	27	40	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			5	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			30	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}			5	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	10	15		kV/μs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	10	15		kV/μs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.14		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.045		mA/Mbps	

[1] Supply current values are for all five channels combined, running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel, operating at a given data rate, can be calculated as described in the Power Consumption section. See Figure 4 through Figure 6 for information on the per-channel supply current as a function of the data rate for unloaded and loaded conditions. See Figure 7 and Figure 8 for total I_{DD1} and I_{DD2} supply currents as a function of the data rate for the ADuM7510.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed. Operation below the minimum pulse width is not recommended.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels within the same component.

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V \times V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 4 through Figure 6 for information on the per-channel supply current as a function of the data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[2]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance, QSOP	θ_{JA}		76		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device. Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 3.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		1000	V rms	1 minute duration
Minimum External Air Gap QSOP Package (Clearance)	L(I01)	3.8 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking QSOP Package (Creepage)	L(I02)	3.8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)
Maximum Working Voltage Compatible with 50 Years Service Life	V_{IORM}	354	V peak	Continuous peak voltage across the isolation barrier

RECOMMENDED OPERATING CONDITIONS

All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

Table 4.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V
Input Signal Rise and Fall Times			1.0	ms

REGULATORY INFORMATION

The ADuM7510 is approved by the organization listed in Table 5.

Table 5.

UL (Pending)
Recognized under UL 1577 component recognition program[1]
Single/basic insulation, 1000 V rms isolation voltage
File E214100

[1] In accordance with UL 1577, each ADuM7510 is proof tested by applying an insulation test voltage of 1200 V rms for 1 sec (current leakage detection limit = 5 µA).

ABSOLUTE MAXIMUM RATINGS

Ambient temperature T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +105°C
Supply Voltages[1] (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages[1] (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{IE})	−0.5 V to V_{DDI} + 0.5 V
Output Voltages[1] (V_{OA}, V_{OB}, V_{OC}, V_{OD}, V_{OE})	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[2]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[3]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] See Figure 3 for maximum rated current values for various temperatures.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

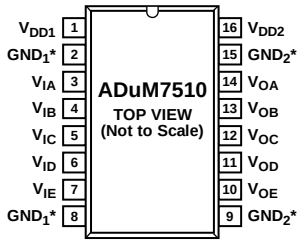


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1 (4.5 V to 5.5 V).
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	V_{IE}	Logic Input E.
8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
9	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
10	V_{OE}	Logic Output E.
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
16	V_{DD2}	Supply Voltage for Isolator Side 2 (4.5 V to 5.5 V).

Table 8. Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	V_{DD1} State	V_{DD2} State	V_{Ox} Output[1]	Description
High	Powered	Powered	High	Normal operation, data is high.
Low	Powered	Powered	Low	Normal operation, data is low.
X	Unpowered	Powered	Low	Input unpowered. Outputs return to input state within 1 µs of V_{DD1} power restoration. See the Power-Up/Power-Down Considerations section for more details.
X	Powered	Unpowered	High-Z	Output unpowered. Output pins are in high impedance state. Outputs return to input state within 1 µs of V_{DD2} power restoration.

[1] V_{IX} and V_{OX} refer to the input and output signals of a given channel (A, B, C, D, or E).
[2] X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

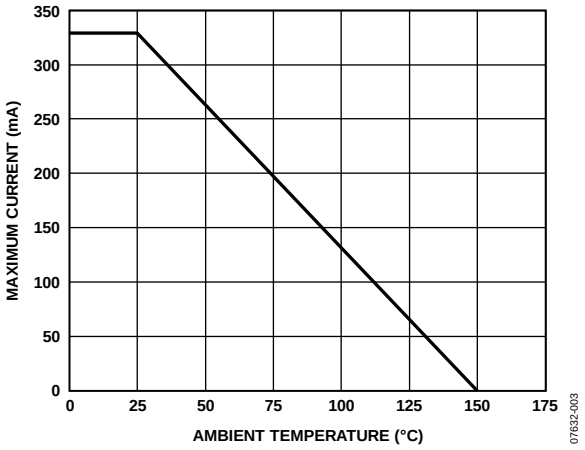


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

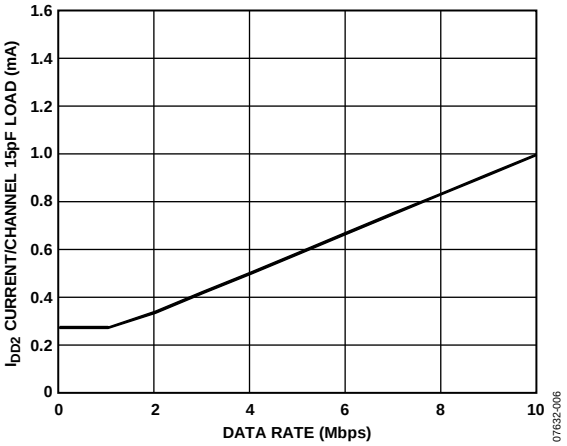


Figure 6. Typical I_{DD2} Supply Current per Channel vs. Data Rate (15 pF Output Load)

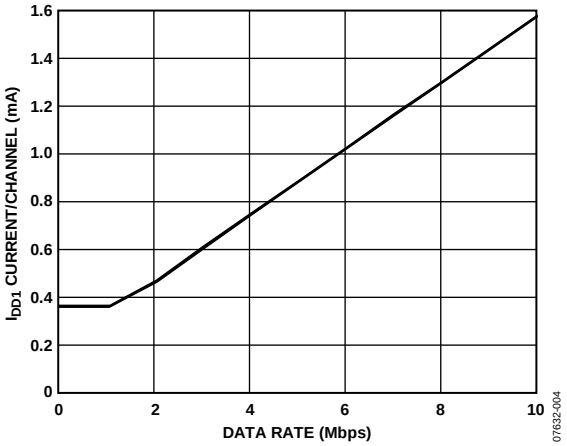


Figure 4. Typical I_{DD1} Supply Current per Channel vs. Data Rate

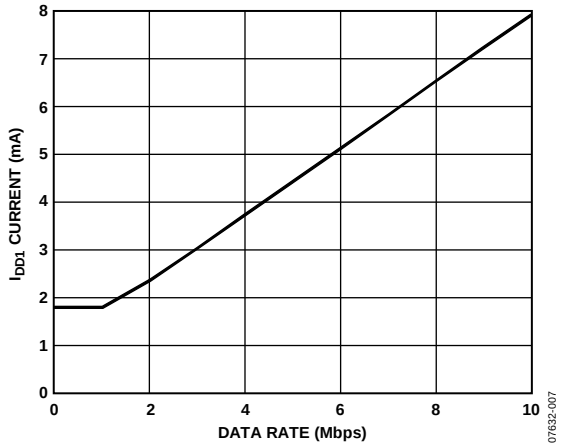


Figure 7. Typical Total I_{DD1} Supply Current vs. Data Rate

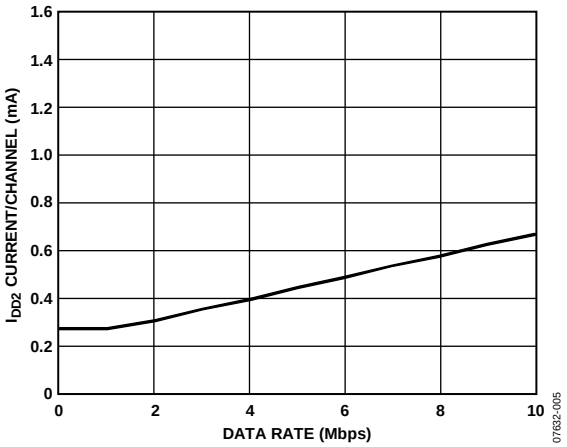


Figure 5. Typical I_{DD2} Supply Current per Channel vs. Data Rate (No Output Load)

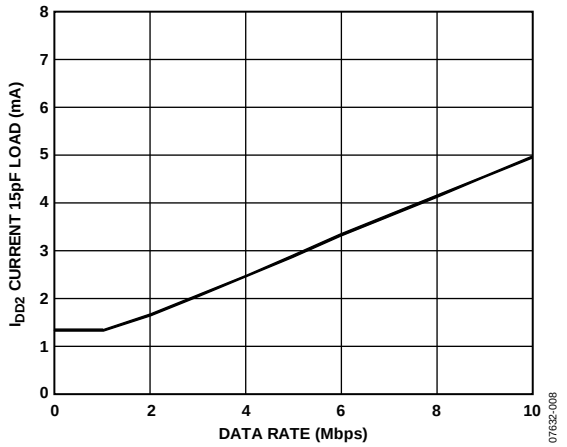


Figure 8. Typical Total I_{DD2} Supply Current vs. Data Rate (15 pF Output Load)

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM7510 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 9). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 10 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side is connected close to the package.

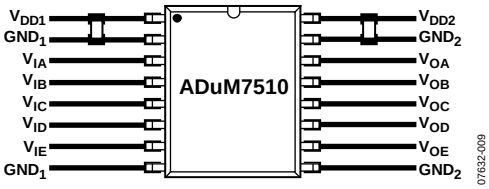


Figure 9. Recommended PCB Layout

See the AN-1109 Application Note for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the length of time it takes for a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

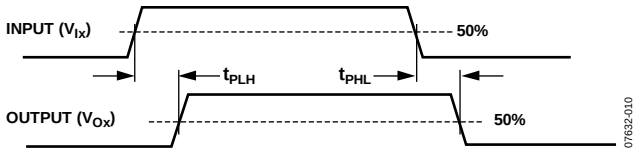


Figure 10. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM7510 component.

Propagation delay skew refers to the maximum amount the propagation delay differs among multiple ADuM7510 components operated under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is, therefore, either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output.

If the decoder receives no pulses for more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default low state by the watchdog timer circuit (see Table 8).

The limitation on the magnetic field immunity of the device is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines such conditions. The ADuM7510 is examined in a 4.5 V operating condition because it represents the most susceptible mode of operation of this product.

The pulses at the transformer output have an amplitude greater than 1.5 V. The decoder has a sensing threshold of about 1.0 V, thereby establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\Pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density.
r_n is the radius of the n^{th} turn in the receiving coil.
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM7510 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 11.

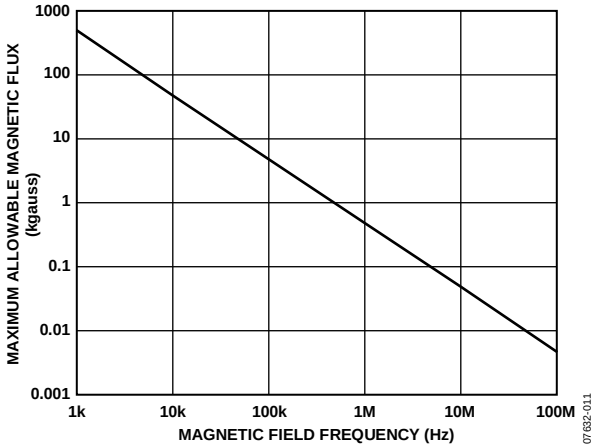


Figure 11. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs with the worst-case polarity during a transmitted pulse, it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM7510 transformers. Figure 12 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM7510 is very insensitive to external fields. Only extremely large, high frequency currents, very close to the component can potentially be a concern. For the 1 MHz example noted, a 1.2 kA current must be placed 5 mm away from the ADuM7510 to affect component operation.

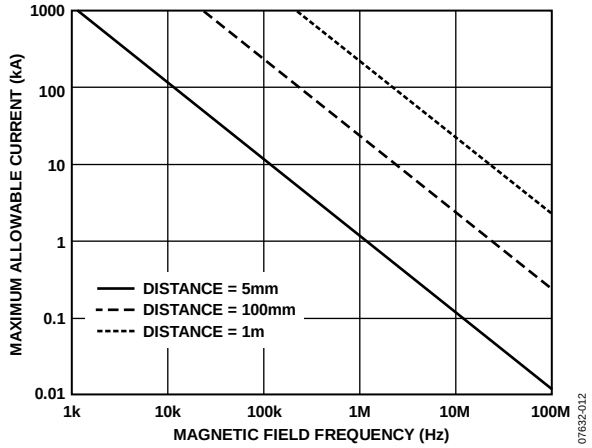


Figure 12. Maximum Allowable Current for Various Current to ADuM7510 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Take care to avoid PCB structures that form loops.

POWER CONSUMPTION

The supply current at a given channel of the ADuM7510 isolator is a function of the supply voltage, the channel data rate, and the channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f \le 0.5f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 4 and Figure 5 provide per-channel supply currents as a function of the data rate for an unloaded output condition. Figure 6 provides per-channel supply current as a function of the data rate for a 15 pF output condition. Figure 7 and Figure 8 provide total I_{DD1} and I_{DD2} supply current as a function of the data rate for ADuM7510 products.

POWER-UP/POWER-DOWN CONSIDERATIONS

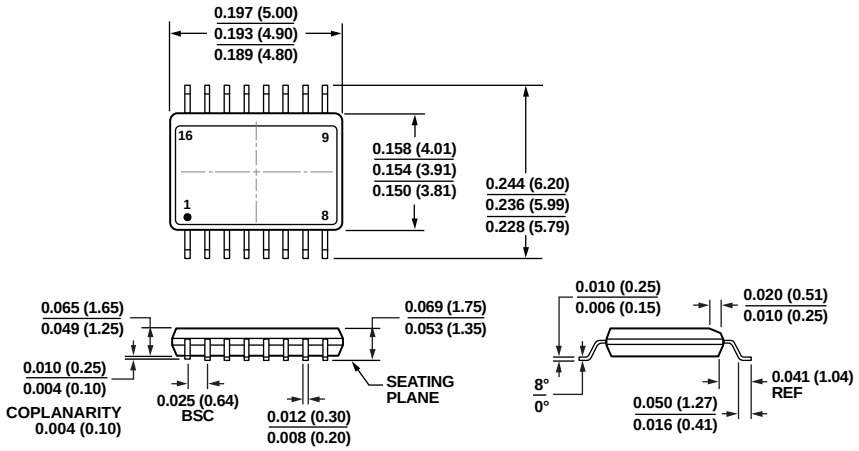
The ADuM7510 behaves as specified in Table 8 during power-up and power-down operations. However, the part can transfer incorrect data when the power supplies are below the minimum operating voltage but the internal circuits are not completely off.

Power-up/power-down errors can occur at V_{DDx} voltage near the operating threshold of 1.9 V. The encoder generates data pulses at low amplitude. The detector can miss data pulses that are near the detection threshold. If the transferring state is a logic high, the encoder generates a pair of pulses; the decoder can reject one of the pulses for low amplitude. A single pulse is interpreted as a logic low, and the output can be placed in the wrong logic state for that refresh cycle.

Glitch-free operation is possible by following these recommendations.

- Slew the power on or off as quickly as possible.
- Use the default low operating mode by holding the inputs low until power is stable.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

01-28-2008-A

Figure 13. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1, 2]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate	Maximum Propagation Delay, 5 V	Maximum Pulse Width Distortion	Temperature Range	Package Description	Package Option
ADuM7510BRQZ	5	0	10 Mbps	40 ns	5 ns	−40°C to +105°C	16-Lead QSOP	RQ-16
ADuM7510BRQZ-RL7	5	0	10 Mbps	40 ns	5 ns	−40°C to +105°C	16-Lead QSOP	RQ-16

[1] Z = RoHS Compliant Part.
[2] RL7 = 7″ tape and reel option.

NOTES

NOTES

D07632-0-2/12(B)