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REVISION HISTORY

10/2018—Rev. A to Rev. B

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4/2016—Rev. 0 to Rev. A

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10/2015—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.8	7.2	13	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	3	ns	$\|t_{PLH} − t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.1	ns	Between any two devices at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.5	3.0	ns	
Opposing Direction	t_{PSKOD}		0.5	3.0	ns	
Jitter			630		ps p-p	See the Jitter Measurement section
			80		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 µA, V_{Ix} = V_{IxH}[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −4 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 µA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 4 mA, V_{Ix} = V_{IxL}[4]
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−3		µA	V_{E2} = 0 V
$DISABLE_1$ Input Pull-Down Current	I_{PD}		9	15	µA	$DISABLE_1$ = V_{DDx}
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	µA	0 V ≤ V_{Ox} ≤ V_{DDx}
Quiescent Supply Current						
ADuM230D/ADuM230E						
	$I_{DD1 (Q)}$		1.35	2.6	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.73	2.9	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		9.7	15.2	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.87	3.0	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM231D/ADuM231E						
	$I_{DD1 (Q)}$		1.62	2.7	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.61	2.8	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		7.4	11.4	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		5.34	7.2	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.02		mA/Mbps	Inputs switching, 50% duty cycle

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\|CM_H\|$	75	100		kV/μs	$V_{Ix} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/μs	$V_{Ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

[1] 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.
[2] I_{Ox} is the Channel x output current, where x = A, B, or C.
[3] V_{IxH} is the input side logic high.
[4] V_{IxL} is the input side logic low.
[5] V_I is the voltage input.
[6] E0 refers to the ADuM230E0/ADuM231E0 models, D0 refers to the ADuM230D0/ADuM231D0 models, E1 refers to the ADuM230E1/ADuM231E1 models, and D1 refers to the ADuM230D1/ADuM231D1 models. See the Ordering Guide section.
[7] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_{Ox}) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM230D/ADuM230E											
Supply Current Side 1	I_{DD1}		5.6	9.0		6.3	9.8		9.4	14.3	mA
Supply Current Side 2	I_{DD2}		1.9	3.7		3.1	4.9		6.8	10	mA
ADuM231D/ADuM231E											
Supply Current Side 1	I_{DD1}		4.6	7.2		5.5	8.3		8.8	11.9	mA
Supply Current Side 2	I_{DD2}		3.6	5.8		4.6	6.8		8.0	11.3	mA

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at $T_A = 25°C$, $V_{DD1} = V_{DD2} = 3.3$ V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.8	6.8	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.5	ns	Between any two devices at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			640		ps p-p	See the Jitter Measurement section
			75		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	$0.7 \times V_{DDx}$			V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic Low	V_{IL}			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	I_{Ox}[2] $= -20$ µA, $V_{Ix} = V_{IxH}$[3]
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	I_{Ox}[2] $= -2$ mA, $V_{Ix} = V_{IxH}$[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] $= 20$ µA, $V_{Ix} = V_{IxL}$[4]
			0.2	0.4	V	I_{Ox}[2] $= 2$ mA, $V_{Ix} = V_{IxL}$[4]
Input Current per Channel	I_I	−10	+0.01	+10	µA	$0\ V \leq V_{Ix} \leq V_{DDx}$
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−3		µA	$V_{E2} = 0$ V
$DISABLE_1$ Input Pull-Down Current	I_{PD}		9	15	µA	$DISABLE_1 = V_{DDx}$
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	µA	$0\ V \leq V_{Ox} \leq V_{DDx}$
Quiescent Supply Current						
ADuM230D/ADuM230E						
	$I_{DD1\ (Q)}$		1.25	2.5	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2\ (Q)}$		1.65	2.8	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1\ (Q)}$		9.57	15.0	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2\ (Q)}$		1.79	2.9	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM231D/ADuM231E						
	$I_{DD1\ (Q)}$		1.52	2.6	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2\ (Q)}$		1.52	2.6	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1\ (Q)}$		7.28	11.3	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2\ (Q)}$		5.24	7.1	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	$V_{Ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

1 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.
2 I_{Ox} is the Channel x output current, where x = A, B, or C.
3 V_{IxH} is the input side logic high.
4 V_{IxL} is the input side logic low.
5 V_I is the voltage input.
6 E0 refers to the ADuM230E0/ADuM231E0 models, D0 refers to the ADuM230D0/ADuM231D0 models, E1 refers to the ADuM230E1/ADuM231E1 models, and D1 refers to the ADuM230D1/ADuM231D1 models. See the Ordering Guide section.
7 $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_{Ox}) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM230D/ADuM230E											
Supply Current Side 1	I_{DD1}		5.4	8.8		6.0	9.4		8.5	12.7	mA
Supply Current Side 2	I_{DD2}		1.8	3.6		2.9	4.7		6.2	8.4	mA
ADuM231D/ADuM231E											
Supply Current Side 1	I_{DD1}		4.4	7.1		5.2	8.0		8.1	10.7	mA
Supply Current Side 2	I_{DD2}		3.4	5.6		4.3	6.5		7.4	9.5	mA

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range: 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.0	7.0	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.8	ns	Between any two devices at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			770		ps p-p	See the Jitter Measurement section
			160		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 µA, $V_{Ix} = V_{IxH}$[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −2 mA, $V_{Ix} = V_{IxH}$[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 µA, $V_{Ix} = V_{IxL}$[4]
			0.2	0.4	V	I_{Ox}[2] = 2 mA, $V_{Ix} = V_{IxL}$[4]
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−3		µA	V_{E2} = 0 V
$DISABLE_1$ Input Pull-Down Current	I_{PD}		9	15	µA	$DISABLE_1 = V_{DDx}$
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	µA	0 V ≤ V_{Ox} ≤ V_{DDx}
Quiescent Supply Current						
ADuM230D/ADuM230E						
	$I_{DD1 (Q)}$		1.2	2.4	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.61	2.7	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		9.52	14.9	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.76	2.8	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM231D/ADuM231E						
	$I_{DD1 (Q)}$		1.47	2.5	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.48	2.5	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		7.23	11.2	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		5.19	7.0	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.
[2] I_{Ox} is the Channel x output current, where x = A, B, or C.
[3] V_{IxH} is the input side logic high.
[4] V_{IxL} is the input side logic low.
[5] V_I is the voltage input.
[6] E0 refers to the ADuM230E0/ADuM231E0 models, D0 refers to the ADuM230D0/ADuM231D0 models, E1 refers to the ADuM230E1/ADuM231E1 models, and D1 refers to the ADuM230D1/ADuM231D1 models. See the Ordering Guide section.
[7] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_{Ox}) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM230D/ADuM230E											
Supply Current Side 1	I_{DD1}		5.3	8.7		5.9	9.3		8.2	12.3	mA
Supply Current Side 2	I_{DD2}		1.8	3.6		2.6	4.4		5.2	7.4	mA
ADuM231D/ADuM231E											
Supply Current Side 1	I_{DD1}		4.4	7.1		5.0	7.8		7.5	10.1	mA
Supply Current Side 2	I_{DD2}		3.4	5.6		4.1	6.3		6.6	8.7	mA

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

All typical specifications are at T_A = 25°C, $V_{DD1} = V_{DD2}$ = 1.8 V. Minimum/maximum specifications apply over the entire recommended operation range: 1.7 V ≤ V_{DD1} ≤ 1.9 V, 1.7 V ≤ V_{DD2} ≤ 1.9 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.8	8.7	15	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\|t_{PLH} − t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.0	ns	Between any two devices at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			600		ps p-p	See the Jitter Measurement section
			90		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage						
Logic High	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	I_{Ox}[2] = −20 µA, $V_{Ix} = V_{IxH}$[3]
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	I_{Ox}[2] = −2 mA, $V_{Ix} = V_{IxH}$[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 µA, $V_{Ix} = V_{IxL}$[4]
			0.2	0.4	V	I_{Ox}[2] = 2 mA, $V_{Ix} = V_{IxL}$[4]
Input Current per Channel	I_I	−10	+0.01	+10	µA	$0 V \leq V_{Ix} \leq V_{DDx}$
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−3		µA	V_{E2} = 0 V
$DISABLE_1$ Input Pull-Down Current	I_{PD}		9	15	µA	$DISABLE_1 = V_{DDx}$
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	µA	$0 V \leq V_{Ox} \leq V_{DDx}$
Quiescent Supply Current						
ADuM230D/ADuM230E						
	$I_{DD1 (Q)}$		1.15	2.3	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.58	2.6	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		9.41	14.8	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.72	2.7	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM231D/ADuM231E						
	$I_{DD1 (Q)}$		1.42	2.4	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.44	2.4	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		7.15	11.1	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		5.13	6.9	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.
[2] I_{Ox} is the Channel x output current, where x = A, B, or C.
[3] V_{IxH} is the input side logic high.
[4] V_{IxL} is the input side logic low.
[5] V_I is the voltage input.
[6] E0 refers to the ADuM230E0/ADuM231E0 models, D0 refers to the ADuM230D0/ADuM231D0 models, E1 refers to the ADuM230E1/ADuM231E1 models, and D1 refers to the ADuM230D1/ADuM231D1 models. See the Ordering Guide section.
[7] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_{Ox}) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 8. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM230D/ADuM230E											
Supply Current Side 1	I_{DD1}		5.2	8.6		5.8	9.3		8.1	12.2	mA
Supply Current Side 2	I_{DD2}		1.7	3.5		2.5	4.3		5.2	7.3	mA
ADuM231D/ADuM231E											
Supply Current Side 1	I_{DD1}		4.3	7.0		4.9	7.7		7.26	10.0	mA
Supply Current Side 2	I_{DD2}		3.3	5.5		4.0	6.2		6.5	8.6	mA

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 9. RW-16 Wide Body [SOIC_W] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	7.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 10. RI-16 -2 Wide Body Increased Creepage [SOIC_IC] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 11.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 17, Table 18, and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 12. RW-16 Wide Body [SOIC_W] Package

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified by CQC11-471543-2012, GB4943.1-2011
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2:	Reinforced insulation, V_{IORM} = 849 peak, V_{IOSM} = 8000 V peak	Basic insulation at 760 V rms (1075 V peak)
Double Protection, 5000 V rms Isolation Voltage	Basic insulation at 780 V rms (1103 V peak)	Basic insulation, V_{IORM} = 849 V peak, V_{IOSM} = 12 kV peak	Reinforced insulation at 380 V rms (537 V peak), tropical climate, altitude ≤ 5000 meters
	Reinforced insulation at 390 V rms (552 V peak)		
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 means of patient protection (1 MOPP)), 490 V rms (686 V peak)		
	Reinforced insulation (2 MOPP), 238 V rms (325 V peak)		
	CSA 61010-1-12 and IEC 61010-1 third edition:		
	Basic insulation at 300 V rms mains, 780 V secondary (1103 V peak)		
	Reinforced insulation at 300 V rms Mains, 390 V secondary (552 V peak)		
File E214100	File 205078	File 2471900-4880-0001	File CQC16001147385

[1] In accordance with UL 1577, each ADuM230D/ADuM230E/ADuM231D/ADuM231E is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each ADuM230D/ADuM230E/ADuM231D/ADuM231E is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

Table 13. RI-16 -2 Wide Body Increased Creepage [SOIC_IC] Package

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified by CQC11-471543-2012, GB4943.1-2011
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2:	Reinforced insulation, V_{IORM} = 849 peak, V_{IOSM} = 8000 V peak	Basic insulation at 820 V rms (1159 V peak)
Double Protection, 5000 V rms Isolation Voltage	Basic insulation at 830 V rms (1174 V peak)	Basic insulation, V_{IORM} = 849 V peak, V_{IOSM} = 12 kV peak	Reinforced insulation at 410 V rms (578 V peak), tropical climate, altitude ≤ 5000 meters
	Reinforced insulation at 415 V rms (587 V peak)		
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 means of patient protection (1 MOPP)), 519 V rms (734 V peak)		
	Reinforced insulation (2 MOPP), 261 V rms (369 V peak)		
	CSA 61010-1-12 and IEC 61010-1 third edition:		
	Basic insulation at 300 V rms mains, 830 V secondary (1174 V peak)		
	Reinforced insulation at 300 V rms Mains, 390 V secondary (587 V peak)		
File E214100	File 205078	File 2471900-4880-0001	File CQC17001171586

[1] In accordance with UL 1577, each ADuM230D/ADuM230E/ADuM231D/ADuM231E is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each ADuM230D/ADuM230E/ADuM231D/ADuM231E is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 14.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd (m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd (m)}$	1592	V peak
Input to Output Test Voltage, Method A		$V_{pd (m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd (m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd (m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1019	V peak
Highest Allowable Overvoltage		V_{IOTM}	8000	V peak
Surge Isolation Voltage Basic	$V_{PEAK} = 12.8$ kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	12,000	V peak
Surge Isolation Voltage Reinforced	$V_{PEAK} = 12.8$ kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	8000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 5)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

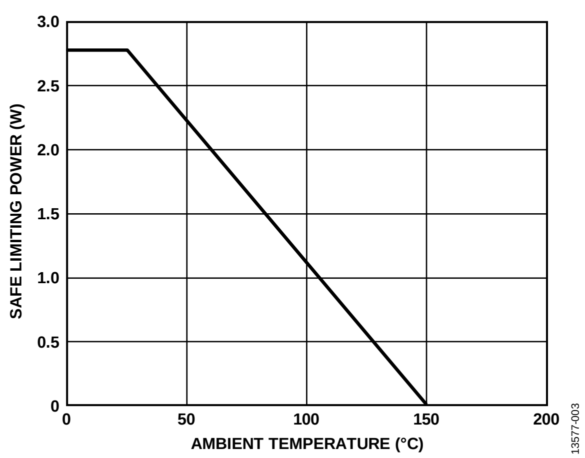


Figure 5. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 15.

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
Supply Voltages	V_{DD1}, V_{DD2}	1.7 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 16.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC}, V_{E1}, V_{E2}, $DISABLE_1$, $DISABLE_2$)[1]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB}, V_{OC})[2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−150 kV/μs to +150 kV/μs

[1] V_{DDI} is the input side supply voltage.
[2] V_{DDO} is the output side supply voltage.
[3] See Figure 5 for the maximum rated current values for various ambient temperatures.
[4] Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 17. Maximum Continuous Working Voltage[1] RW-16 Wide Body [SOIC_W] Package

Parameter	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	849 V peak	50-year minimum insulation lifetime
Reinforced Insulation	790 V peak	50-year minimum insulation lifetime
Unipolar Waveform		
Basic Insulation	1698 V peak	50-year minimum insulation lifetime
Reinforced Insulation	849 V peak	50-year minimum insulation lifetime
DC Voltage		
Basic Insulation	1118 V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Reinforced Insulation	559 V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 18. Maximum Continuous Working Voltage[1] RI-16 -2 Wide Body Increased Creepage [SOIC_IC] Package

Parameter	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	849 V peak	50-year minimum insulation lifetime
Reinforced Insulation	819 V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Unipolar Waveform		
Basic Insulation	1698 V peak	50-year minimum insulation lifetime
Reinforced Insulation	943 V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
DC Voltage		
Basic Insulation	1157 V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Reinforced Insulation	579 V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Truth Tables

Table 19. ADuM230D/ADuM231D Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	$V_{DISABLEx}$ Input[1, 2]	V_{DDI} State[2]	V_{DDO} State[2]	Default Low (D0), V_{Ox} Output[1, 2, 3]	Default High (D1), V_{Ox} Output[1, 2, 3]	Test Conditions/ Comments
L	L or NC	Powered	Powered	L	L	Normal operation
H	L or NC	Powered	Powered	H	H	Normal operation
X	H	Powered	Powered	L	H	Inputs disabled, fail-safe output
X[4]	X[4]	Unpowered	Powered	L	H	Fail-safe output
X[4]	X[4]	Powered	Unpowered	Indeterminate	Indeterminate	

[1] L means low, H means high, X means don't care, and NC means not connected.
[2] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, or C). $V_{DISABLEx}$ refers to the input disable signal on the same side as the V_{Ix} inputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.
[3] D0 refers to the ADuM230D0/ADuM231D0 models, and D1 refers to the ADuM230D1/ADuM231D1 models. See the Ordering Guide section.
[4] Input pins (V_{Ix}, $DISABLE_x$) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

Table 20. ADuM230E/ADuM231E Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	V_{Ex} Input[1, 2]	V_{DDI} State[2]	V_{DDO} State[2]	Default Low (E0), V_{Ox} Output[1, 2, 3]	Default High (E1), V_{Ox} Output[1, 2, 3]	Test Conditions/ Comments
L	H or NC	Powered	Powered	L	L	Normal operation
H	H or NC	Powered	Powered	H	H	Normal operation
X	L	Powered	Powered	Z	Z	Outputs disabled
L	H or NC	Unpowered	Powered	L	H	Fail-safe output
X[4]	L[4]	Unpowered	Powered	Z	Z	Outputs disabled
X[4]	X[4]	Powered	Unpowered	Indeterminate	Indeterminate	

[1] L means low, H means high, X means don't care, and NC means not connected, and Z means high impedance.
[2] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, or C). V_{Ex} refers to the output enable signal on the same side as the V_{Ox} inputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.
[3] E0 refers to the ADuM230E0/ADuM231E0 models, and E1 refers to the ADuM230E1/ADuM231E1 models. See the Ordering Guide section.
[4] Input pins (V_{Ix}, V_{Ex}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

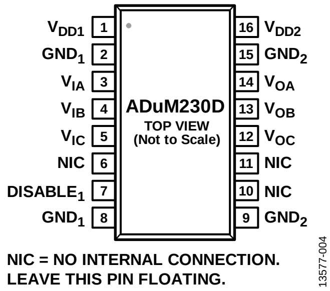


Figure 6. ADuM230D Pin Configuration

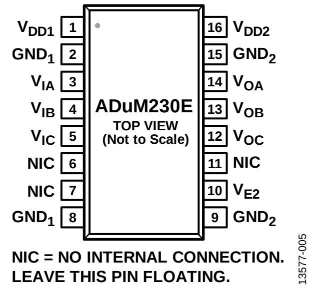


Figure 7. ADuM230E Pin Configuration

Table 21. Pin Function Descriptions

Pin No.[1]			
ADuM230D	**ADuM230E**	**Mnemonic**	**Description**
1	1	V_{DD1}	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND_1	Ground Reference for Isolator Side 1.
3	3	V_{IA}	Logic Input A.
4	4	V_{IB}	Logic Input B.
5	5	V_{IC}	Logic Input C.
6, 10, 11	6, 7, 11	NIC	No Internal Connection. Leave these pins floating.
7	Not applicable	$DISABLE_1$	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide.
9, 15	9, 15	GND_2	Ground Reference for Isolator Side 2.
Not applicable	10	V_{E2}	Output Enable 2. Active high logic input. When V_{E2} is high or disconnected, the V_{OA}, V_{OB}, and V_{OC} outputs are enabled. When V_{E2} is low, the V_{OA}, V_{OB}, and V_{OC} outputs are disabled to the high-Z state.
12	12	V_{OC}	Logic Output C.
13	13	V_{OB}	Logic Output B.
14	14	V_{OA}	Logic Output A.
16	16	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Reference the AN-1109 Application Note for specific layout guidelines.

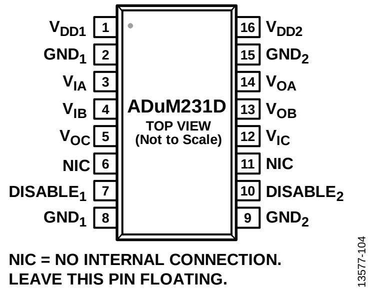


Figure 8. ADuM231D Pin Configuration

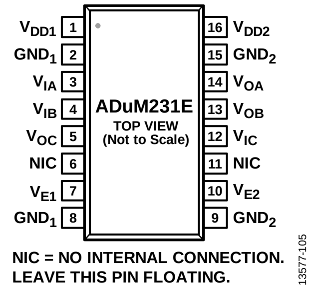


Figure 9. ADuM231E Pin Configuration

Table 22. Pin Function Descriptions

Pin No.[1]			
ADuM231D	**ADuM231E**	**Mnemonic**	**Description**
1	1	V_{DD1}	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND_1	Ground Reference for Isolator Side 1.
3	3	V_{IA}	Logic Input A.
4	4	V_{IB}	Logic Input B.
5	5	V_{OC}	Logic Output C.
6, 11	6, 11	NIC	No Internal Connection. Leave these pins floating.
7	Not applicable	$DISABLE_1$	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide.
Not applicable	7	V_{E1}	Output Enable 1. Active high logic input. When V_{E1} is high or disconnected, the V_{OC} output is enabled. When V_{E1} is low, the V_{OC} output is disabled to the high-Z state.
9, 15	9, 15	GND_2	Ground Reference for Isolator Side 2.
10	Not applicable	$DISABLE_2$	Input Disable 2. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide.
Not applicable	10	V_{E2}	Output Enable 2. Active high logic input. When V_{E2} is high or disconnected, the V_{OA} and V_{OB} outputs are enabled. When V_{E2} is low, the V_{OA} and V_{OB} outputs are disabled to the high-Z state.
12	12	V_{IC}	Logic Input C.
13	13	V_{OB}	Logic Output B.
14	14	V_{OA}	Logic Output A.
16	16	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Reference the AN-1109 Application Note for specific layout guidelines.

TYPICAL PERFORMANCE CHARACTERISTICS

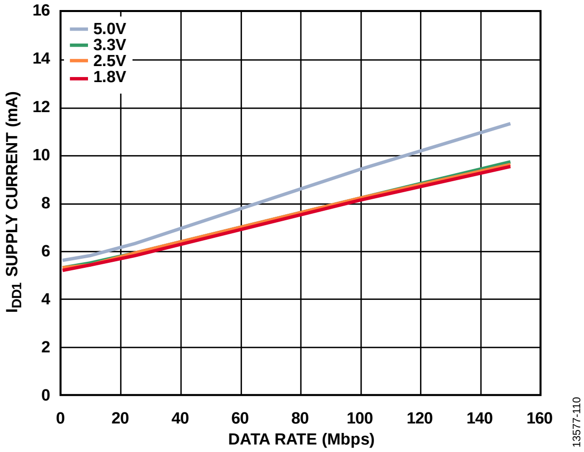


Figure 10. ADuM230D/ADuM230E I_{DD1} Supply Current vs. Data Rate at Various Voltages

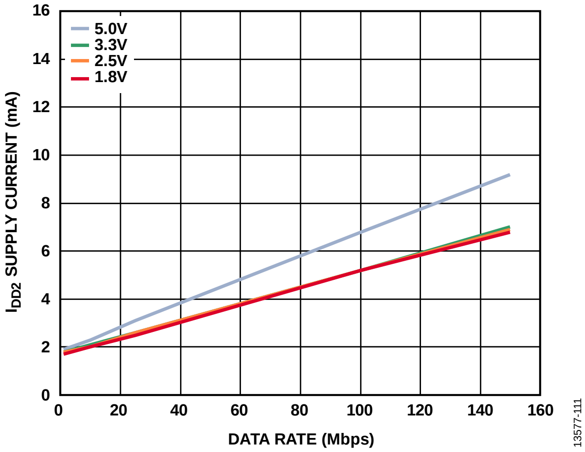


Figure 11. ADuM230D/ADuM230E I_{DD2} Supply Current vs. Data Rate at Various Voltages

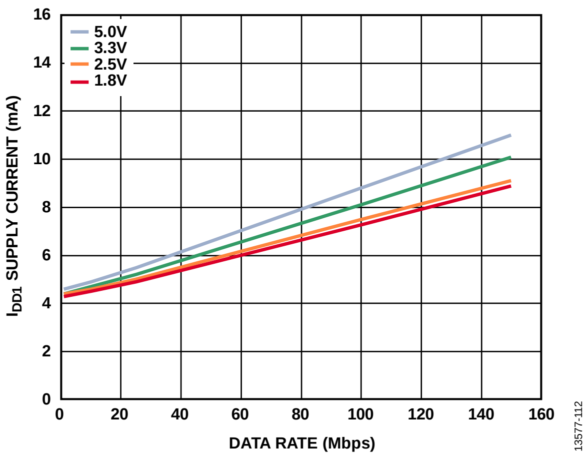


Figure 12. ADuM231D/ADuM231E I_{DD1} Supply Current vs. Data Rate at Various Voltages

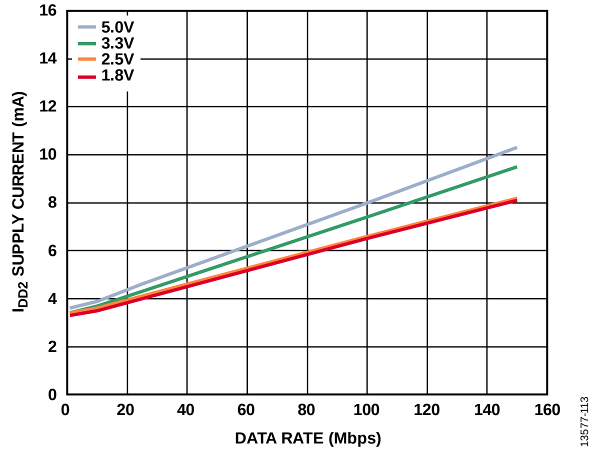


Figure 13. ADuM231D/ADuM231E I_{DD2} Supply Current vs. Data Rate at Various Voltages

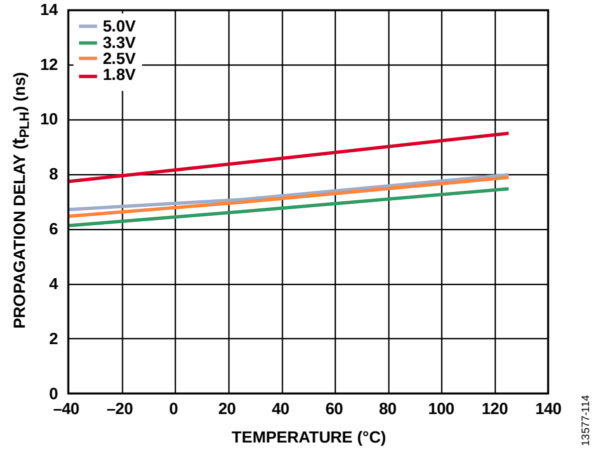


Figure 14. Propagation Delay (t_{PLH}) vs. Temperature at Various Voltages

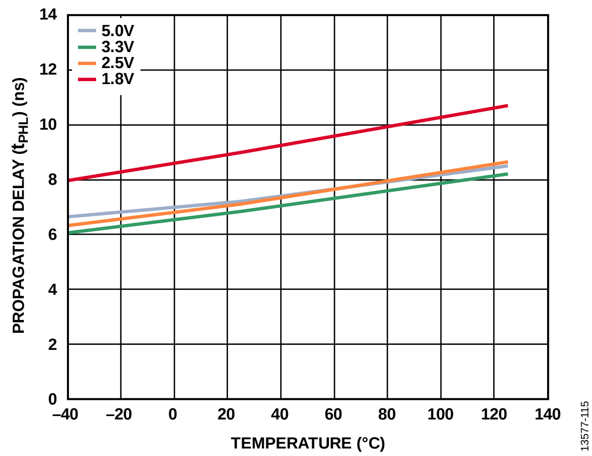


Figure 15. Propagation Delay(t_{PHL}) vs. Temperature at Various Voltages

THEORY OF OPERATION

The ADuM230D/ADuM230E/ADuM231D/ADuM231E use a high frequency carrier to transmit data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 16 and Figure 17, the ADuM230D/ADuM230E/ADuM231D/ ADuM231E have very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 16 illustrates the waveforms for the models of the ADuM230D/ADuM230E/ADuM231D/ADuM231E that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the low fail-safe output state (the ADuM230D0, ADuM231D0, ADuM230E0, and ADuM231E0 models) sets the output to low. For the ADuM230D/ADuM230E/ ADuM231D/ADuM231E models that have a fail-safe output state of high, Figure 17 illustrates the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the high fail-safe output state (the ADuM230D1, ADuM231D1, ADuM230E0, and ADuM231E1 models) sets the output to high. See the Ordering Guide for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

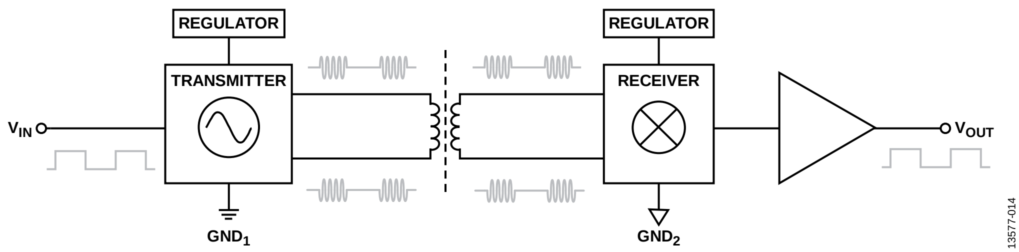


Figure 16. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

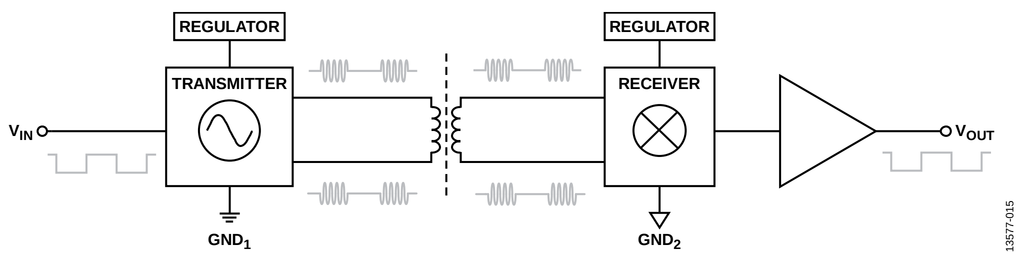


Figure 17. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM230D/ADuM230E/ADuM231D/ADuM231E digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 18). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The recommended bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered, unless the ground pair on each package side is connected close to the package.

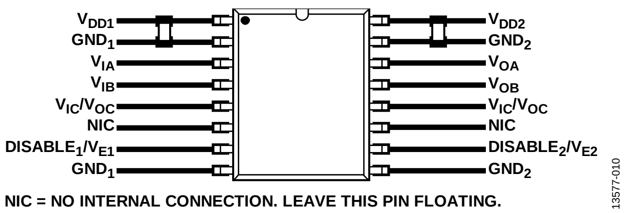


Figure 18. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time required for a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

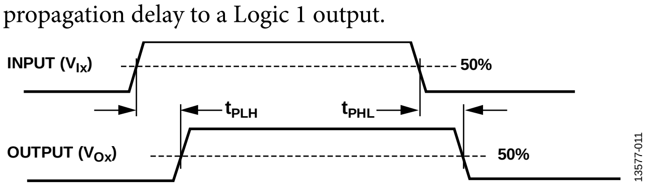


Figure 19. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single ADuM230D/ADuM230E/ADuM231D/ADuM231E component.

Propagation delay skew is the maximum amount the propagation delay differs between multiple ADuM230D/ADuM230E/ADuM231D/ADuM231E components operating under the same conditions.

JITTER MEASUREMENT

Figure 20 shows the eye diagram for the ADuM230D/ADuM230E/ADuM231D/ADuM231E. The measurement was taken using an Agilent 81110A pulse pattern generator at 150 Mbps with pseudorandom bit sequences (PRBS), 2(n − 1), n = 14, for 5 V supplies. Jitter was measured with the Tektronix Model 5104B oscilloscope, 1 GHz, 10 GSPS with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the ADuM230D/ADuM230E/ADuM231D/ADuM231E with 630 ps p-p jitter.

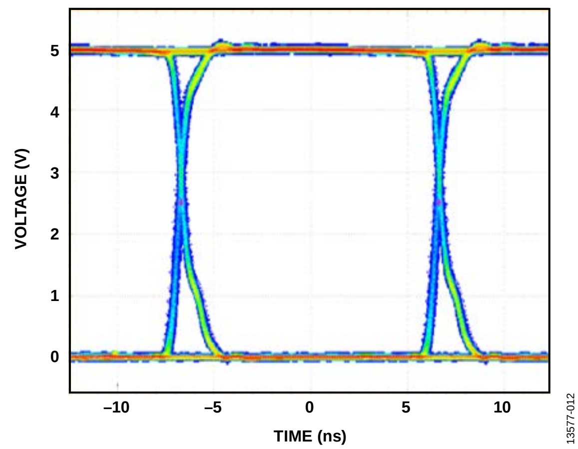


Figure 20. Eye Diagram

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components, which allows the components to be categorized in different material groups.

Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM230D/ADuM230E/ADuM231D/ADuM231E isolators are presented in Table 9.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by the insulation thickness and material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as is shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}^{2} + V_{DC}^{2}} \qquad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}^{2} - V_{DC}^{2}} \qquad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 21 and the following equations.

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}^{2} + V_{DC}^{2}}$$

$$V_{RMS} = \sqrt{240^{2} + 400^{2}}$$

$$V_{RMS} = 466\text{ V}$$

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}^{2} - V_{DC}^{2}}$$

$$V_{AC\ RMS} = \sqrt{466^{2} - 400^{2}}$$

$$V_{AC\ RMS} = 240\text{ V rms}$$

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 17 for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit in Table 17 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

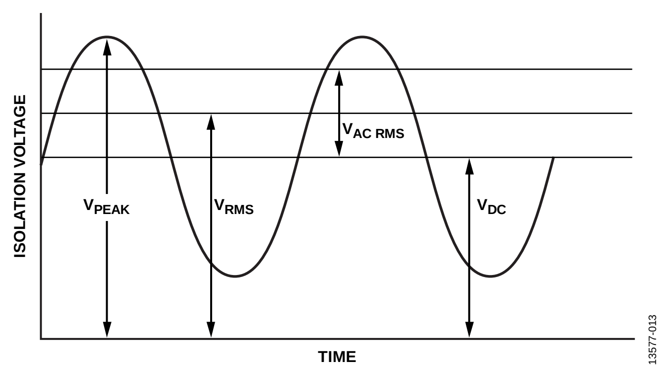
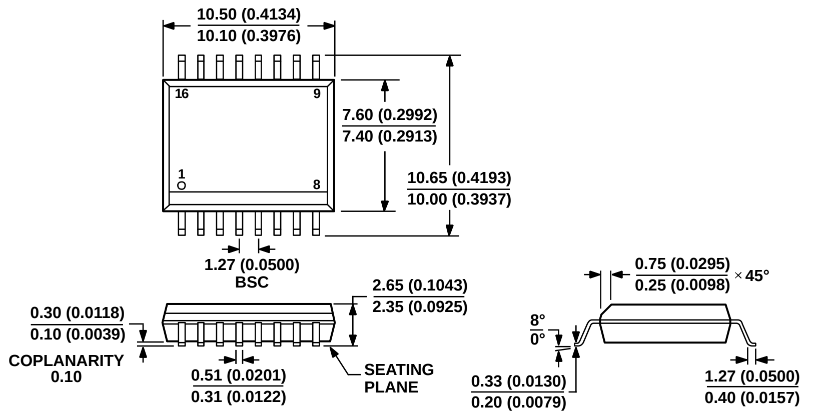


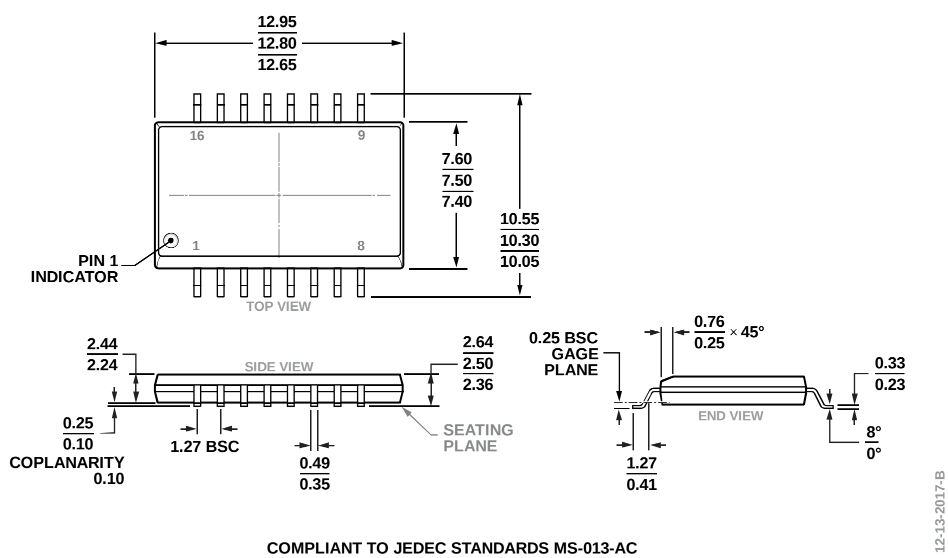
Figure 21. Critical Voltage Example

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 22. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013-AC

Figure 23. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Input Disable	Output Enable	Package Description	Package Option
ADuM230D1BRWZ	−40°C to +125°C	3	0	5.0	High	Yes	No	16-Lead SOIC_W	RW-16
ADuM230D1BRWZ-RL	−40°C to +125°C	3	0	5.0	High	Yes	No	16-Lead SOIC_W	RW-16
ADuM230D0BRWZ	−40°C to +125°C	3	0	5.0	Low	Yes	No	16-Lead SOIC_W	RW-16
ADuM230D0BRWZ-RL	−40°C to +125°C	3	0	5.0	Low	Yes	No	16-Lead SOIC_W	RW-16
ADuM230E1BRWZ	−40°C to +125°C	3	0	5.0	High	No	Yes	16-Lead SOIC_W	RW-16
ADuM230E1BRWZ-RL	−40°C to +125°C	3	0	5.0	High	No	Yes	16-Lead SOIC_W	RW-16
ADuM230E0BRWZ	−40°C to +125°C	3	0	5.0	Low	No	Yes	16-Lead SOIC_W	RW-16
ADuM230E0BRWZ-RL	−40°C to +125°C	3	0	5.0	Low	No	Yes	16-Lead SOIC_W	RW-16
ADuM230D1BRIZ	−40°C to +125°C	3	0	5.0	High	Yes	No	16-Lead SOIC_IC	RI-16-2
ADuM230D1BRIZ-RL	−40°C to +125°C	3	0	5.0	High	Yes	No	16-Lead SOIC_IC	RI-16-2
ADuM230D0BRIZ	−40°C to +125°C	3	0	5.0	Low	Yes	No	16-Lead SOIC_IC	RI-16-2
ADuM230D0BRIZ-RL	−40°C to +125°C	3	0	5.0	Low	Yes	No	16-Lead SOIC_IC	RI-16-2
ADuM230E1BRIZ	−40°C to +125°C	3	0	5.0	High	No	Yes	16-Lead SOIC_IC	RI-16-2
ADuM230E1BRIZ-RL	−40°C to +125°C	3	0	5.0	High	No	Yes	16-Lead SOIC_IC	RI-16-2
ADuM230E0BRIZ	−40°C to +125°C	3	0	5.0	Low	No	Yes	16-Lead SOIC_IC	RI-16-2
ADuM230E0BRIZ-RL	−40°C to +125°C	3	0	5.0	Low	No	Yes	16-Lead SOIC_IC	RI-16-2
ADuM231D1BRWZ	−40°C to +125°C	2	1	5.0	High	Yes	No	16-Lead SOIC_W	RW-16
ADuM231D1BRWZ-RL	−40°C to +125°C	2	1	5.0	High	Yes	No	16-Lead SOIC_W	RW-16
ADuM231D0BRWZ	−40°C to +125°C	2	1	5.0	Low	Yes	No	16-Lead SOIC_W	RW-16
ADuM231D0BRWZ-RL	−40°C to +125°C	2	1	5.0	Low	Yes	No	16-Lead SOIC_W	RW-16
ADuM231E1BRWZ	−40°C to +125°C	2	1	5.0	High	No	Yes	16-Lead SOIC_W	RW-16
ADuM231E1BRWZ-RL	−40°C to +125°C	2	1	5.0	High	No	Yes	16-Lead SOIC_W	RW-16
ADuM231E0BRWZ	−40°C to +125°C	2	1	5.0	Low	No	Yes	16-Lead SOIC_W	RW-16
ADuM231E0BRWZ-RL	−40°C to +125°C	2	1	5.0	Low	No	Yes	16-Lead SOIC_W	RW-16
ADuM231D1BRIZ	−40°C to +125°C	2	1	5.0	High	Yes	No	16-Lead SOIC_IC	RI-16-2
ADuM231D1BRIZ-RL	−40°C to +125°C	2	1	5.0	High	Yes	No	16-Lead SOIC_IC	RI-16-2
ADuM231D0BRIZ	−40°C to +125°C	2	1	5.0	Low	Yes	No	16-Lead SOIC_IC	RI-16-2
ADuM231D0BRIZ-RL	−40°C to +125°C	2	1	5.0	Low	Yes	No	16-Lead SOIC_IC	RI-16-2
ADuM231E1BRIZ	−40°C to +125°C	2	1	5.0	High	No	Yes	16-Lead SOIC_IC	RI-16-2
ADuM231E1BRIZ-RL	−40°C to +125°C	2	1	5.0	High	No	Yes	16-Lead SOIC_IC	RI-16-2
ADuM231E0BRIZ	−40°C to +125°C	2	1	5.0	Low	No	Yes	16-Lead SOIC_IC	RI-16-2
ADuM231E0BRIZ-RL	−40°C to +125°C	2	1	5.0	Low	No	Yes	16-Lead SOIC_IC	RI-16-2

[1] Z = RoHS Compliant Part.

D13577-0-10/18(B)