

AD9059* PRODUCT PAGE QUICK LINKS

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Application Notes

- AN-302: Exploit Digital Advantages in an SSB Receiver
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter

Data Sheet

- AD9059: Dual 8-Bit, 60 MSPS A/D Converter Data Sheet

REFERENCE MATERIALS

Technical Articles

- Correlating High-Speed ADC Performance to Multicarrier 3G Requirements
- DNL and Some of its Effects on Converter Performance
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9059 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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AD9059—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_D = 5 V, V_{DD} = 3 V, external reference, ENCODE = 60 MSPS, unless otherwise noted.)

Parameter	Temp	Test Level	AD9059BRS			Unit
			Min	Typ	Max	
RESOLUTION			8			Bits
DC ACCURACY						
Differential Nonlinearity	25°C	I		0.75	2.0	LSB
	Full	VI			2.5	LSB
Integral Nonlinearity	25°C	I		0.75	2.0	LSB
	Full	VI			2.5	LSB
No Missing Codes	Full	VI	Guaranteed			
Gain Error ¹	25°C	I	−6	−2.5	+6	% FS
	Full	VI	−8		+8	% FS
Gain Temperature Coefficient ¹	Full	V		±70		ppm/°C
ANALOG INPUT						
Input Voltage Range (Centered at 2.5 V)	25°C	V		1.0		V p-p
Input Offset Voltage	25°C	I	−15	0	+15	mV
	Full	VI	−25		+25	mV
Input Resistance	25°C	V		150		kΩ
Input Capacitance	25°C	V		2		pF
Input Bias Current	25°C	I		6	16	μA
Analog Bandwidth	25°C	V		120		MHz
CHANNEL MATCHING (A to B)						
Gain Delta	25°C	V		±1		% FS
Input Offset Voltage Delta	25°C	V		±4		mV
BAND GAP REFERENCE						
Output Voltage	Full	VI	2.4	2.5	2.6	V
Temperature Coefficient	Full	V		±10		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	60			MSPS
Minimum Conversion Rate	Full	IV			5	MSPS
Aperture Delay (t _A)	25°C	V		2.7		ns
Aperture Uncertainty (Jitter)	25°C	V		5		ps, rms
Output Valid Time (t _V) ²	Full	IV	4.0	6.6		ns
Output Propagation Delay (t _{PD}) ²	Full	IV		9.5	14.2	ns
DYNAMIC PERFORMANCE ³						
Transient Response	25°C	V		9		ns
Overvoltage Recovery Time	25°C	V		9		ns
Signal-to-Noise Ratio (SINAD) (with Harmonics)						
f _{IN} = 10.3 MHz	25°C	I	40	44.5		dB
f _{IN} = 76 MHz	25°C	V		43.5		dB
Effective Number of Bits (ENOB)						
f _{IN} = 10.3 MHz	25°C	I	6.35	7.1		Bits
f _{IN} = 76 MHz	25°C	V		6.9		Bits
Signal-to-Noise Ratio (SNR) (Without Harmonics)						
f _{IN} = 10.3 MHz	25°C	I	42	46		dB
f _{IN} = 76 MHz	25°C	V		45		dB
Second Harmonic Distortion						
f _{IN} = 10.3 MHz	25°C	I	−50	−62		dBc
f _{IN} = 76 MHz	25°C	V		−54		dBc
Third Harmonic Distortion						
f _{IN} = 10.3 MHz	25°C	I	−46	−60		dBc
f _{IN} = 76 MHz	25°C	V		−54		dBc
Two-Tone Intermodulation Distortion (IMD)	25°C	V		−52		dBc
Channel Crosstalk Rejection	25°C	V		−50		dBc
Differential Phase	25°C	V		0.8		Degrees
Differential Gain	25°C	V		1.0		%

SPECIFICATIONS (continued)

Parameter	Temp	Test Level	AD9059BRS			Unit
			Min	Typ	Max	
DIGITAL INPUTS						
Logic 1 Voltage	Full	VI	2.0			V
Logic 0 Voltage	Full	VI			0.8	V
Logic 1 Current	Full	VI			±1	μA
Logic 0 Current	Full	VI			±1	μA
Input Capacitance	25°C	V		4.5		pF
Encode Pulsewidth High (t_{EH})	25°C	IV	6.7		166	ns
Encode Pulsewidth Low (t_{EL})	25°C	IV	6.7		166	ns
DIGITAL OUTPUTS						
Logic 1 Voltage ($V_{DD} = 3\text{ V}$)	Full	VI	2.95			V
Logic 1 Voltage ($V_{DD} = 5\text{ V}$)	Full	IV	4.95			V
Logic 0 Voltage ($V_{DD} = 3\text{ V}$ or 5 V)	Full	VI			0.05	V
Output Coding			Offset Binary Code			
POWER SUPPLY						
V_D Supply Current ($V_D = 5\text{ V}$)	Full	VI		72	92	mA
V_{DD} Supply Current ($V_{DD} = 3\text{ V}$) ⁴	Full	VI		13	15	mA
Power Dissipation ^{5, 6}	Full	VI		400	505	mW
Power-Down Dissipation	Full	VI		6	12	mW
Power Supply Rejection Ratio (PSRR)	25°C	I		3		mV/V

NOTES

¹Gain error and gain temperature coefficient are based on the ADC only (with a fixed 2.5 V external reference).

² t_V and t_{PD} are measured from the 1.5 V level of the ENCODE to the 10%/90% levels of the digital output swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 μA.

³SNR/harmonics based on an analog input voltage of −0.5 dBFS referenced to a 1.0 V full-scale input range.

⁴Digital supply current based on $V_{DD} = 3\text{ V}$ output drive with <10 pF loading under dynamic test conditions.

⁵Power dissipation is based on 60 MSPS encode and 10.3 MHz analog input dynamic test conditions ($V_D = 5\text{ V} \pm 5\%$, $V_{DD} = 3\text{ V} \pm 5\%$).

⁶Typical thermal impedance for the RS style (SSOP) 28-lead package: $\theta_{JC} = 39^\circ\text{C/W}$, $\theta_{CA} = 70^\circ\text{C/W}$, and $\theta_{JA} = 109^\circ\text{C/W}$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

- I – 100% production tested.
- II – 100% production tested at +25°C and sample tested at specified temperatures.
- III – Sample tested only.
- IV – Parameter is guaranteed by design and characterization testing.
- V – Parameter is a typical value only.
- VI – 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range.

ABSOLUTE MAXIMUM RATINGS*

V_D, V_{DD}	7 V
Analog Inputs	−0.5 V to $V_D + 0.5\text{ V}$
Digital Inputs	−0.5 V to $V_D + 0.5\text{ V}$
VREF Input	−0.5 V to $V_D + 0.5\text{ V}$
Digital Output Current	20 mA
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9059BRS	−40°C to +85°C	RS-28
AD9059/PCB	25°C	Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9059 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



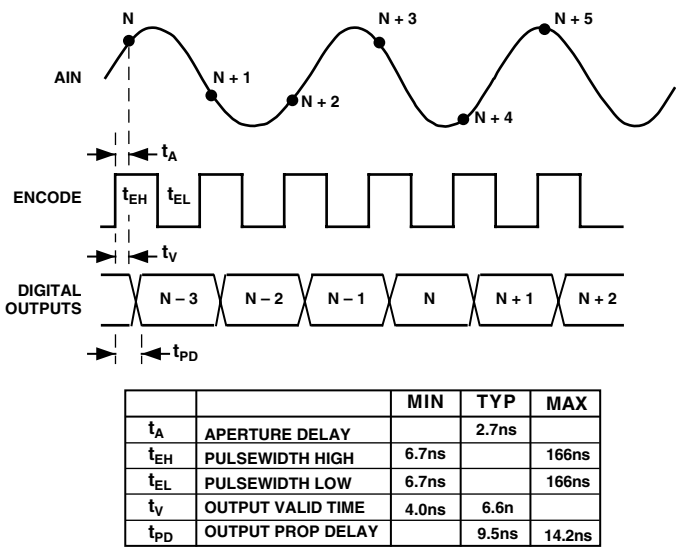
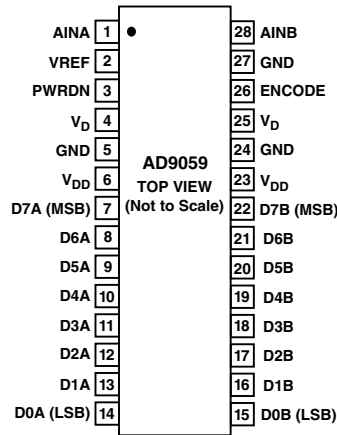


Figure 1. Timing Diagram

PIN CONFIGURATION



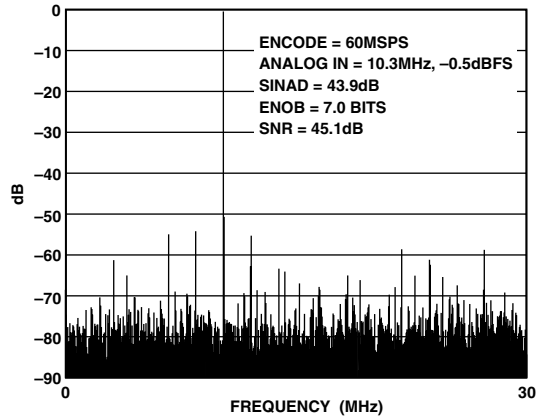
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1, 28	AINA, AINB	Analog Inputs for ADC A and B.
2	VREF	Internal Voltage Reference (2.5 V Typical); Bypass with 0.1 μ F to Ground or Overdrive with External Voltage Reference.
3	PWRDN	Power-Down Function Select; Logic HIGH for Power-Down Mode (Digital Outputs Go to High-Impedance State).
4, 25	V _D	Analog 5 V Power Supply.
5, 24, 27	GND	Ground.
6, 23	V _{DD}	Digital Output Power Supply. Nominally 3 V to 5 V.
7–14	D7A–D0A	Digital Outputs of ADC A.
22–15	D7B–D0B	Digital Outputs of ADC B.
26	ENCODE	Encode Clock for ADCs A and B (ADCs Sample Simultaneously on the Rising Edge of ENCODE).

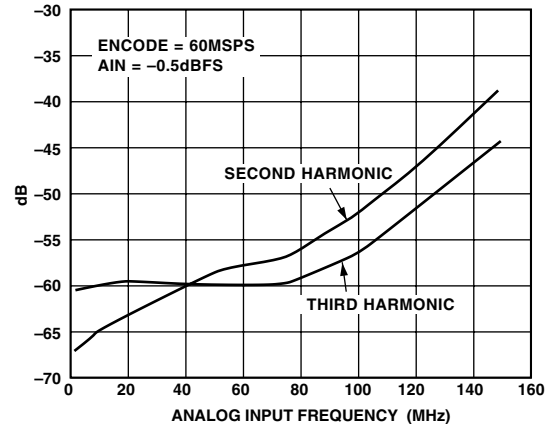
Table I. Digital Coding (VREF = 2.5 V)

Analog Input (V)	Voltage Level	Digital Output
3.0	Positive Full Scale	1111 1111
2.502	Midscale + 1/2 LSB	1000 0000
2.498	Midscale – 1/2 LSB	0111 1111
2.0	Negative Full Scale	0000 0000

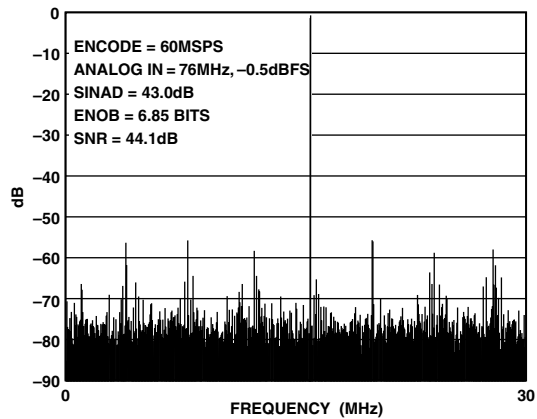
Typical Performance Characteristics—AD9059



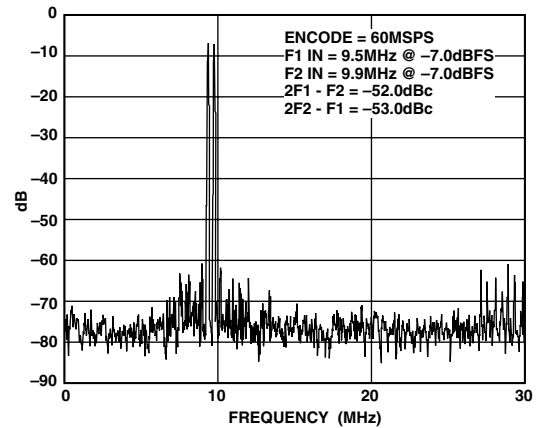
TPC 1. FFT Spectral Plot 60 MSPS, 10.3 MHz



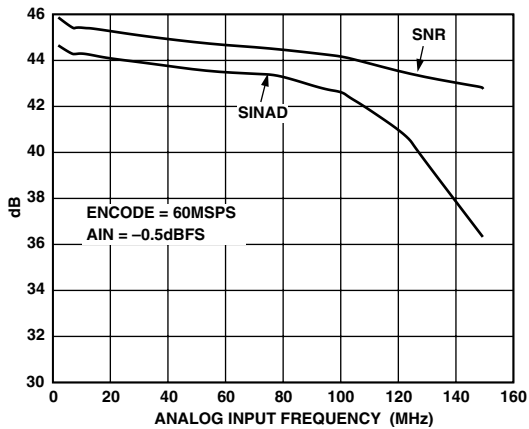
TPC 4. Harmonic Distortion vs. AIN Frequency



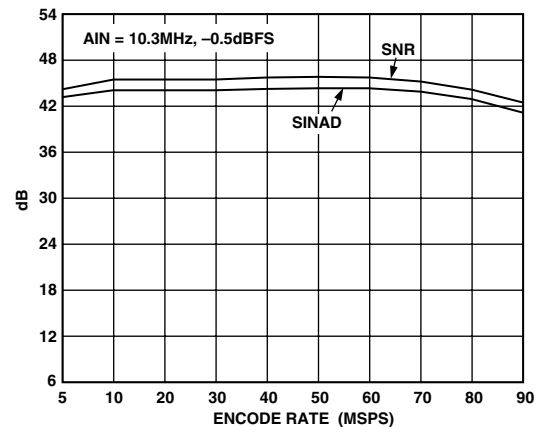
TPC 2. Spectral Plot 60 MSPS, 76 MHz



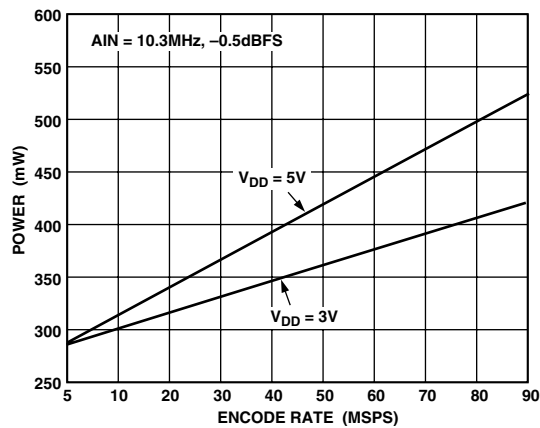
TPC 5. Two-Tone IMD



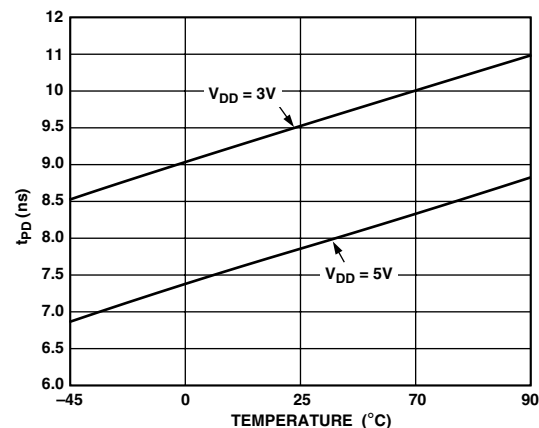
TPC 3. SINAD/SNR vs. AIN Frequency



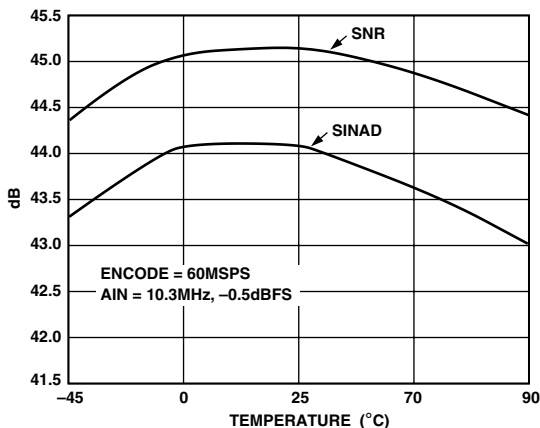
TPC 6. SINAD/SNR vs. Encode Rate



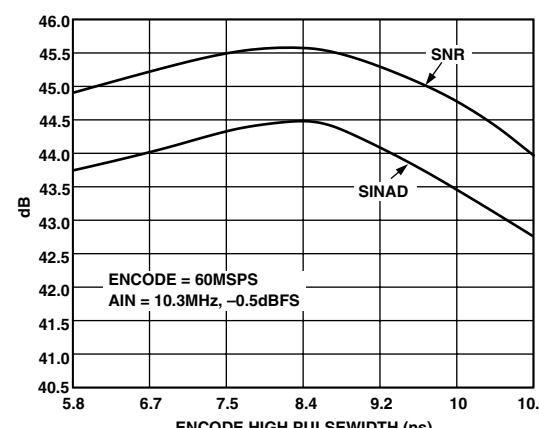
TPC 7. Power Dissipation vs. Encode Rate



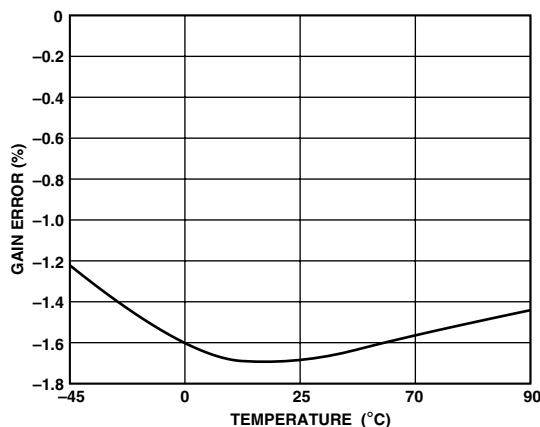
TPC 10. t_{PD} vs. Temperature/Supply (3 V/5 V)



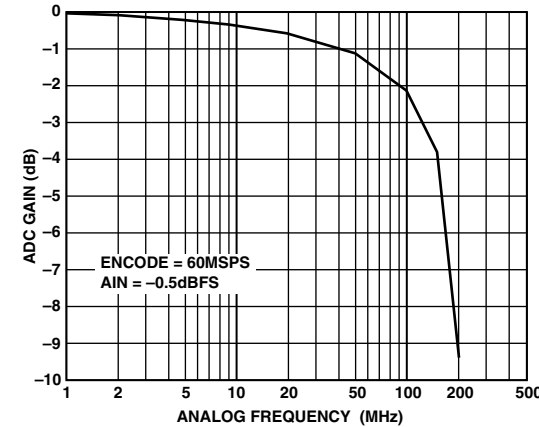
TPC 8. SINAD/SNR vs. Temperature



TPC 11. SINAD/SNR vs. Encode Pulsewidth



TPC 9. ADC Gain vs. Temperature (With External 2.5 V Reference)



TPC 12. ADC Frequency Response

THEORY OF OPERATION

The AD9059 combines Analog Devices' proprietary MagAmp gray code conversion circuitry with flash converter technology to provide dual high performance 8-bit ADCs in a single low cost monolithic device. The design architecture ensures low power, high speed, and 8-bit accuracy.

The AD9059 provides two linked ADC channels that are clocked from a single ENCODE input (see Functional Block Diagram). The two ADC channels simultaneously sample the analog inputs (AINA and AINB) and provide noninterleaved parallel digital outputs (D0A–D7A and D0B–D7B). The voltage reference (VREF) is internally connected to both ADCs so channel gains and offsets will track if external reference control is desired.

The analog input signal is buffered at the input of each ADC channel and applied to a high speed track-and-hold. The track-and-hold circuit holds the analog input value during the conversion process (beginning with the rising edge of the ENCODE command). The track-and-hold's output signal passes through the gray code and flash conversion stages to generate coarse and fine digital representations of the held analog input level. Decode logic combines the multistage data and aligns the 8-bit word for strobed outputs on the rising edge of the ENCODE command. The MagAmp/Flash architecture of the AD9059 results in three pipeline delays for the output data.

USING THE AD9059

Analog Inputs

The AD9059 provides independent single-ended high impedance (150 k Ω) analog inputs for the dual ADCs. Each input requires a dc bias current of 6 μ A (typical) centered near 2.5 V ($\pm 10\%$). The dc bias may be provided by the user or may be derived from the ADC's internal voltage reference. Figure 2 shows a low cost dc bias implementation that allows the user to capacitively couple ac signals directly into the ADC without additional active circuitry. For best dynamic performance, the VREF pin should be decoupled to ground with a 0.1 μ F capacitor (to minimize modulation of the reference voltage), and the bias resistor should be approximately 1 k Ω .

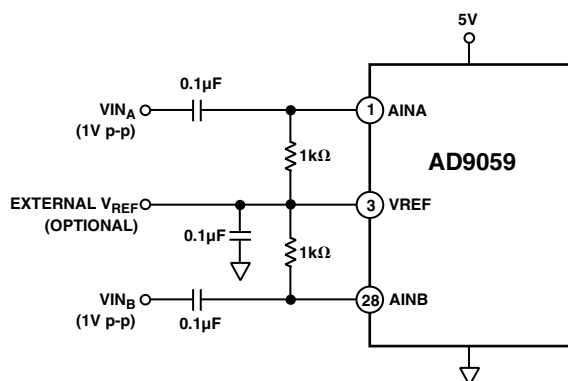


Figure 2. Capacity Coupled AD9059

Figure 3 shows typical connections for high performance dc biasing using the ADC's internal voltage reference. All components may be powered from a single 5 V supply (analog input signals are referenced to ground).

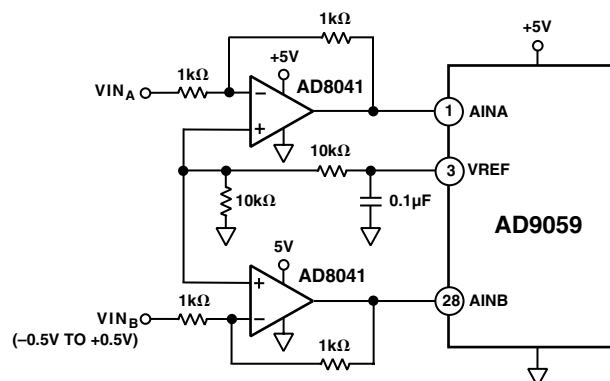


Figure 3. DC-Coupled AD9059 (VIN Inverted)

Voltage Reference

A stable and accurate 2.5 V voltage reference is built into the AD9059 (VREF). The reference output is used to set the ADC gain/offset and can provide dc bias for the analog input signals. The internal reference is tied to the ADC circuitry through an 800 Ω internal impedance and is capable of providing 300 μ A external drive current (for dc biasing the analog input or other user circuitry).

Some applications may require greater accuracy, improved temperature performance, or gain adjustments that cannot be obtained using the internal reference. An external voltage may be applied to the VREF pin to overdrive the internal voltage reference for gain adjustment of up to $\pm 10\%$ (the VREF pin is internally tied directly to the ADC circuitry). ADC gain and offset will vary simultaneously with external reference adjustment with a 1:1 ratio (a 2% or 50 mV adjustment to the 2.5 V reference varies ADC gain by 2% and ADC offset by 50 mV).

Theoretical input voltage range versus reference input voltage may be calculated using the following equations.

$$V_{\text{RANGE}} (p - p) = V_{\text{REF}}/2.5$$

$$V_{\text{MIDSCALE}} = V_{\text{REF}}$$

$$V_{\text{TOP-OF-RANGE}} = V_{\text{REF}} + V_{\text{RANGE}}/2$$

$$V_{\text{BOTTOM-OF-RANGE}} = V_{\text{REF}} - V_{\text{RANGE}}/2$$

The external reference should have a 1 mA minimum sink/source current capability to ensure complete overdrive of the internal voltage reference.

AD9059

Digital Logic (5 V/3 V Systems)

The digital inputs and outputs of the AD9059 can easily be configured to interface directly with 3 V or 5 V logic systems. The encode and power-down (PWRDN) inputs are CMOS stages with TTL thresholds of 1.5 V, making the inputs compatible with TTL, 5 V CMOS, and 3 V CMOS logic families. As with all high speed data converters, the encode signal should be clean and jitter free to prevent degradation of ADC dynamic performance.

The AD9059's digital outputs will also interface directly with 5 V or 3 V CMOS logic systems. The voltage supply pins (V_{DD}) for these CMOS stages are isolated from the analog V_D voltage supply. By varying the voltage on these supply pins, the digital output high levels will change for 5 V or 3 V systems. The V_{DD} pins are internally connected on the AD9059 die. Care should be taken to isolate the V_{DD} supply voltages from the 5 V analog supply to minimize noise coupling into the ADCs.

The AD9059 provides high impedance digital output operation when the ADC is driven into power-down mode (PWRDN, logic high). A 200 ns (minimum) power-down time should be provided before a high impedance characteristic is required. A 200 ns power-up period should be provided to ensure accurate ADC output data after reactivation (valid output data is available three clock cycles after the 200 ns delay).

Timing

The AD9059 is guaranteed to operate with conversion rates from 5 MSPS to 60 MSPS. At 60 MSPS, the ADC is designed to operate with an encode duty cycle of 50%, but performance is insensitive to moderate variations. Pulswidth variations of up to $\pm 10\%$ (allowing the encode signal to meet the minimum/maximum high/low specifications) will cause no degradation in ADC performance (see Figure 1).

Due to the linked ENCODE architecture of the ADCs, the AD9059 cannot be operated in a 2-channel ping-pong mode.

Power Dissipation

The power dissipation of the AD9059 is specified to reflect a typical application setup under the following conditions: encode is 60 MSPS, analog input is -0.5 dBFS at 10.3 MHz, V_D is 5 V, V_{DD} is 3 V, and digital outputs are loaded with 7 pF typical (10 pF maximum). The actual dissipation will vary as these conditions are modified in user applications. TPC 7 shows typical power consumption for the AD9059 versus ADC encode frequency and V_{DD} supply voltage.

A power-down function allows users to reduce power dissipation when ADC data is not required. A TTL/CMOS high signal (PWRDN) shuts down portions of the dual ADC and brings total power dissipation to less than 10 mW. The internal band gap voltage reference remains active during power-down mode to minimize ADC reactivation time. If the power-down function is not desired, Pin 3 should be tied to ground. Both ADC channels are controlled simultaneously by the PWRDN pin; they cannot be shut down or turned on independently.

Applications

The wide analog bandwidth of the AD9059 makes it attractive for a variety of high performance receiver and encoder applications. Figure 4 shows the dual ADC in a typical low cost I and Q demodulator implementation for cable, satellite, or wireless LAN modem receivers. The excellent dynamic performance of the ADC at higher analog input frequencies and encode rates empowers users to employ direct IF sampling techniques (see TPC 2). IF sampling eliminates or simplifies analog mixer and filter stages to reduce total system cost and power.

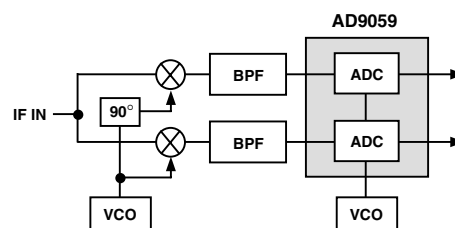


Figure 4. I and Q Digital Receiver

The high sampling rate and analog bandwidth of the AD9059 are ideal for computer RGB video digitizer applications. With a full-power analog bandwidth of $2\times$ the maximum sampling rate, the ADC provides sufficient pixel-to-pixel transient settling time to ensure accurate 60 MSPS video digitization. Figure 5 shows a typical RGB video digitizer implementation for the AD9059.

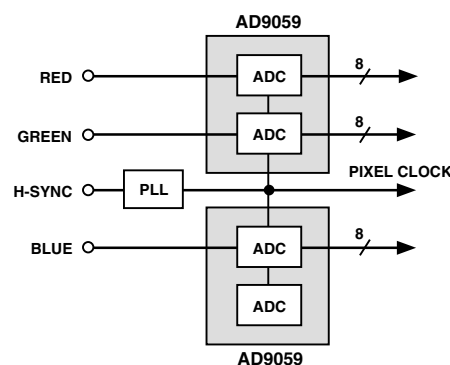


Figure 5. RGB Video Encoder

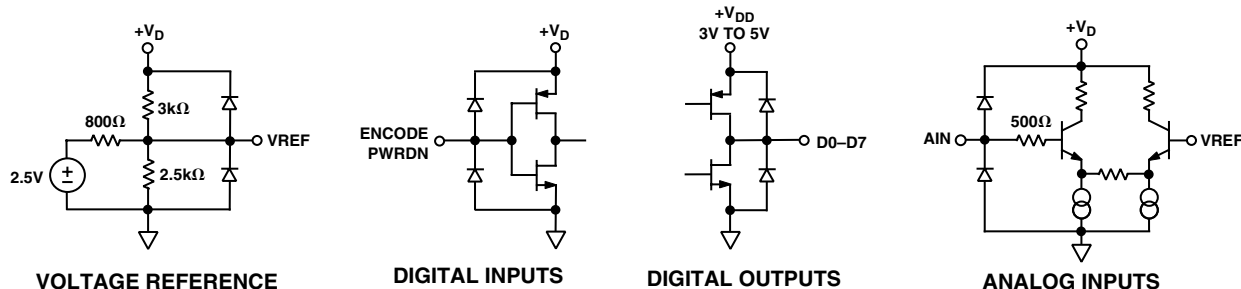


Figure 6. Equivalent Circuits

Evaluation Board

The AD9059/PCB evaluation board provides an easy-to-use analog/digital interface for the dual 8-bit, 60 MSPS ADC. The board includes typical hardware configurations for a variety of high speed digitization evaluations. On-board components include the AD9059 (in the 28-lead SSOP package), optional analog input buffer amplifiers, digital output latches, board timing drivers, and configurable jumpers for ac coupling, dc coupling, and power-down function testing. The board is configured at shipment for dc coupling using the AD9059's internal reference.

For dc-coupled analog input applications, amplifiers U3 and U4 are configured to operate as unity gain inverters with adjustable offset for the analog input signals. For full-scale ADC drive, each analog input signal should be 1 V p-p into 50 Ω referenced to ground. Each amplifier offsets its analog signal by +VREF (2.5 V typical) to center the voltage for proper ADC input drive. For dc-coupled operation, connect E7 to E9 (analog input A to R11), E14 to E13 (amplifier output to analog input A of AD9059), E4 to E5 (analog input B to R10), and E11 to E10 (amplifier output to analog input B of AD9059) using the board jumper connectors.

For ac-coupled analog input applications, amplifiers U3 and U4 are removed from the analog signal paths. The analog signals are coupled through Capacitors C11 and C12, each terminated to the VREF voltage through separate 1 k Ω resistors (providing bias current for the AD9059 analog inputs, AINA and AINB).

Analog input signals to the board should be 1 V p-p into 50 Ω for full-scale ADC drive. For ac-coupled operation, connect E7 to E8 (analog input A to C12 feedthrough capacitor), E13 to E15 (C12 to R15 termination resistor for Channel A), E4 to E6 (analog input B to C11 feedthrough capacitor), and E10 to E12 (C11 to R14 termination resistor for Channel B) using the board jumper connectors.

The on-board reference voltage may be used to drive the ADC or an external reference may be applied. The standard configuration employs the internal voltage reference without any external connection requirements. An external voltage reference may be applied at board connector input REF to overdrive the limited current output of the AD9059's internal voltage reference. The external voltage reference should be 2.5 V typical.

The power-down function of the AD9059 can be exercised through a board jumper connection. Connect E2 to E1 (5 V to PWRDN) for power-down mode operation. For normal operation, connect E3 to E1 (ground to PWRDN).

The encode signal source should be TTL/CMOS compatible and capable of driving a 50 Ω termination. The digital outputs of the AD9059 are buffered through latches on the evaluation board (U5 and U6) and are available for the user at connector Pins 30–37 and Pins 22–29. Latch timing is derived from the ADC ENCODE clock and a digital clocking signal is provided for the board user at connector Pins 2 and 21.

AD9059

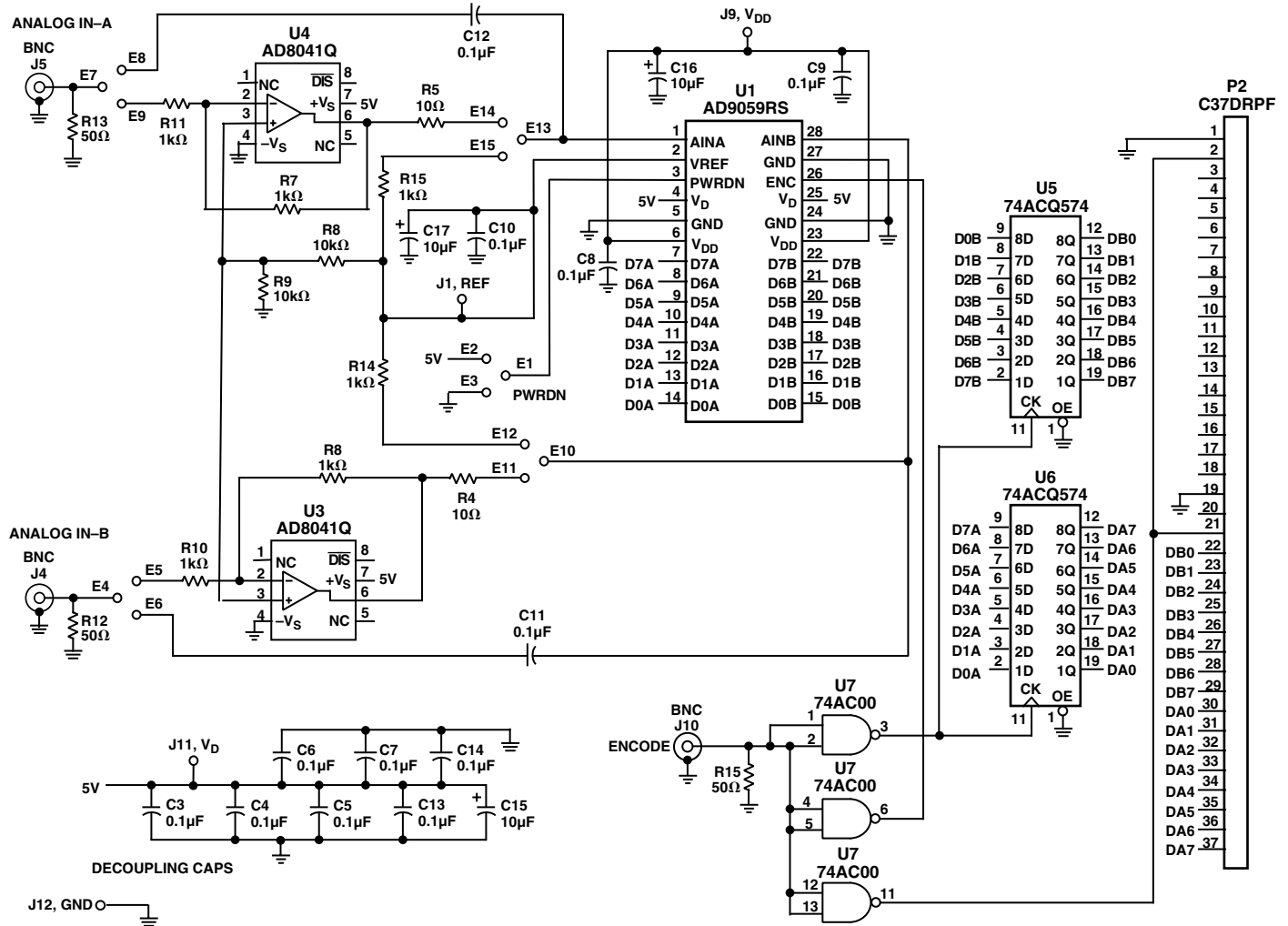


Figure 7. AD9059 Dual Evaluation Board Schematic

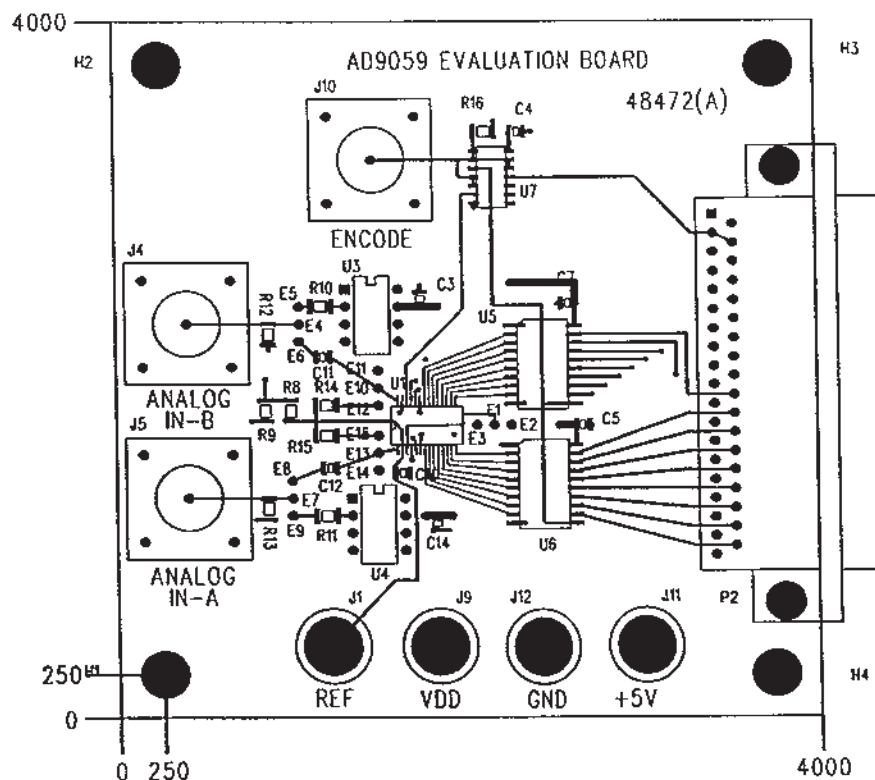


Figure 8. Evaluation Board Layout (Top)

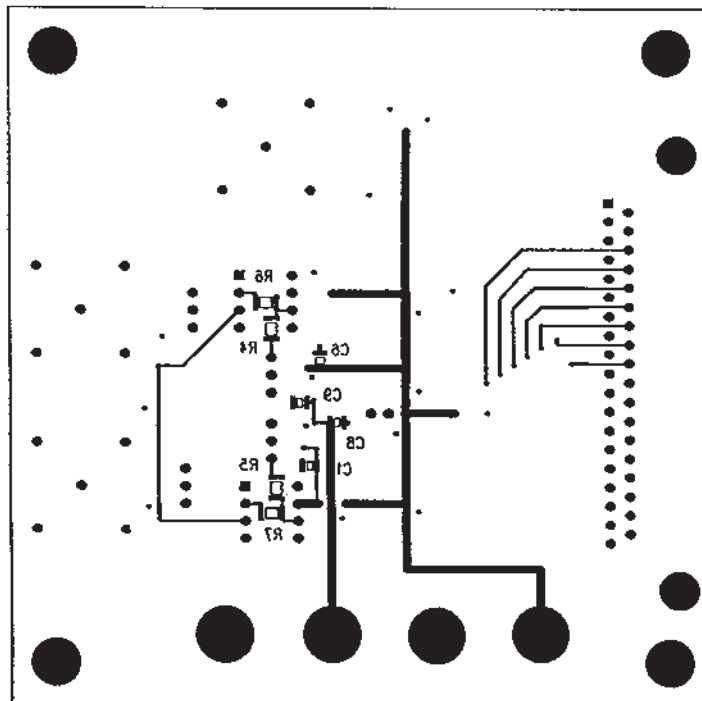
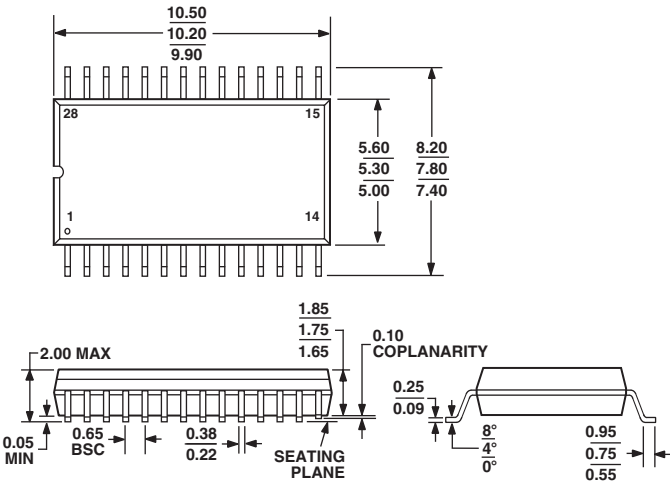


Figure 9. Evaluation Board Layout (Bottom)

OUTLINE DIMENSIONS

28-Lead Shrink Small Outline Package [SSOP]
(RS-28)

Dimensions shown in millimeters



Revision History

Location	Page
4/03—Data Sheet changed from REV. 0 to REV. A.	
Renumbered Figures and TPCs	Universal
Changes to SPECIFICATIONS	3
Updated OUTLINE DIMENSIONS	12

C00563-0-4/03(A)