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7/2014—Rev. 0 to Rev. A

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1/2014—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, V_{REF} = 5 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage	IN+ and IN−	−0.1		V_{REF} + 0.1	V
Common-Mode Input Range	IN+ and IN−	$V_{REF} \times 0.475$	$V_{REF} \times 0.5$	$V_{REF} \times 0.525$	V
Analog Input Common Mode Rejection Ratio (CMRR)	f_{IN} = 450 kHz		67		dB
Leakage Current at 25°C	Acquisition phase		200		nA
Input Impedance			See the Analog Inputs section		
ACCURACY					
No Missing Codes		18			Bits
Differential Nonlinearity Error (DNL)		−0.85	±0.5	+1.5	LSB
Integral Nonlinearity Error (INL)		−2	±1	+2	LSB
Transition Noise	V_{REF} = 5 V		1.05		LSB[1]
Gain Error, T_{MIN} to T_{MAX}[2]		−0.023	+0.004	+0.023	% of FS
Gain Error Temperature Drift			±1		ppm/°C
Zero Error, T_{MIN} to T_{MAX}[2]			±100	+700	µV
Zero Temperature Drift			0.5		ppm/°C
Power Supply Rejection Ratio (PSRR)	VDD = 2.5 V ± 5%		90		dB
THROUGHPUT					
AD7989-1 Conversion Rate		0		100	kSPS
AD7989-5 Conversion Rate		0		500	kSPS
Transient Response	Full-scale step			400	ns
AC ACCURACY					
Dynamic Range	V_{REF} = 5 V	97	99		dB[3]
	V_{REF} = 2.5 V		93		dB[3]
Oversampled Dynamic Range[4]	f_O = 1 kSPS		126		dB[3]
Signal-to-Noise Ratio (SNR)	f_{IN} = 1 kHz, V_{REF} = 5 V	95.5	98		dB[3]
	f_{IN} = 1 kHz, V_{REF} = 2.5 V		92.5		dB[3]
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 10 kHz		−115		dB[3]
Total Harmonic Distortion[5] (THD)	f_{IN} = 10 kHz		−120		dB[3]
Signal-to-Noise-and-Distortion Ratio (SINAD)	f_{IN} = 1 kHz, V_{REF} = 5 V		97		dB[3]

[1] LSB means least significant bit. With the ±5 V input range, 1 LSB is 38.15 µV.
[2] See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
[3] All specifications expressed in decibels are referred to a full-scale range (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[4] Dynamic range is obtained by oversampling the ADC running at a throughput, f_S, of 500 kSPS followed by postdigital filtering with an output word rate of f_O.
[5] Tested fully in production at f_{IN} = 1 kHz.

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, V_{REF} = 5 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		2.4		5.1	V
Load Current	V_{REF} = 5 V		250		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			10		MHz
Aperture Delay	VDD = 2.5 V		2		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}	VIO > 3 V	−0.3		+0.3 × VIO	V
	VIO ≤ 3 V	−0.3		+0.1 × VIO	V
V_{IH}	VIO > 3 V	0.7 × VIO		VIO + 0.3	V
	VIO ≤ 3 V	0.9 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial, 18 bits, twos complement			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		2.375	2.5	2.625	V
VIO		1.71		5.5	V
Standby Current[1, 2]	VDD and VIO = 2.5 V, 25°C		0.35		µA
AD7989-1 Power Dissipation	VDD = 2.625 V, V_{REF} = 5 V, VIO = 3 V				
Total	10 kSPS throughput		70	86	µW
	100 kSPS throughput		700	860	µW
VDD Only			400		µW
REF Only			170		µW
VIO Only			130		µW
AD7989-5 Power Dissipation	VDD = 2.625 V, V_{REF} = 5 V, VIO = 3 V				
Total	500 kSPS throughput		3.5	4.3	mW
VDD Only			2		mW
REF Only			0.85		mW
VIO Only			0.65		mW
Energy per Conversion			7.0		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VIO or ground as required.
[2] During acquisition phase.

TIMING SPECIFICATIONS

VDD = 2.37 V to 2.63 V, VIO = 1.71 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted. See Figure 2 for load conditions.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
THROUGHPUT RATE					
AD7989-1				100	kSPS
AD7989-5				500	kSPS
CONVERSION AND ACQUISITION TIMES					
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}				
AD7989-1				9500	ns
AD7989-5				1600	ns
Acquisition Time	t_{ACQ}				
AD7989-1		500			ns
AD7989-5		400			ns
Time Between Conversions	t_{CYC}				
AD7989-1		10			µs
AD7989-5		2			µs
CNV PULSE WIDTH ($\overline{CS}$ MODE)	t_{CNVH}	500			ns
SCK					
SCK Period ($\overline{CS}$ Mode)	t_{SCK}				
VIO Above 4.5 V		10.5			ns
VIO Above 3 V		12			ns
VIO Above 2.7 V		13			ns
VIO Above 2.3 V		15			ns
VIO Above 1.71 V		22			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 4.5 V		11.5			ns
VIO Above 3 V		13			ns
VIO Above 2.7 V		14			ns
VIO Above 2.3 V		16			ns
VIO Above 1.71 V		23			ns
SCK Low Time	t_{SCKL}				
VIO Above 2.3 V		4.5			ns
VIO Above 1.71 V		6			ns
SCK High Time	t_{SCKH}				
VIO Above 2.3 V		4.5			ns
VIO Above 1.71 V		6			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				9.5	ns
VIO Above 3 V				11	ns
VIO Above 2.7 V				12	ns
VIO Above 2.3 V				14	ns
VIO Above 1.71 V			14	21	ns

Parameter[1]	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ MODE					
CNV or SDI Low to SDO D17 MSB Valid	t_{EN}				
VIO Above 3 V				10	ns
VIO Above 2.3 V				15	ns
VIO Above 1.71 V			18	40	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	5			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$				
VIO Above 2.3 V		2			ns
VIO Above 1.71 V		10			ns
CHAIN MODE					
SCK Valid Setup Time from CNV Rising Edge	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge	$t_{HSDISCK}$	3			ns

[1] Timing parameters measured with respect to a falling edge are defined as triggered at X% VIO. Timing parameters measured with respect to a rising edge are defined as triggered at Y% VIO. For VIO ≤ 3 V, X = 90 and Y = 10. For VIO > 3 V, X = 70 and Y = 30. The minimum V_{IH} and maximum V_{IL} are used. See the Digital Inputs Specifications in Table 2.

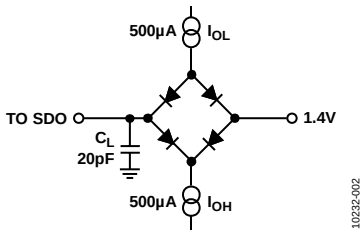


Figure 2. Load Circuit for Digital Interface Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
IN+, IN− to GND[1]	−0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply Voltage	
REF, VIO to GND	−0.3 V to +6.0 V
VDD to GND	−0.3 V to +3.0 V
VDD to VIO	+3 V to −6 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Output to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering	JEDEC Standard (J-STD-020)

[1] See the Analog Inputs section for an explanation of IN+ and IN−.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
RM-10	200	44	°C/W
CP-10-9	48.7	2.96	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on use of a 2S2P JEDEC PCB. See the Ordering Guide.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

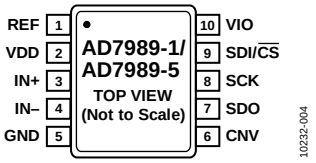


Figure 3. 10-Lead MSOP Pin Configuration

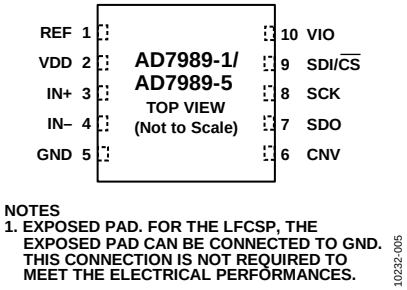


Figure 4. 10-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REF	AI	Reference Input Voltage. The REF range is 2.4 V to 5.1 V. This pin is referred to the GND pin and must be decoupled closely to the GND pin with a 10 µF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Differential Positive Analog Input.
4	IN–	AI	Differential Negative Analog Input.
5	GND	P	Power Supply Ground.
6	CNV	DI	Conversion Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the device: chain mode or chip select ($\overline{CS}$) mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In chain mode, the data is read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.
9	SDI/$\overline{CS}$	DI	Serial Data Input/Chip Select. This input has multiple functions. It selects the interface mode of the ADC as follows: Chain mode is selected if this pin is low during the CNV rising edge. In this mode, SDI/$\overline{CS}$ is a data input that daisy-chains the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI/$\overline{CS}$ is the output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI/$\overline{CS}$ is high during the CNV rising edge. In this mode, either SDI/$\overline{CS}$ or CNV can enable the serial output signals when low.
10	VIO	P	Input/Output Interface Digital Power. This pin is nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
	EPAD		Exposed Pad. For the LFCSP, the exposed pad can be connected to GND. This connection is not required to meet the electrical performances.

[1]AI means analog input, DI means digital input, DO means digital output, and P means power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V, V_{REF} = 5.0 V, VIO = 3.3 V.

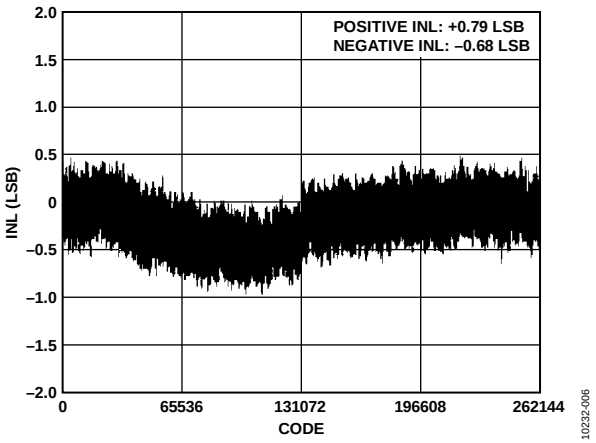


Figure 5. INL vs. Code

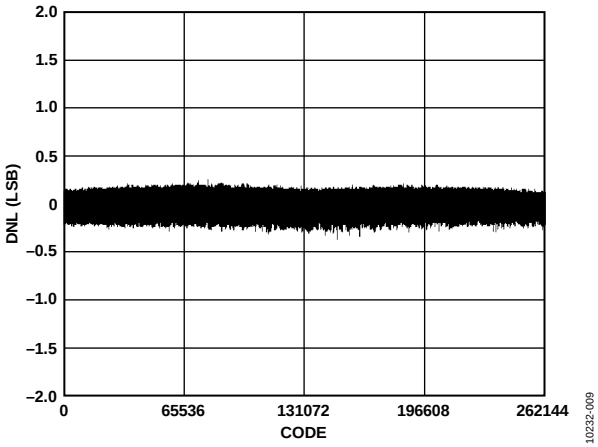


Figure 8. DNL vs. Code

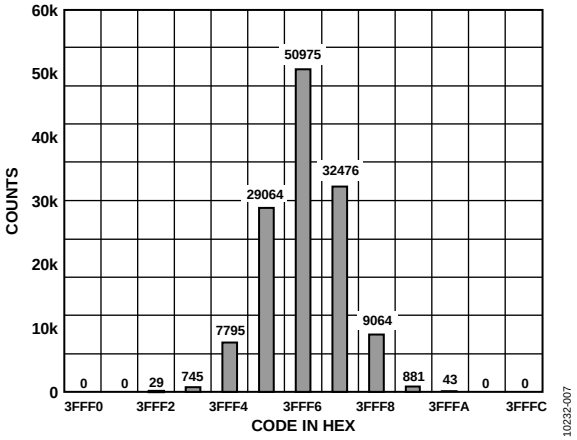


Figure 6. Histogram of a DC Input at the Code Center

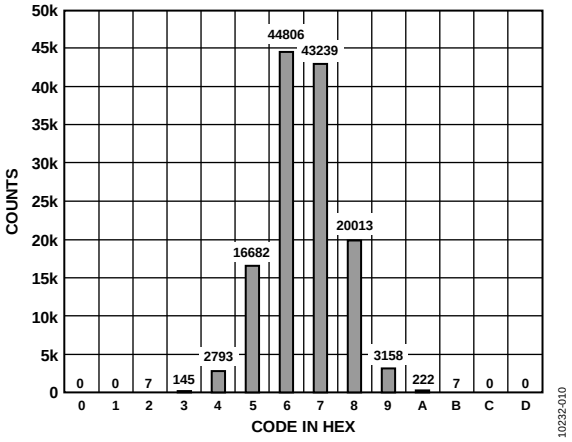


Figure 9. Histogram of a DC Input at the Code Transition

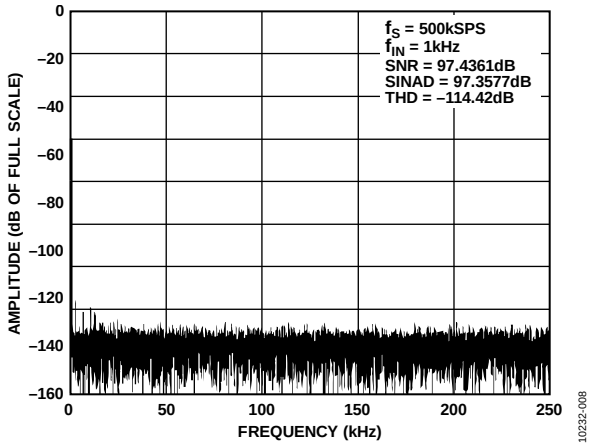


Figure 7. AD7989-5 Fast Fourier Transform (FFT) Plot

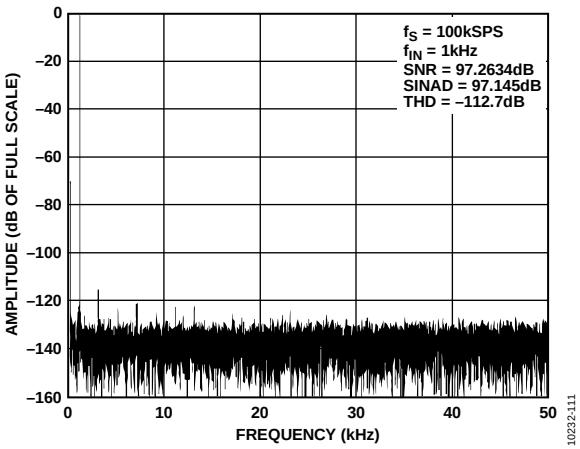


Figure 10. AD7989-1 FFT Plot

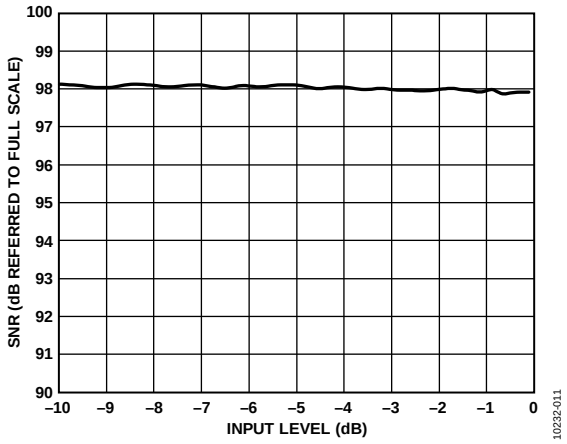


Figure 11. SNR vs. Input Level

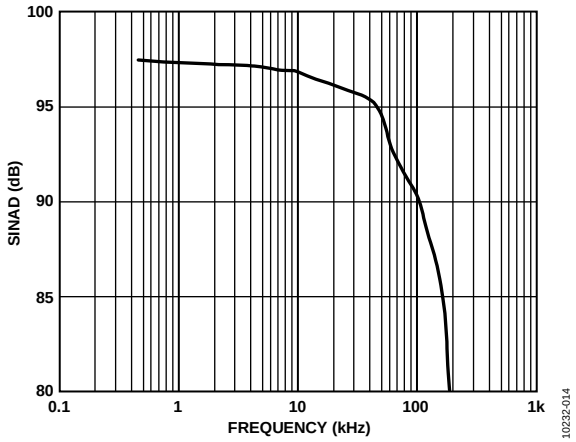


Figure 14. SINAD vs. Frequency

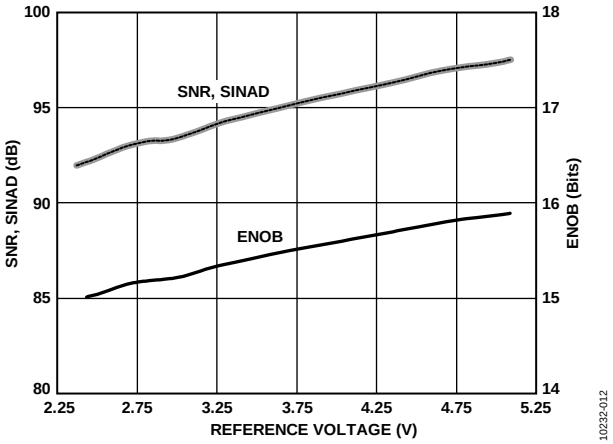


Figure 12. SNR, SINAD, and ENOB vs. Reference Voltage

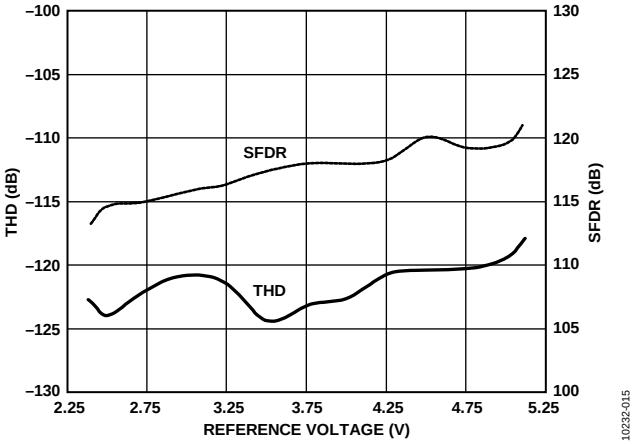


Figure 15. THD and SFDR vs. Reference Voltage

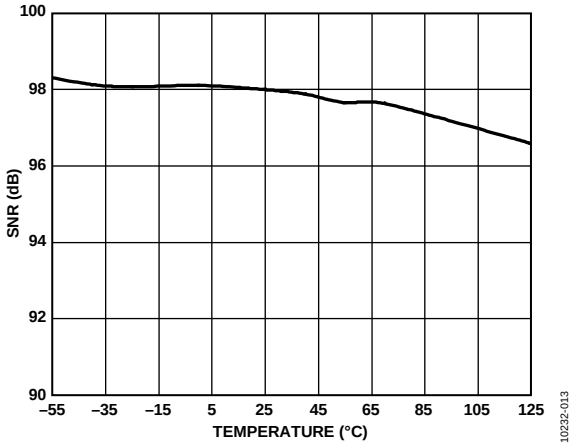


Figure 13. SNR vs. Temperature

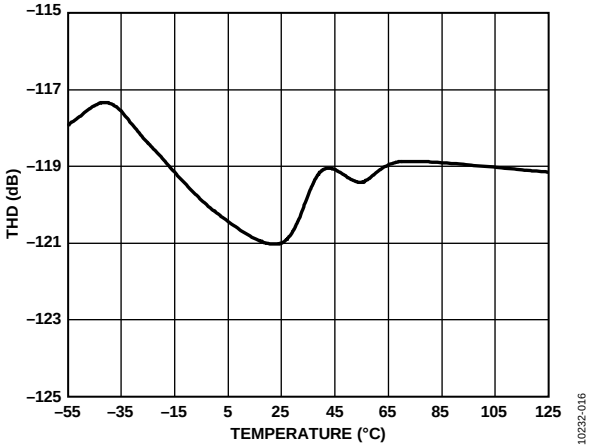


Figure 16. THD vs. Temperature

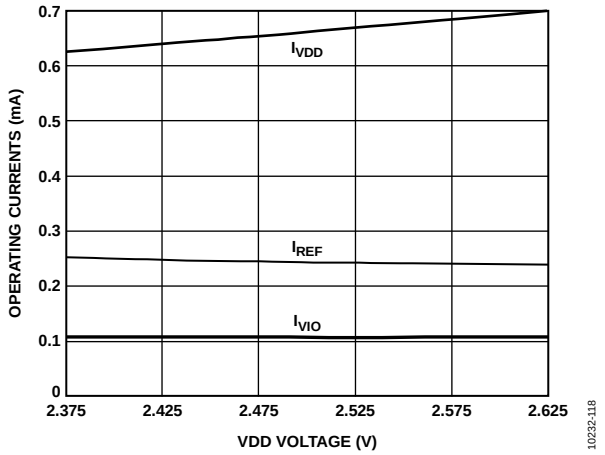


Figure 17. Operating Currents vs. VDD Voltage (AD7989-5)

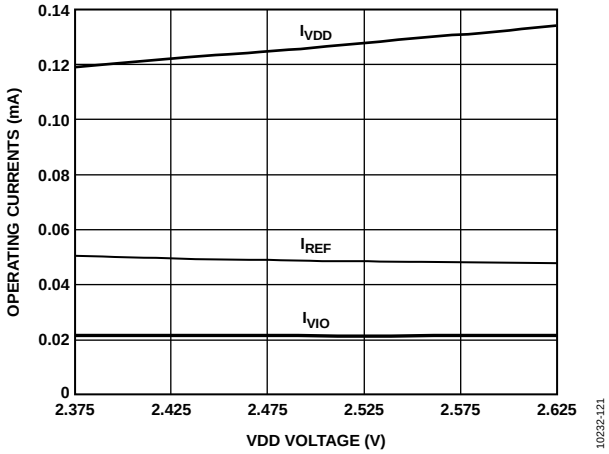


Figure 20. Operating Currents vs. VDD Voltage (AD7989-1)

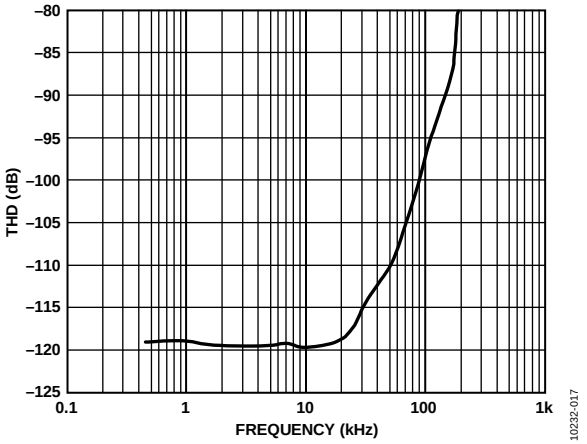


Figure 18. THD vs. Frequency

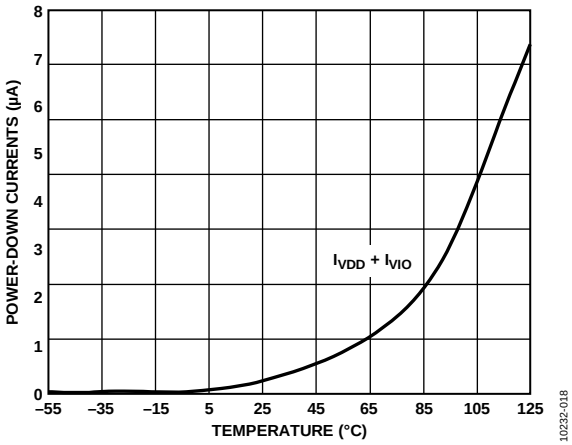


Figure 21. Power-Down Currents vs. Temperature

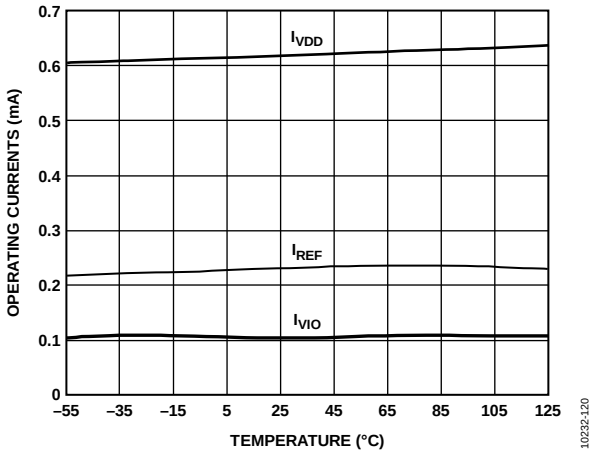


Figure 19. Operating Currents vs. Temperature (AD7989-5)

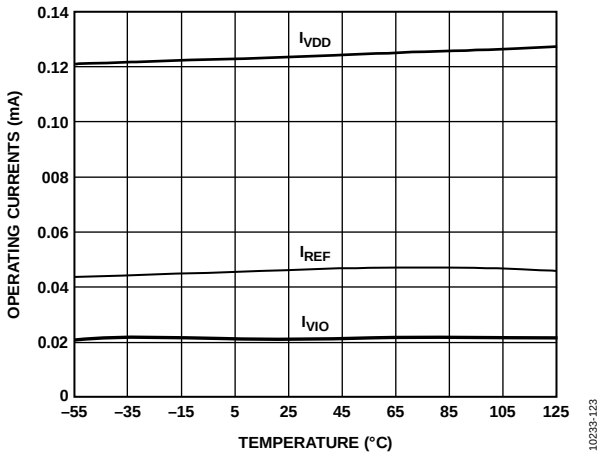


Figure 22. Operating Currents vs. Temperature (AD7989-1)

TERMINOLOGY

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 24).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
Zero error is the difference between the ideal midscale voltage, that is, 0 V, and the actual voltage producing the midscale output code, that is, 0 LSB.

Gain Error
The first code transition (from 100 … 00 to 100 …01) occurs at a level ½ LSB above nominal negative full scale (−4.999981 V for the ±5 V range). The last transition (from 011 … 10 to 011 … 11) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.999943 V for the ±5 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD as follows:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Noise Free Code Resolution
Noise free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as

$$Noise\ Free\ Code\ Resolution = \log_2(2^N/Peak\text{-}to\text{-}Peak\ Noise)$$

and is expressed in bits.

Effective Resolution
Effective resolution is calculated as

$$Effective\ Resolution = \log_2(2^N/RMS\ Input\ Noise)$$

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels. It is measured with a signal at −60 dB so it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay
Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

THEORY OF OPERATION

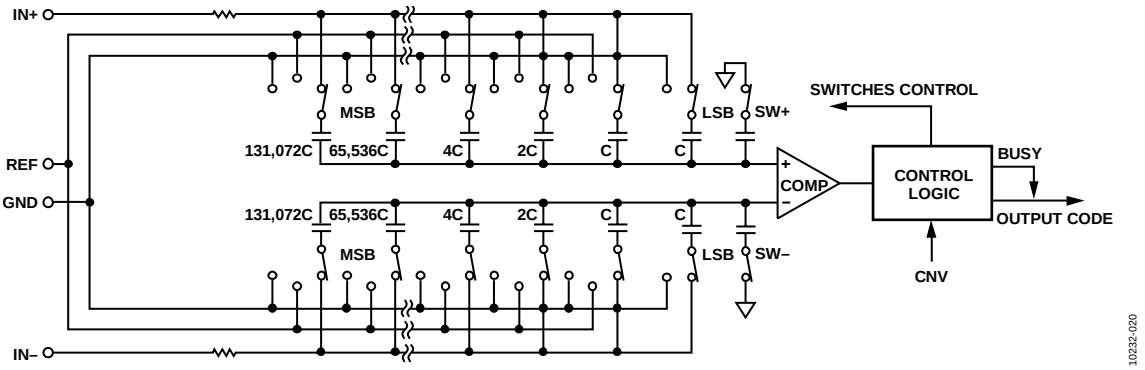


Figure 23. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7989-1/AD7989-5 are high speed, low power, single-supply, precise, 18-bit ADCs using a successive approximation architecture.

The AD7989-1 is capable of converting 100,000 samples per second (100 kSPS), whereas the AD7989-5 is capable of converting 500,000 samples per second (500 kSPS), and they power down between conversions. When operating at 100 kSPS, the ADC typically consumes 700 µW, making the AD7989-1 ideal for battery-powered applications.

The AD7989-1/AD7989-5 provide the user with an on-chip track-and-hold amplifier and do not exhibit any pipeline delay or latency, making these devices ideal for multiple multiplexed channel applications.

The AD7989-1/AD7989-5 can be interfaced to any 1.8 V to 5 V digital logic family. It is available in a 10-lead MSOP or a tiny 10 lead LFCSP that allows space savings and flexible configurations.

CONVERTER OPERATION

The AD7989-1/AD7989-5 are a successive approximation ADCs based on a charge redistribution digital-to-analog converter (DAC). Figure 23 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 18 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via Switch SW+ and Switch SW−. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ input and IN− input. When the acquisition phase completes and the CNV input goes high, a conversion phase initiates. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays then disconnect from the inputs and connect to the GND input. Therefore, the differential voltage between the IN+ and IN− inputs captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ ... $V_{REF}/262,144$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase, and the control logic generates the ADC output code.

Because the AD7989-1/AD7989-5 have an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7989-1/AD7989-5 is shown in Figure 24 and Table 8.

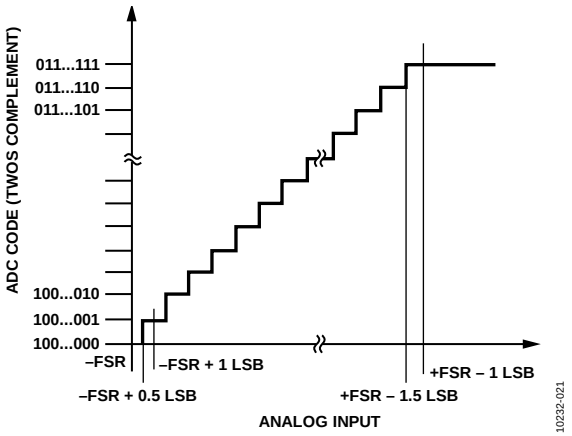


Figure 24. ADC Ideal Transfer Function

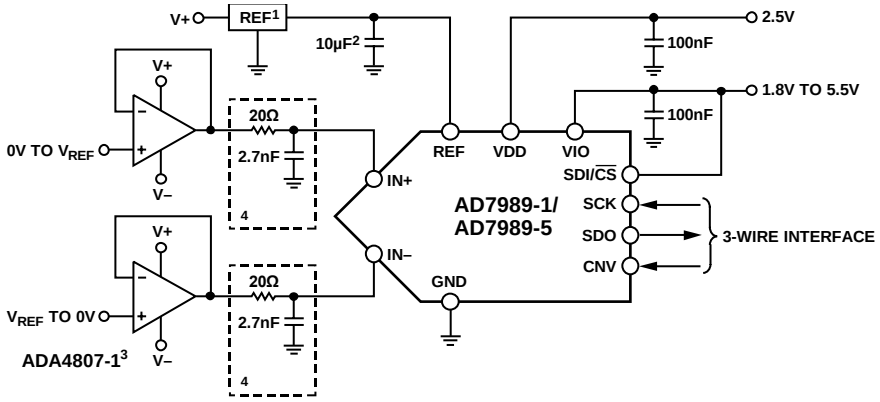
Table 8. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code (Hex)
+FSR – 1 LSB	+4.999962 V	0x1FFFF[1]
Midscale + 1 LSB	+38.15 µV	0x00001
Midscale	0 V	0x00000
Midscale – 1 LSB	–38.15 µV	0x3FFFF
–FSR + 1 LSB	–4.999962 V	0x20001
–FSR	–5 V	0x20000[2]

[1] This is also the code for an overranged analog input ($V_{IN+} – V_{IN-}$ above $V_{REF} – V_{GND}$).
[2] This is also the code for an underranged analog input ($V_{IN+} – V_{IN-}$ below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 25 shows an example of the recommended connection diagram for the AD7989-1/AD7989-5 when multiple supplies are available.



[1]SEE THE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
[2]C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
SEE THE RECOMMENDED LAYOUT IN FIGURE 39 AND FIGURE 40.
[3]SEE THE DRIVER AMPLIFIER CHOICE SECTION.
[4]RECOMMENDED FILTER CONFIGURATION. SEE THE ANALOG INPUTS SECTION.

Figure 25. Typical Application Diagram with Multiple Supplies

ANALOG INPUTS

Figure 26 shows an equivalent circuit of the input structure of the AD7989-1/AD7989-5.

The two diodes, D1 and D2, provide electrostatic discharge (ESD) protection for the IN+ analog input and IN− analog input. Ensure the analog input signal does not exceed the reference input voltage (REF) by more than 0.3 V. If the analog input signal exceeds this level, the diodes become forward-biased and begin conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer (for example, the supplies of the ADA4807-1 in Figure 25) are different from those of REF, the analog input signal can eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short circuit), the current limitation can protect the device.

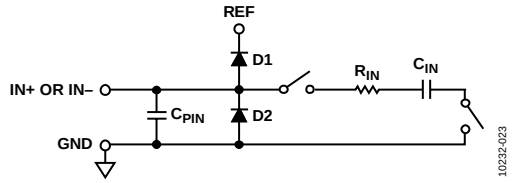


Figure 26. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected.

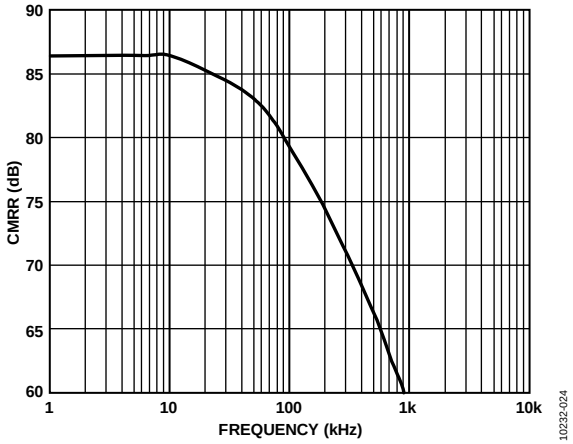


Figure 27. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of Capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor.

During the sampling phase when the switches are closed, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits noise.

When the source impedance of the driving circuit is low, the AD7989-1/AD7989-5 can be driven directly.

Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7989-1/AD7989-5 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7989-1/AD7989-5. The noise from the driver is filtered by the one-pole, low-pass filter of the AD7989-1/AD7989-5 analog input circuit made by R_{IN} and C_{IN} or by the external filter, if one is used. Because the typical noise of the AD7989-1/AD7989-5 is 40 µV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left(\frac{40}{\sqrt{40^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)$$

- where:
  f_{-3dB} is the input bandwidth, in megahertz, of the AD7989-1/AD7989-5 (10 MHz) or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the op amp in nV/√Hz.
- For ac applications, use a driver with a THD performance commensurate with the AD7989-1/AD7989-5.
- For multichannel, multiplexed applications, the driver amplifier and the AD7989-1/AD7989-5 analog input circuit must settle for a full-scale step onto the capacitor array at an 18-bit level (0.0004%, 4 ppm). In the data sheet of the amplifier, settling at 0.1% to 0.01% is more commonly specified. This settling can differ significantly from the settling time at an 18-bit level and must be verified prior to driver selection.

Table 9. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4805-1/ ADA4805-2	Low noise, small size, and low power
ADA4807-1/ ADA4807-2	Very low noise and high frequency
ADA4841-1/ ADA4841-2	Low noise, low distortion and low power
ADA4941-1	Very low noise, low power single-to-differential
ADA4945-1	Low noise, low distortion, fully differential
LTC6363	Low power, low noise, fully differential

SINGLE-ENDED TO DIFFERENTIAL DRIVER

For applications using a single-ended analog signal, either bipolar or unipolar, the ADA4941-1 single-ended to differential driver allows a differential input to the device. The schematic is shown in Figure 28.

R1 and R2 set the attenuation ratio between the input range and the ADC voltage range (V_{REF}). R1, R2, and C_F are chosen depending on the desired input resistance, signal bandwidth, antialiasing, and noise contribution. For example, for the ±10 V range with a 4 kΩ impedance, R2 = 1 kΩ and R1 = 4 kΩ.

R3 and R4 set the common mode on the IN− input, and R5 and R6 set the common mode on the IN+ input of the ADC. Ensure the common mode is close to $V_{REF}/2$. For example, for the ±10 V range with a single supply, R3 = 8.45 kΩ, R4 = 11.8 kΩ, R5 = 10.5 kΩ, and R6 = 9.76 kΩ.

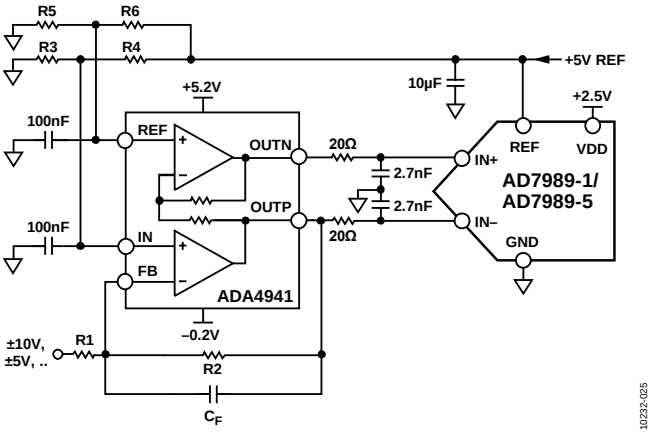


Figure 28. Single-Ended to Differential Driver Circuit

VOLTAGE REFERENCE INPUT

The AD7989-1/AD7989-5 voltage reference input, REF, has a dynamic input impedance and must, therefore, be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source (for example, a reference buffer using the AD8031, the ADA4805-1, or the ADA4807-1), a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If using an unbuffered reference voltage, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift reference, such as the ADR435, ADR445, LTC6655, or ADR4550.

If desired, use a reference decoupling capacitor with values as small as 2.2 µF with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

POWER SUPPLY

The AD7989-1/AD7989-5 use two power supply pins: a core supply (VDD) and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and 5.5 V. To reduce the number of supplies needed, tie VIO and VDD together. When VIO is greater than or equal to VDD, the AD7989-1/AD7989-5 are insensitive to power supply sequencing. In normal operation, if the magnitude of VIO is less than the magnitude of VDD, VIO must be applied before VDD. Additionally, they are insensitive to power supply variations over a wide frequency range, as shown in Figure 29.

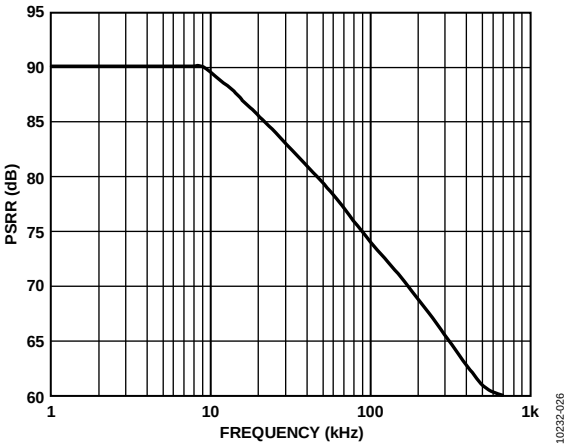


Figure 29. PSRR vs. Frequency

The AD7989-1/AD7989-5 power down automatically at the end of each conversion phase.

DIGITAL INTERFACE

Although the AD7989-1/AD7989-5 have a reduced number of pins, they offer flexibility in their serial interface modes.

When in $\overline{CS}$ mode, the AD7989-1/AD7989-5 are compatible with SPI, queued serial peripheral interface (QSPI), digital hosts, and digital signal processors (DSPs). In this mode, the AD7989-1/AD7989-5 can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections, which is useful, for instance, in isolated applications. A 4-wire interface using the SDI/$\overline{CS}$, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

When in chain mode, the AD7989-1/AD7989-5 provide a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line, similar to a shift register.

The mode in which the device operates depends on the SDI/$\overline{CS}$ level when the CNV rising edge occurs. $\overline{CS}$ mode is selected if SDI/$\overline{CS}$ is high, and chain mode is selected if SDI/$\overline{CS}$ is low. The SDI/$\overline{CS}$ hold time is such that when SDI/$\overline{CS}$ and CNV are connected together, chain mode is always selected. The user must timeout the maximum conversion time prior to readback.

$\overline{CS}$ MODE, 3-WIRE

This mode is usually used when a single AD7989-1/AD7989-5 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 30, and the corresponding timing is given in Figure 31.

With SDI/$\overline{CS}$ tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance.

When the conversion is complete, the AD7989-1/AD7989-5 enter the acquisition phase and power down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that it has an acceptable hold time. After the 18th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

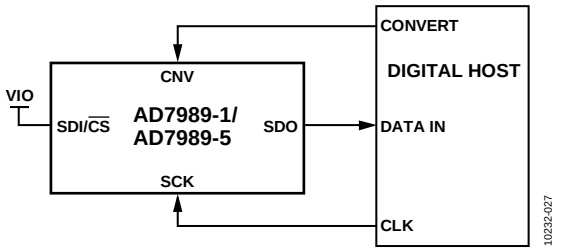


Figure 30. $\overline{CS}$ Mode, 3-Wire Connection Diagram (SDI High)

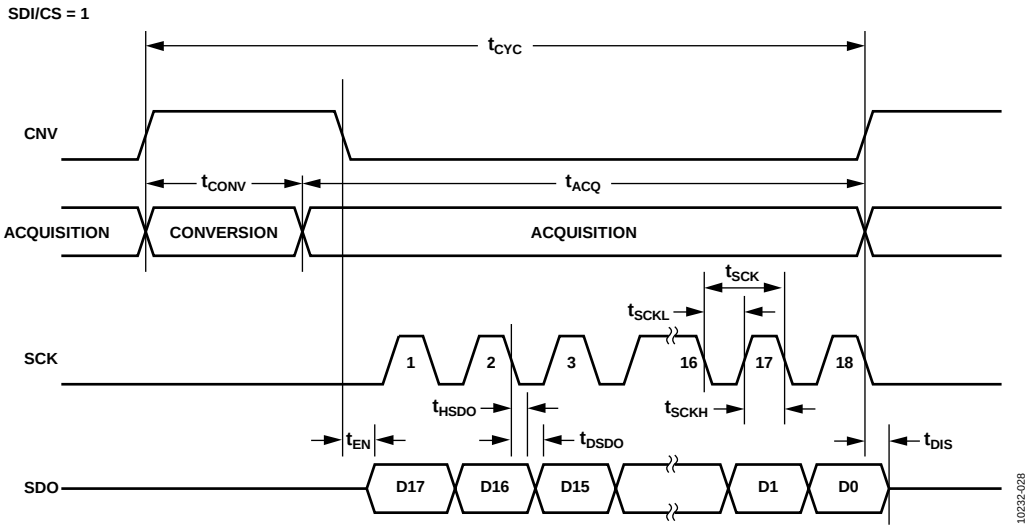


Figure 31. $\overline{CS}$ Mode, 3-Wire Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 4-WIRE

This mode is usually used when multiple AD7989-1/AD7989-5 devices are connected to an SPI-compatible digital host.

A connection diagram example using two AD7989-1/AD7989-5 devices is shown in Figure 32, and the corresponding timing is given in Figure 33.

With SDI high, a rising edge on CNV initiates a conversion, selects SDI/$\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. If SDI/$\overline{CS}$ and CNV are low, SDO is driven low.

Prior to the minimum conversion time, SDI/$\overline{CS}$ can select other SPI devices, such as analog multiplexers, but SDI/$\overline{CS}$ must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time.

When the conversion is complete, the AD7989-1/AD7989-5 enter the acquisition phase and power down. Each ADC result can be read by bringing its SDI/$\overline{CS}$ input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 18th SCK falling edge or when SDI/$\overline{CS}$ goes high (whichever occurs first), SDO returns to high impedance and another AD7989-1/AD7989-5 can be read.

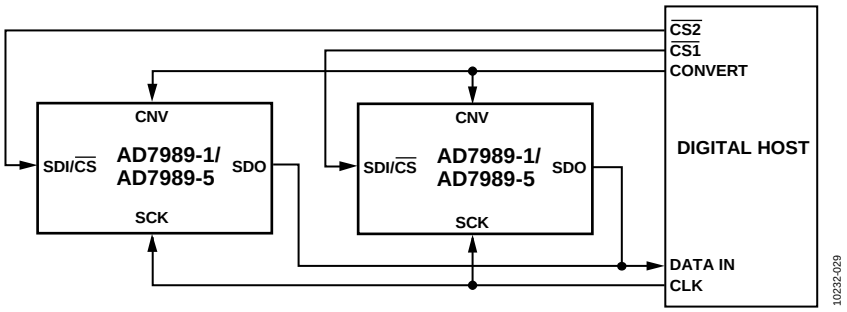


Figure 32. $\overline{CS}$ Mode, 4-Wire Connection Diagram

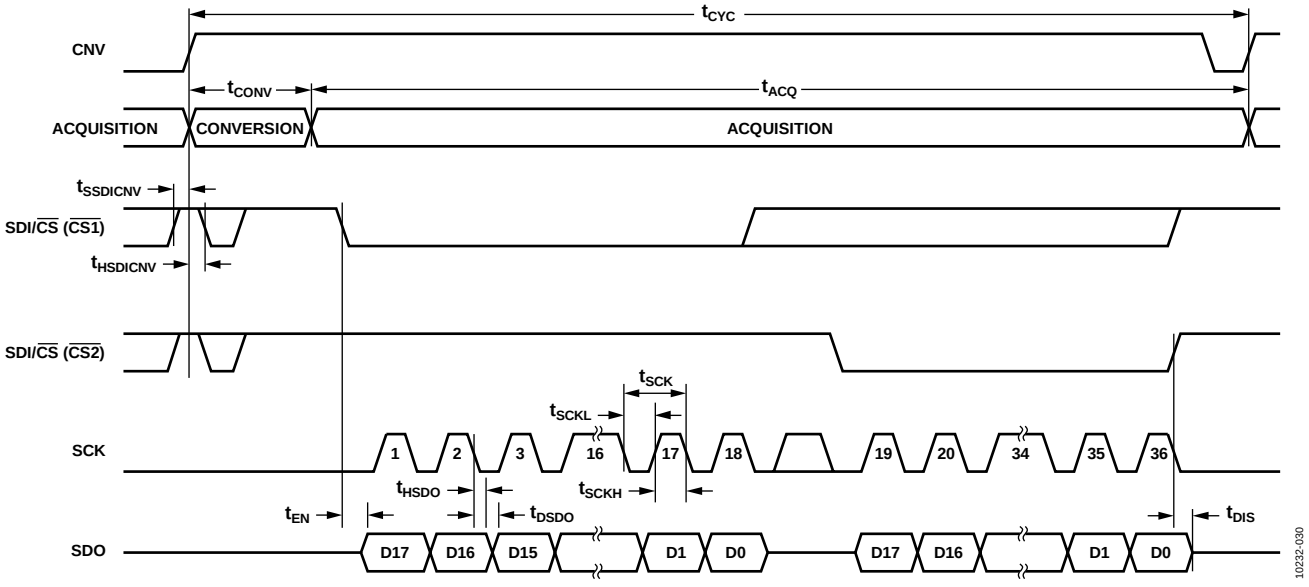


Figure 33. $\overline{CS}$ Mode, 4-Wire Serial Interface Timing

CHAIN MODE

This mode can daisy-chain multiple AD7989-1/AD7989-5 devices on a 3-wire serial interface. This feature reduces component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7989-1/AD7989-5 devices is shown in Figure 34, and the corresponding timing is given in Figure 35.

When SDI/$\overline{CS}$ and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, and selects the chain mode.

In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7989-1/AD7989-5 enter the acquisition phase and power down. The remaining data bits stored in the internal shift register are clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 18 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7989-1/AD7989-5 devices in the chain, provided that the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time.

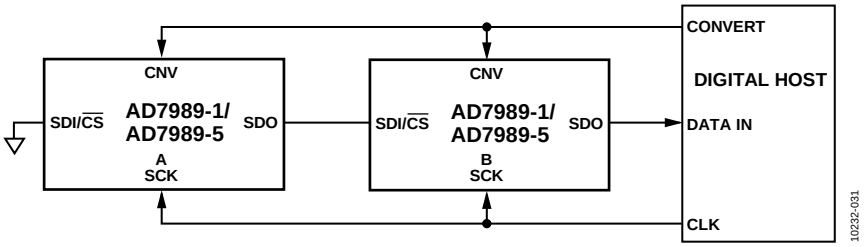


Figure 34. Chain Mode Connection Diagram

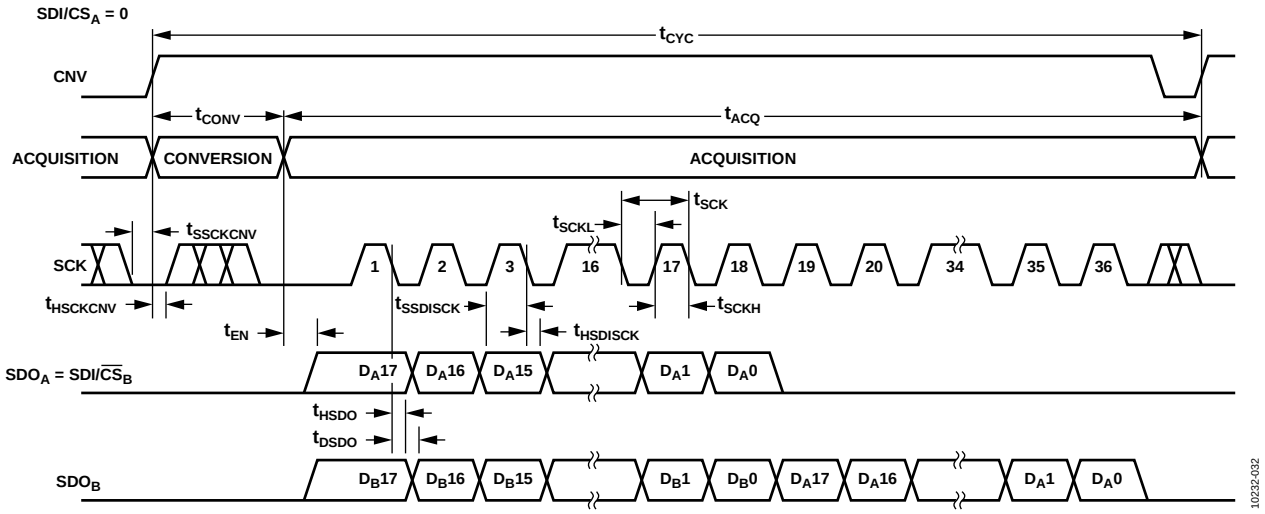


Figure 35. Chain Mode Serial Interface Timing

APPLICATIONS INFORMATION

INTERFACING TO BLACKFIN® DSP

The AD7989-1/AD7989-5 can easily connect to a DSP, SPI, or SPORT. The SPI configuration is straightforward using the standard SPI interface, as shown in Figure 36.

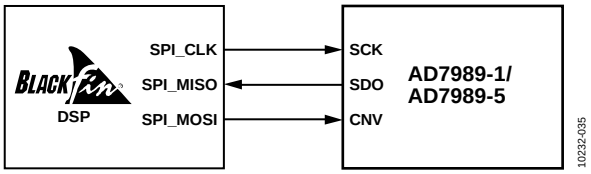


Figure 36. Typical Connection to Blackfin SPI Interface

Similarly, the SPORT interface can interface to this ADC. The SPORT interface has some benefits in that it can use direct memory access (DMA) and provides a lower jitter CNV signal generated from a hardware counter.

Some glue logic may be required between SPORT and the AD7989-1/AD7989-5 interface. The EVAL-AD7989-5SDZ evaluation board for the AD7989-1/AD7989-5 interfaces directly to the SPORT of the Blackfin-based (ADSP-BF527) SDP board. The configuration used for the SPORT interface requires the addition of some glue logic as shown in Figure 37. The SCK input to the ADC was gated off when CNV was high to keep the SCK line static while converting the data, thereby ensuring the best integrity of the result. This approach uses an AND gate and a NOT gate for the SCK path. The other logic gates used on the RSCLK and RFS paths are for delay matching purposes and may not be necessary when path lengths are short.

This is one approach to using the SPORT interface for the AD7989-1/AD7989-5 ADC; there can be other solutions similar to this approach.

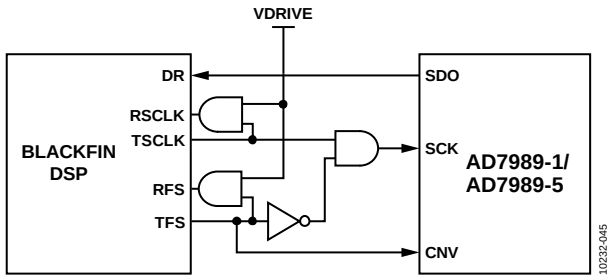


Figure 37. The EVAL-AD7989-5SDZ Evaluation Board Connection to Blackfin SPORT Interface

LAYOUT

The printed circuit board (PCB) that houses the AD7989-1/AD7989-5 must be designed so the analog and digital sections are separated and confined to certain areas of the PCB. The pinout of the AD7989-1/AD7989-5, with its analog signals on the left side and its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7989-1/AD7989-5 is used as a shield. Do not run fast switching signals, such as CNV or clocks, near analog signal paths. Avoid crossover of digital and analog signals.

Using at least one ground plane is recommended. The ground plane can be common or split between the digital and analog sections. In the latter case, join the planes underneath the AD7989-1/AD7989-5 devices.

The AD7989-1/AD7989-5 voltage reference input, REF, has a dynamic input impedance. Decouple REF with minimal parasitic inductances by placing the reference decoupling ceramic capacitor close to, but ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Finally, decouple the power supplies of the AD7989-1/AD7989-5, VDD and VIO, with ceramic capacitors, typically 100 nF, placed close to the AD7989-1/AD7989-5 and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

An example of a layout following these rules is shown in Figure 38 and Figure 39.

EVALUATING AD7989-1/AD7989-5 PERFORMANCE

Other recommended layouts for the AD7989-1/AD7989-5 are outlined in UG-340 user guide for the EVAL-AD7989-5SDZ. The evaluation board package includes a fully assembled and tested evaluation board, the user guide, and software for controlling the evaluation board from a PC via the EVAL-SDP-CB1Z.

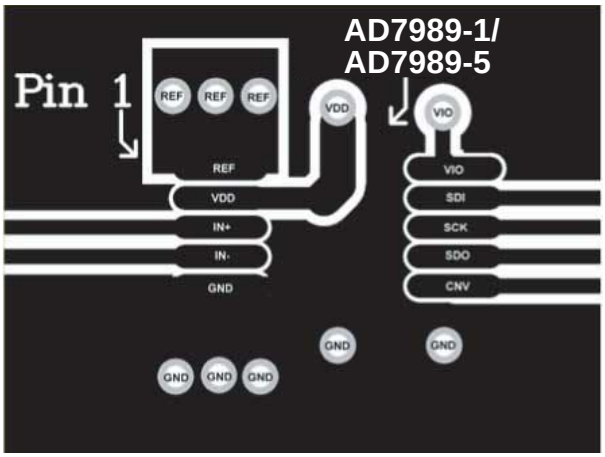


Figure 38. Recommended Layout of the AD7989-1/AD7989-5 (Top Layer)

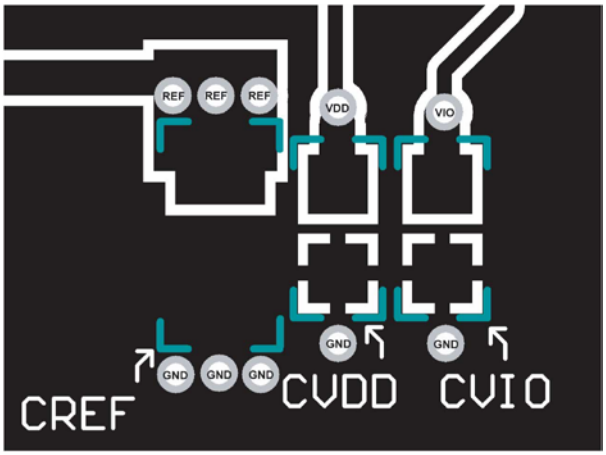


Figure 39. Recommended Layout of the AD7989-1/AD7989-5 (Bottom Layer)

OUTLINE DIMENSIONS

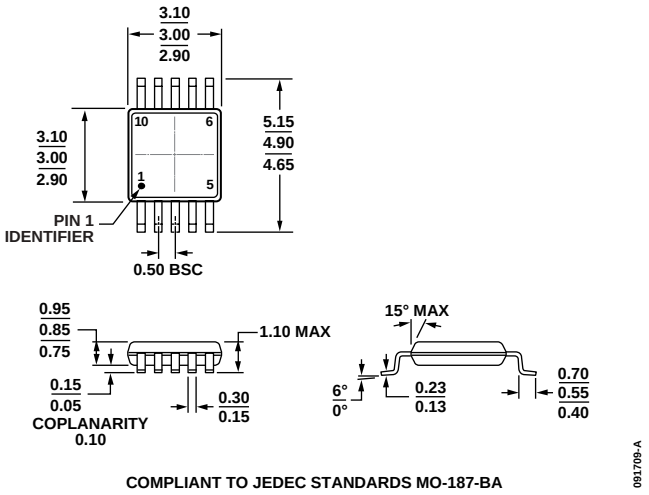


Figure 40. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

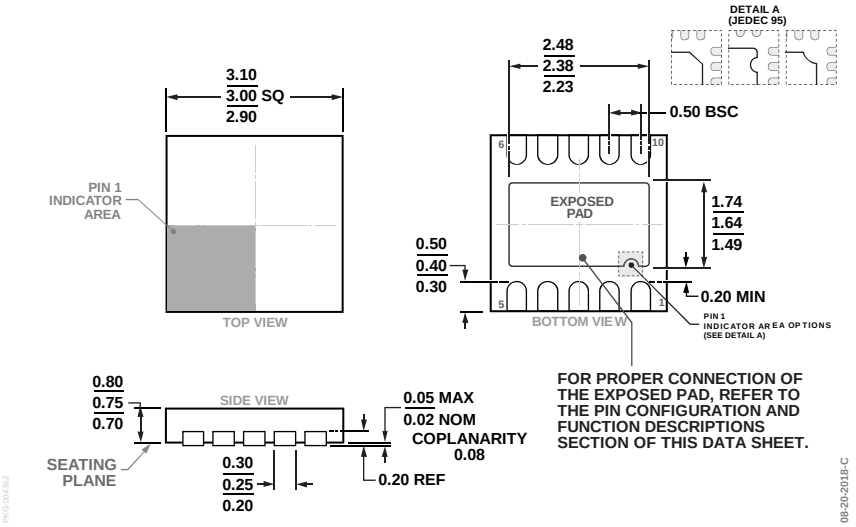


Figure 41. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body, Very Very Thin, Dual Lead (CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
AD7989-1BRMZ	−40°C to +85°C	10-Lead MSOP, Tube	RM-10	C76	50
AD7989-1BRMZ-RL7	−40°C to +85°C	10-Lead MSOP, 7″ Tape and Reel	RM-10	C76	1,000
AD7989-1BCPZ-RL7	−40°C to +85°C	10-Lead LFCSP, 7″ Tape and Reel	CP-10-9	C80	1,500
AD7989-1BCPZ-R2	−40°C to +85°C	10-Lead LFCSP	CP-10-9	C80	250
AD7989-5BRMZ	−40°C to +85°C	10-Lead MSOP, Tube	RM-10	C7N	50
AD7989-5BRMZ-RL7	−40°C to +85°C	10-Lead MSOP, 7″ Tape and Reel	RM-10	C7N	1,000
AD7989-5BCPZ-RL7	−40°C to +85°C	10-Lead LFCSP, 7″ Tape and Reel	CP-10-9	C7Y	1,500
AD7989-5BCPZ-R2	−40°C to +85°C	10-Lead LFCSP	CP-10-9	C7Y	250
EVAL-AD7989-5SDZ		Evaluation Board with AD7989-5 Populated; Use for Evaluation of Both AD7989-1 and AD7989-5			
EVAL-SDP-CB1Z		System Demonstration Board, Used as a Controller Board for Data Transfer via USB Interface to PC			

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7989-5SDZ board can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CB1Z for evaluation/demonstration purposes.
[3] The EVAL-SDP-CB1Z board allows a PC to control and communicate with all Analog Devices, Inc., evaluation boards ending in the SD designator.

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