Selection Guide

Part Number	Packing
A3908EEETR-T	Tape and reel, 3000 pieces/reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}		–	–	6	V
Logic Input Voltage Range	V_{IN}		–0.3	–	6	V
Output Current	I_{OUT}				500	mA
Junction Temperature	T_J		–	–	150	°C
Storage Temperature Range	T_{stg}		–40	–	150	°C
Operating Temperature Range	T_A	Range E	–40	–	85	°C

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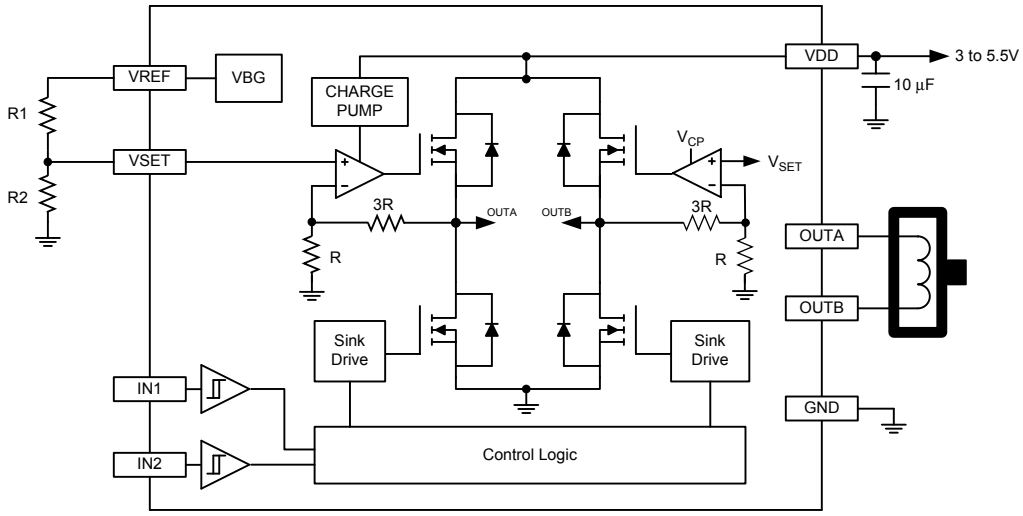
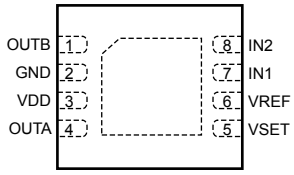
Functional Block Diagram



Terminal Diagram



(Top View)

Number	Name	Description
1	OUTB	Motor terminal
2	GND	Ground
3	VDD	Input supply
4	OUTA	Motor terminal
5	VSET	Select source-side output voltage
6	VREF	Bandgap reference
7	IN1	Control logic input
8	IN2	Control logic input

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ELECTRICAL CHARACTERISTICS at T_A=25°C, and V_{DD} = 3 to 5.5 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Current	I_{DD}		–	0.5	2	mA
	I_{DDSTB}	Standby mode	–	–	500	nA
UVLO Enable Threshold	V_{DDUVLO}	V_{DD} rising	–	–	2.6	V
UVLO Hysteresis	V_{UVHYS}		–	120	–	mV
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing.	–	165	–	°C
Thermal Shutdown Hysteresis	T_{JHYS}	Recovery = T_{JTSD} – T_{JHYS}	–	15	–	°C
Logic Input Low Level	V_{IL}		–	–	V_{DD} x 20%	V
Logic Input High Level	V_{IH}		V_{DD} x 55%	–	–	V
Input Hysteresis	V_{HYS}		–	V_{DD} x 7%	–	mV
Logic Input Current	I_{IN}	V_{IN} = 0 to 5 V	–1	0	1	µA
Output Driver						
Sink Driver Output Resistance	R_{DS}	V_{DD} = 5 V, I_{OUT} = 500 mA	–	0.6	–	Ω
		V_{DD} = 3 V, I_{OUT} = 500 mA	–	0.8	–	Ω
Source Driver On Resistance	$R_{DS(on)}$	V_{DD} = 5 V, I_{OUT} = 500 mA	–	0.6	–	Ω
		V_{DD} = 3 V, I_{OUT} = 500 mA	–	0.65	–	Ω
Bandgap Reference	VBG		1.235	1.285	1.335	V
V_{OUT} Accuracy (V_{OUTA} –V_{OUTB})	V_{OUT}	V_{SET} = 1.2 V	4.608	4.8	4.992	V
		V_{SET} = 825 mV	3.135	3.3	3.465	V
		V_{SET} = 500 mV	1.84	2	2.16	V

THERMAL CHARACTERISTICS

Characteristics	Symbol	Test Conditions	Rating	Unit
Package Thermal Resistance*	$R_{\theta JA}$	Measured on 4-layer board based on JEDEC standard	49	°C/W

*Additional thermal information is available on the Allegro Web site.

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Functional Description

Voltage Regulation The A3908 regulates the voltage across the motor coil. The voltage across the OUTA and OUTB terminal is sensed and compared to an internal threshold voltage. The high-side switch will be driven in linear mode to keep the applied voltage maintained at the calculated level, as follows:

$$V_{OUT} = 4 \times V_{REF} (R_2 / [R_1 + R_2]) ,$$

where V_{REF} (VBG) is 1.285 V typical.

Then, for forward mode:

$$V_{OUT} = V_{OUTA} - V_{OUTB} ,$$

and for reverse mode:

$$V_{OUT} = V_{OUTB} - V_{OUTA} .$$

The alternative method is to provide a tightly regulated voltage to the motor supply pin and run the source and sink drivers as switches. The voltage drop across these switches will vary linearly with temperature and current, therefore the voltage across the motor coil also will vary. The A3908 will eliminate these sources of error for a system where controlling the motor voltage is the optimum means of control.

Thermal Shutdown The A3908 will disable the outputs if the junction temperature, T_J , reaches 165°C. There is 15°C of hysteresis, so when the junction temperature drops below 150°C, the device will begin to operate normally.

Dropout Mode The source and sink drivers have a total $R_{DS(on)}$ of approximately 1.2 Ω total. When the motor supply voltage, V_{DD}, drops too low compared to the regulated value, the IC enters dropout mode. In this case, the voltage across the motor coil will be:

$$V_{MOTOR} = V_{DD} - I_{LOAD} (R_{DS(sink)} + R_{DS(src)})$$

Brake Mode When both inputs are high, the A3908 goes into high-side brake mode (turns on both source drivers). There is no protection during braking, so care must be taken to ensure that the peak current does not exceed the absolute maximum current, I_{OUT}.

Standby Mode To minimize battery drain, standby mode will turn off all of the circuitry and draw typically less than 100 nA from the VDD line. There will be a very short delay, approximately 2 µs, before enabling the output drivers after release of standby mode.

Power Dissipation. Power can be approximated based on the below three components:

$$P_{D(src)} = I_{LOAD} (V_{DD} - V_{REG}) ,$$

$$P_{D(sink)} = I_{LOAD} \times R_{DS(sink)} , \text{ and}$$

$$P_{bias} = V_{DD} \times I_{DD}.$$

Control Logic Table

Settings				Resulting Mode
IN1	IN2	OUTA	OUTB	
0	0	Off	Off	Standby
0	1	Low	V_{REG}	Reverse
1	0	V_{REG}	Low	Forward
1	1	High	High	Brake

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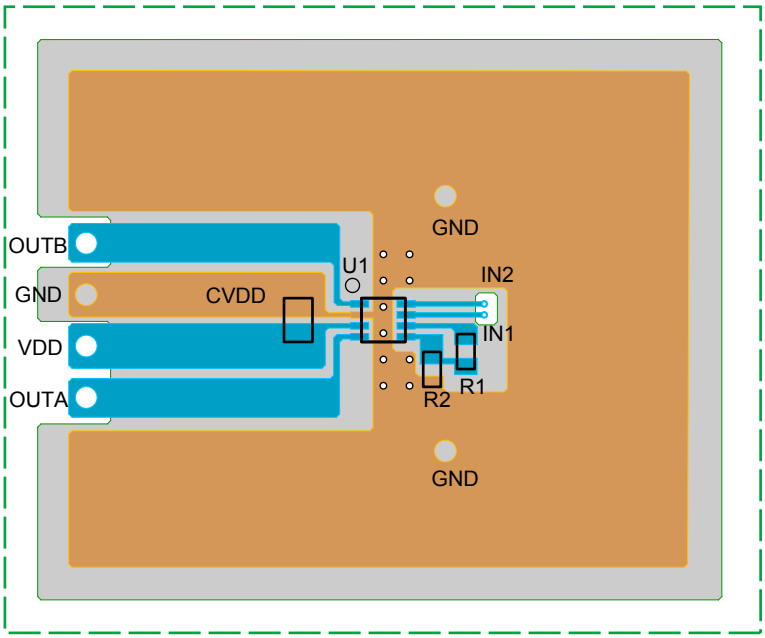
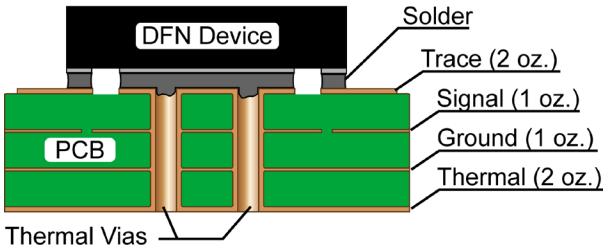
Application Information

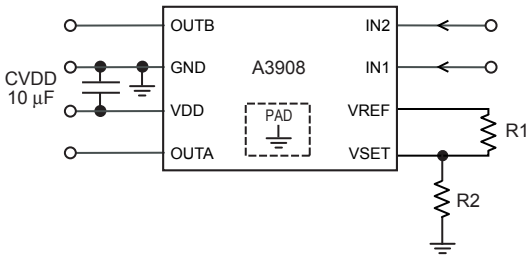
Layout

The printed circuit board should use a heavy groundplane for optimum thermal performance. The A3908 must be soldered directly onto the board. On the underside of the A3908 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB. Thermal vias should not have any thermal relief and should be connected to internal layers, if available, to maximize the dissipation area.

Grounding In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance, single-point ground, known as a *star ground*, located very close to the device. By making the connection between the exposed thermal pad and the groundplane directly under the A3908, that area becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during PWM operation and ensure that the supply voltage remains stable at the input terminal. Bulk capacitance is often located at a non-ideal distance from the device. If the recommended capacitance of 10 µF cannot be located very close to the supply terminal on the A3908, it is recommended that a 0.1 µF capacitor be placed as close to the VDD terminal as possible to provide a path for transient currents.







A3908 Evaluation Board

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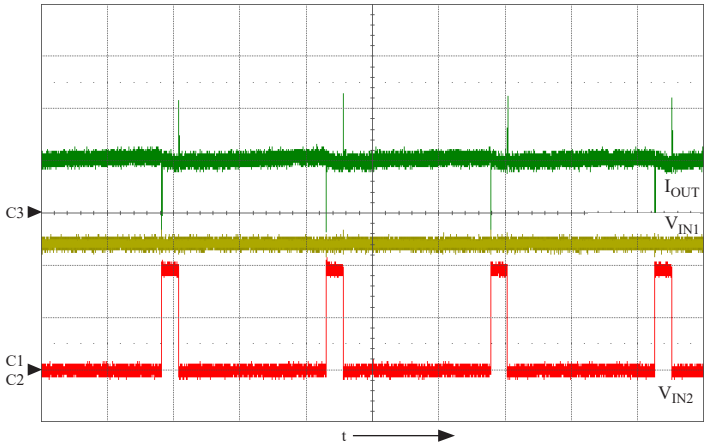
PWM Operation

In some applications current control may be desired. Pulse width modulating the inputs will allow the output current to be regulated. When external PWM control is used, the VREF pin should be connected directly to the VSET pin. This effectively disables voltage control on the source driver, and allows maximum current to flow through the driver. Current is then controlled using *enable chopping*, described below.

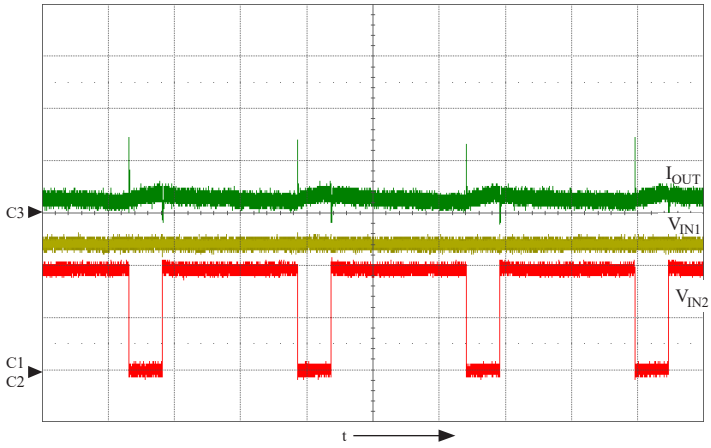
Enable Chopping By PWMing the logic inputs between enable and brake modes, the current in the motor winding can be controlled. It is accomplished by holding one input high while PWMing the other input. During the on-cycle, current flows in the bridge consistent with the direction programmed on the input pins. During the off-cycle, the A3908 enters brake mode. Enable chopping is illustrated in figure 1.

Current in the motor winding is controlled by changing the duty cycle on the PWM input. As shown in figure 2, the average current is still positive but, because the duty cycle is less, the average current is much lower.



Symbol	Parameter	Units/Division
C1	V_{IN1}	2 V
C2	V_{IN2}	2 V
C3	I_{OUT}	100 mA
t	time	20 µs

Figure 1. Enable chopping. Forward direction, output duty cycle 90%.



Symbol	Parameter	Units/Division
C1	V_{IN1}	2 V
C2	V_{IN2}	2 V
C3	I_{OUT}	100 mA
t	time	20 µs

Figure 2. Enable chopping. Forward direction, output duty cycle 20%.

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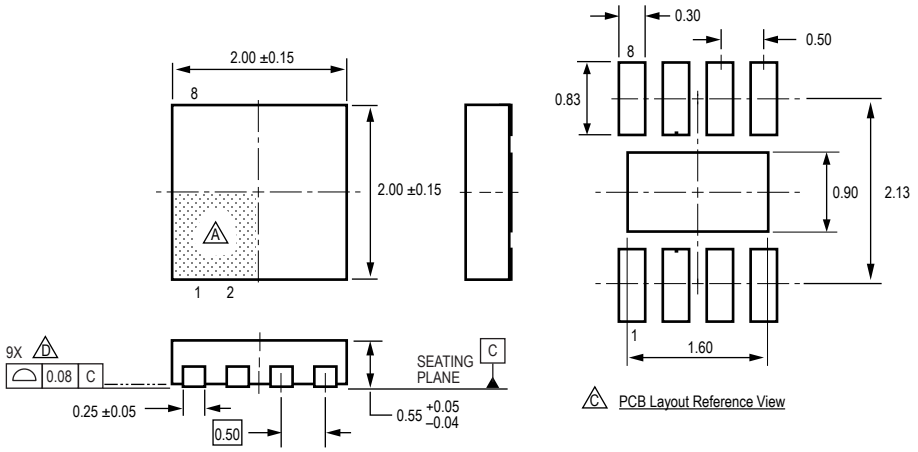
Package EE, 8-contact DFN



All dimensions nominal, not for tooling use
(reference JEDEC MO-229UCCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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Revision History

Number	Date	Description
1	April 10, 2019	Minor editorial updates

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