Description (continued)

achieves industry-leading digital output jitter performance that is critical in high-performance motor commutation applications. An on-chip regulator allows the use of this device over a wide operating voltage range. Post-assembly factory programming at Allegro provides sensitive switch points that are symmetrical between the two switches.

The A1230 is available in a plastic 8-pin SOIC surface-mount package (L) and a plastic 4-pin SIP (K). Both are available in a temperature range of –40°C to 150°C. Each package is lead (Pb) free, with 100% matte-tin-plated leadframe.

Selection Guide

Part Number	Packing*	Mounting	Ambient, T_A
A1230LK-T	Bulk, 500 pieces/bag	4-pin SIP through hole	–40ºC to 150ºC
A1230LLTR-T	13-in. reel, 3000 pieces/reel	8-pin SOIC surface mount	

*Contact Allegro for additional packing options.

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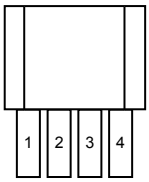
SPECIFICATIONS

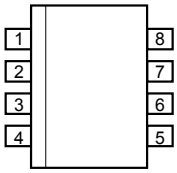
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		26.5	V
Reverse Battery Voltage	V_{RCC}		–16	V
Output Off Voltage	V_{OUTPUT}		V_{CC}	V
Output Sink Current	$I_{OUTPUT(Sink)}$		Internally Limited	–
Magnetic Flux Density	B		Unlimited	–
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pin-Out Diagrams and Terminal List Table



Package K, 4-Pin SIP



Package L, 8-Pin SOIC

Terminal List Table

Pin Number		Name	Function
Package K	Package L		
1	1	VCC	Connects power supply to on-chip voltage regulator
2	2	OUTPUTA	Output from E1 via first Schmitt circuit
3	3	OUTPUTB	Output from E2 via second Schmitt circuit
4	4	GND	Terminal for ground connection
–	5-8	NC	No connection

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OPERATING CHARACTERISTICS: valid over operating temperature ranges unless otherwise noted; typical data applies to V_{CC} = 12 V, and T_A = 25ºC

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage[2]	V_{CC}	Operating; $T_A \le 150°C$	3.3	–	18	V
Output Leakage Current	$I_{OUTPUT(OFF)}$	Either output	–	< 1	10	µA
Supply Current	$I_{CC(OFF)}$	$B < B_{RP(A)}$,$B < B_{RP(B)}$	–	3.5	6.0	mA
	$I_{CC(ON)}$	$B > B_{OP(A)}$,$B > B_{OP(B)}$	–	3.5	6.0	mA
Low Output Voltage	$V_{OUTPUT(ON)}$	Both outputs; $I_{OUTPUT(SINK)}$ = 20 mA; $B > B_{OP(A)}$, $B > B_{OP(B)}$	–	160	500	mV
Output Sink Current	$I_{OUTPUT(SINK)}$		–	–	20	mA
Output Sink Current, Continuous[3]	$I_{OUTPUT(SINK)C}$	$T_J < T_{J(max)}$,V_{OUTPUT} = 12 V	–	–	70	mA
Output Sink Current, Peak[4]	$I_{OUTPUT(SINK)P}$	t < 3 seconds	–	–	220	mA
Chopping Frequency	f_C		–	780	–	kHz
Output Rise Time	t_r	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	1.8	–	µs
Output Fall Time	t_f	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	1.2	–	µs
Power-On Time	t_{ON}	B > 40 G or B < –40 G	–	15	–	µs
Power-Off Time	t_{OFF}	B > 40 G or B < –40 G	–	25	–	µs
Power-On State	POS	B = 0 G	–	Low	–	–
TRANSIENT PROTECTION CHARACTERISTICS						
Supply Zener Voltage	V_Z	I_{CC} = 9 mA, T_A = 25°C	28	–	–	V
Supply Zener Current[5]	I_Z	V_S = 28 V	–	–	9.0	mA
Reverse-Battery Current	I_{RCC}	V_{RCC} = –18 V, $T_J < T_{J(max)}$	–	2	15	mA
MAGNETIC CHARACTERISTICS[6]						
Operate Point: $B > B_{OP}$	$B_{OP(A)}$, $B_{OP(B)}$		–	7	30	G
Release Point: $B < B_{RP}$	$B_{RP(A)}$, $B_{RP(B)}$		–30	–7	–	G
Hysteresis: $B_{OP(A)} – B_{RP(A)}$, $B_{OP(B)} – B_{RP(B)}$	$B_{HYS(A)}$, $B_{HYS(B)}$		5	14	35	G
Symmetry: Channel A, Channel B, $B_{OP(A)} + B_{RP(A)}$, $B_{OP(B)} + B_{RP(B)}$	SYM_A, SYM_B		–35	–	35	G
Operate Symmetry: $B_{OP(A)} – B_{OP(B)}$	$SYM_{AB(OP)}$		–25	–	25	G
Release Symmetry: $B_{RP(A)} – B_{RP(B)}$	$SYM_{AB(RP)}$		–25	–	25	G

[1] 1 G (gauss) = 0.1 mT (millitesla).

[2] When operating at maximum voltage, never exceed maximum junction temperature, T_J(max). Refer to power derating curve charts.

[3] Device will survive the current level specified, but operation within magnetic specification cannot be guaranteed.

[4] Short circuit of the output to VCC is protected for the time duration specified.

[5] Maximum specification limit is equivalent to $I_{CC(max)}$ + 3 mA.

[6] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and as a positive value for south-polarity magnetic fields. This so-called algebraic convention supports arithmetic comparison of north and south polarity values, where the relative strength of the field is indicated by the absolute value of B, and the sign indicates the polarity of the field (for example, a –100 G field and a 100 G field have equivalent strength, but opposite polarity).

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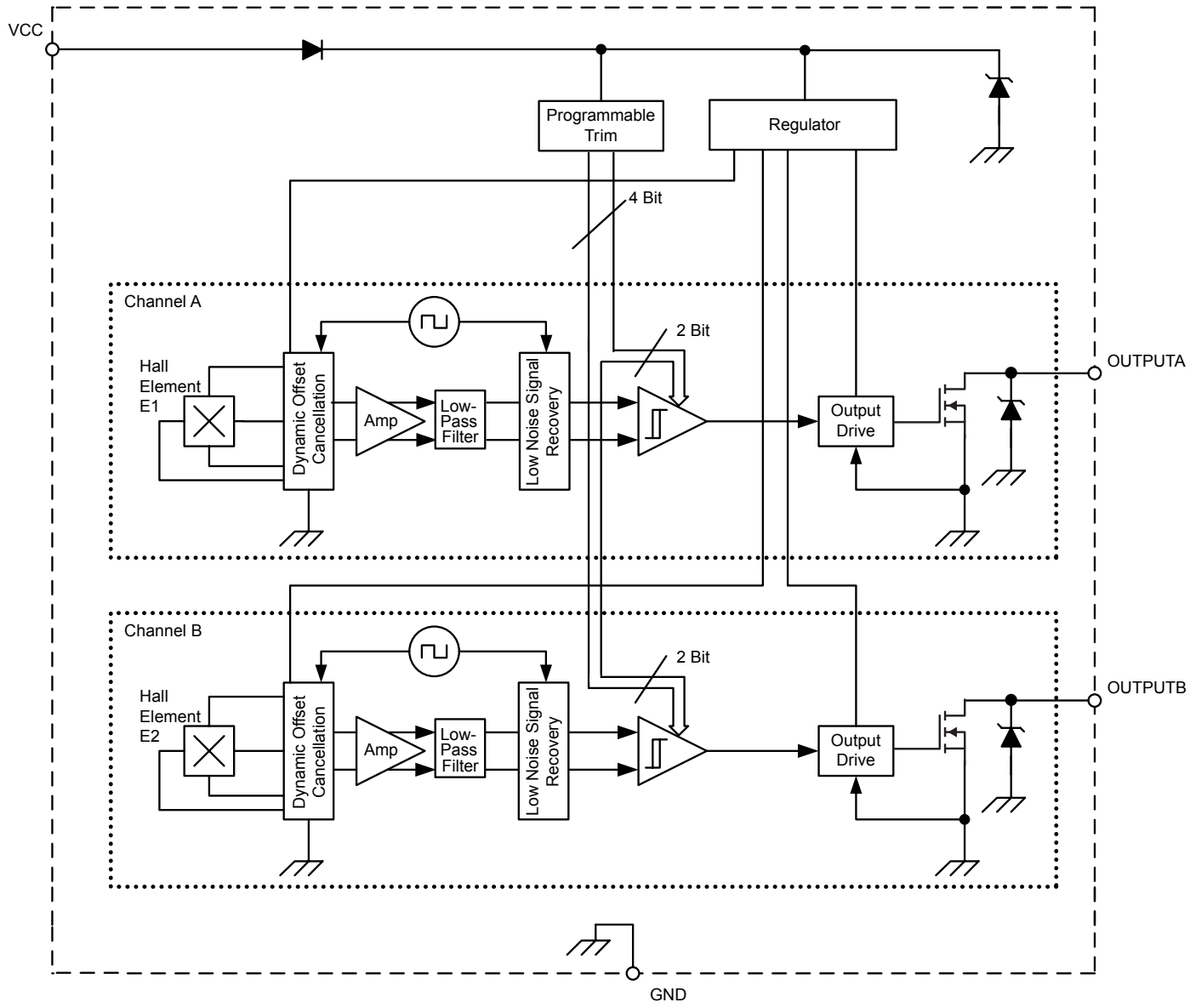
EMC

Contact Allegro MicroSystems for EMC performance.



Functional Block Diagram

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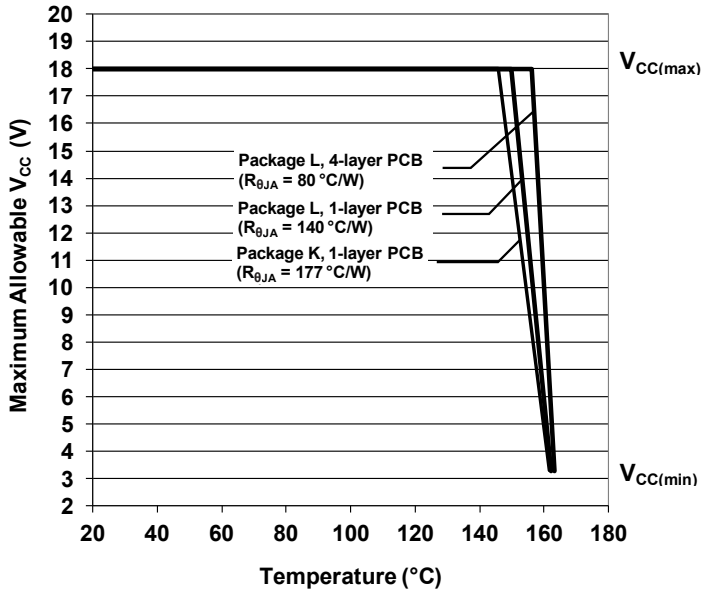
THERMAL CHARACTERISTICS: may require derating at maximum conditions; see application information

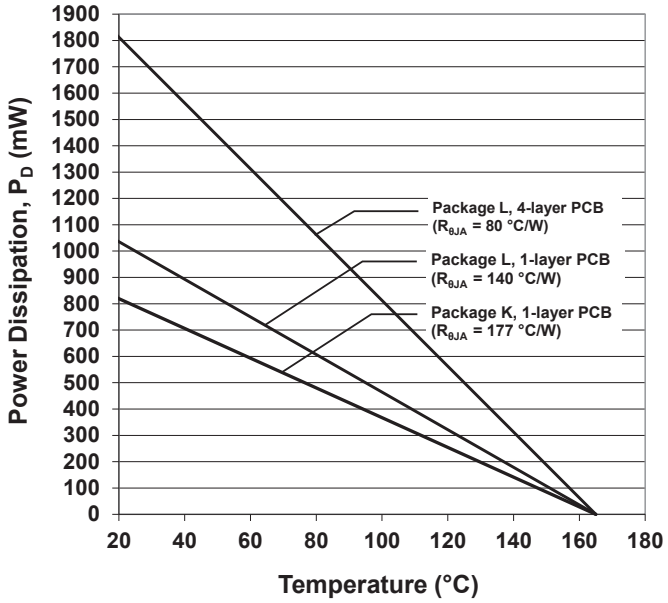
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package K, 1-layer PCB with copper limited to solder pads	177	ºC/W
		Package L-8 pin, 1-layer PCB with copper limited to solder pads	140	ºC/W
		Package L-8 pin, 4-layer PCB based on JEDEC standard	80	ºC/W

*Additional thermal data available on the Allegro website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



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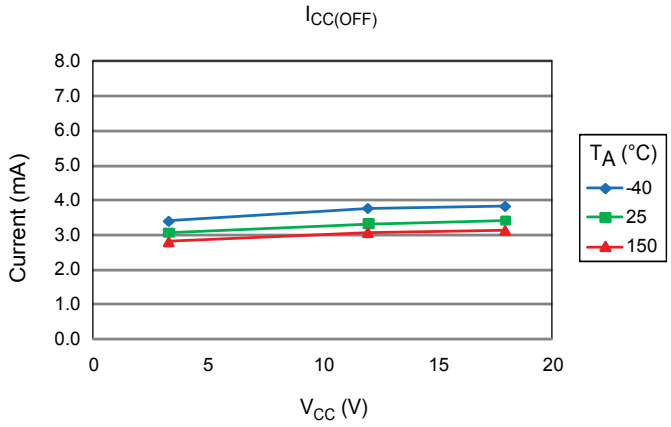
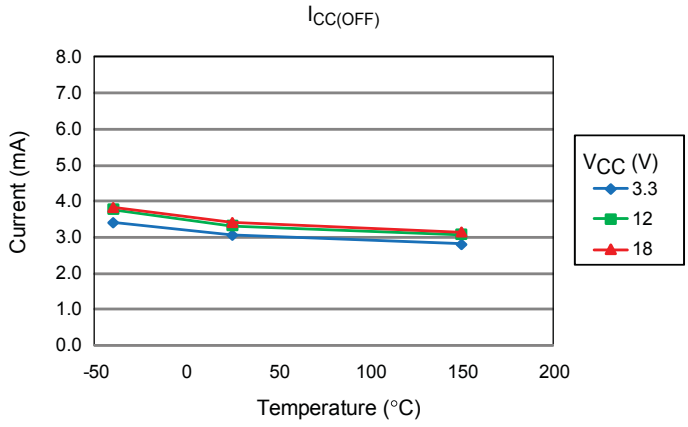
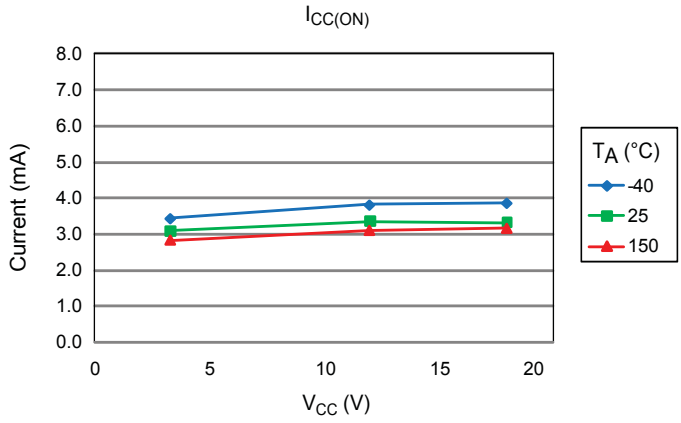
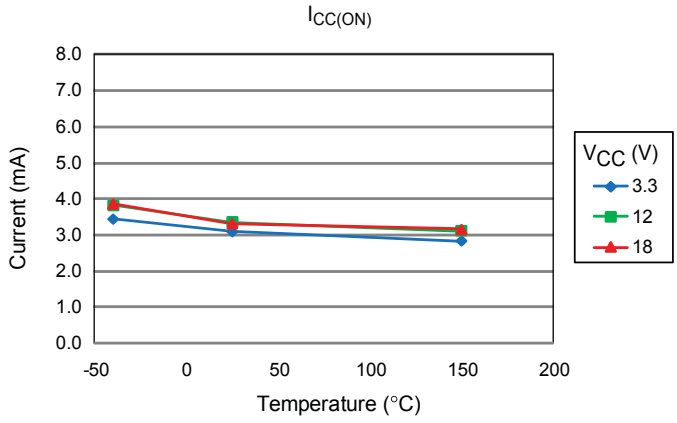
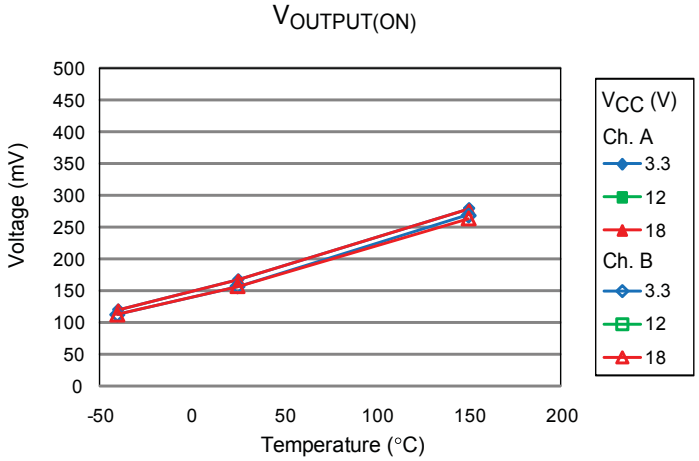
Electrical Operating Characteristics











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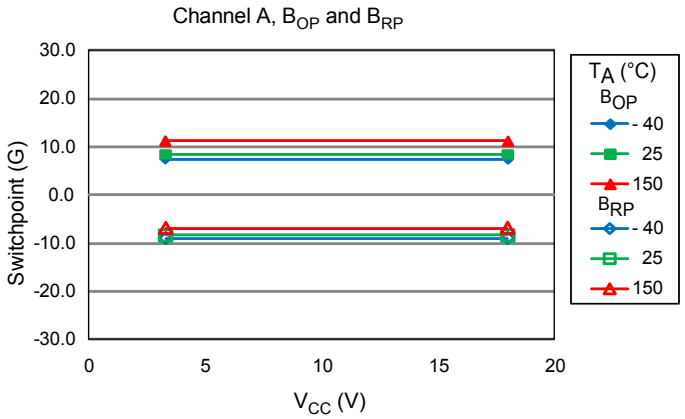
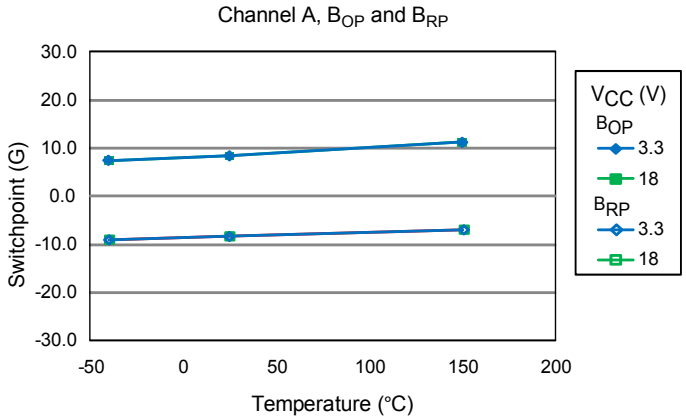
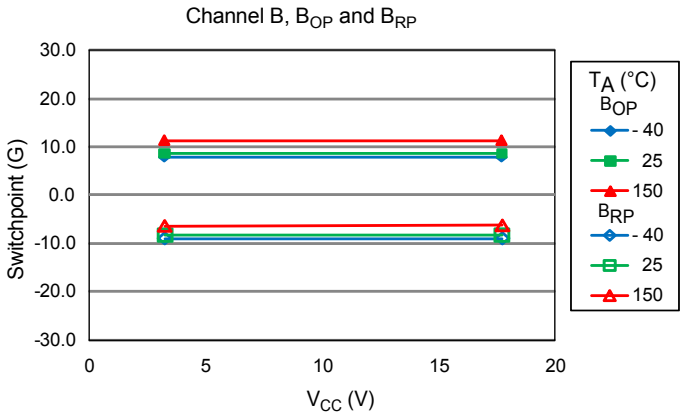
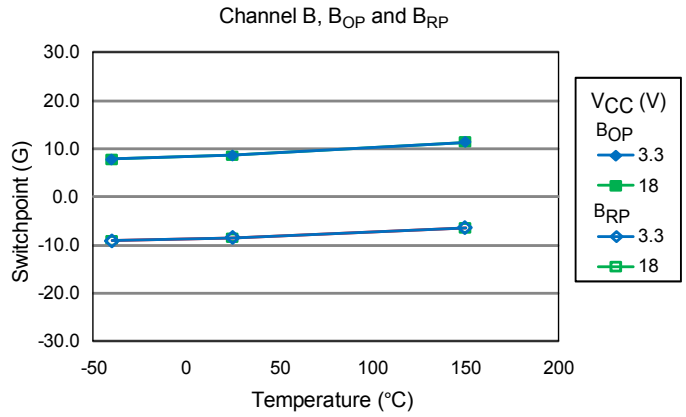
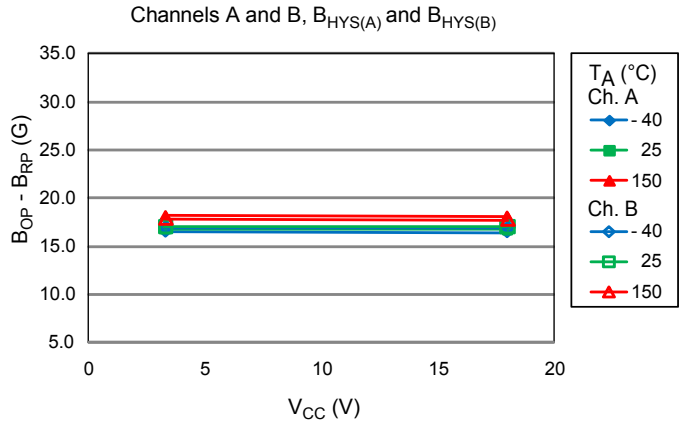
Magnetic Operating Characteristics

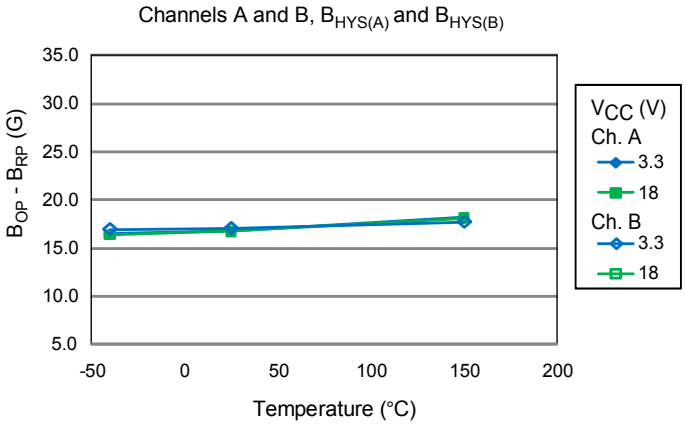












Additional magnetic characteristics on next page

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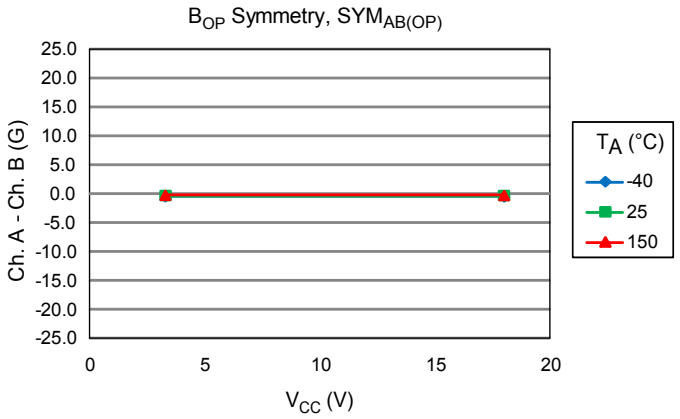

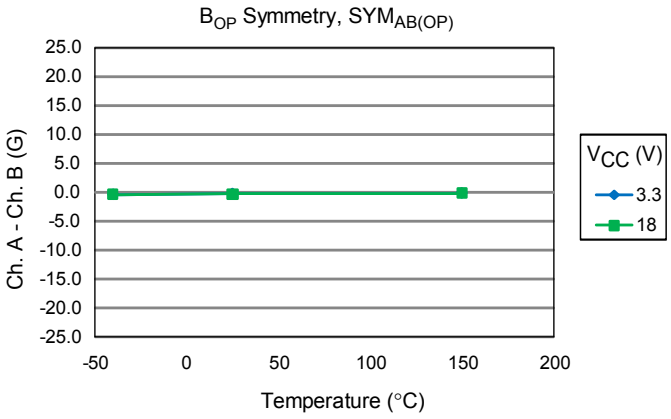

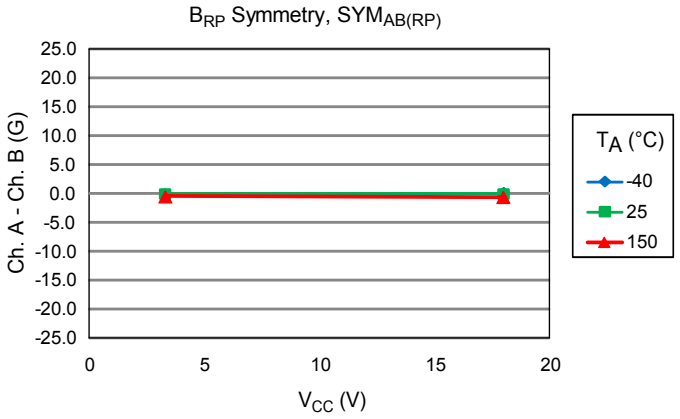

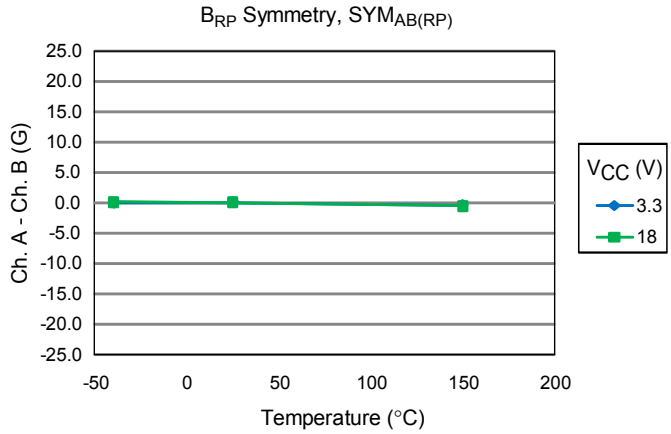

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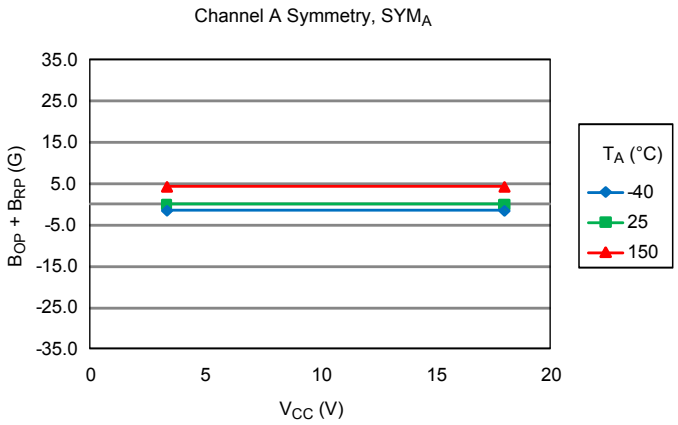

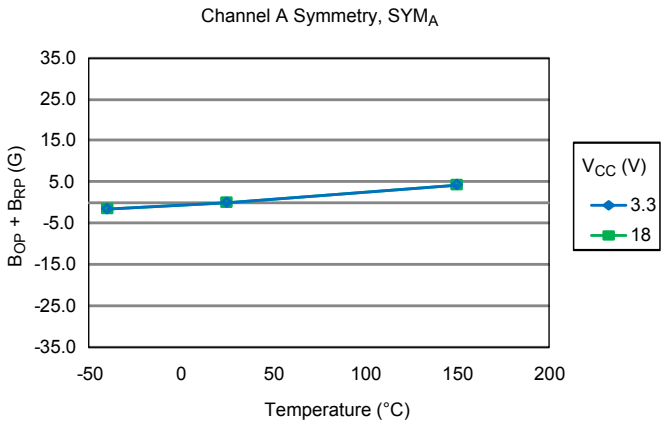

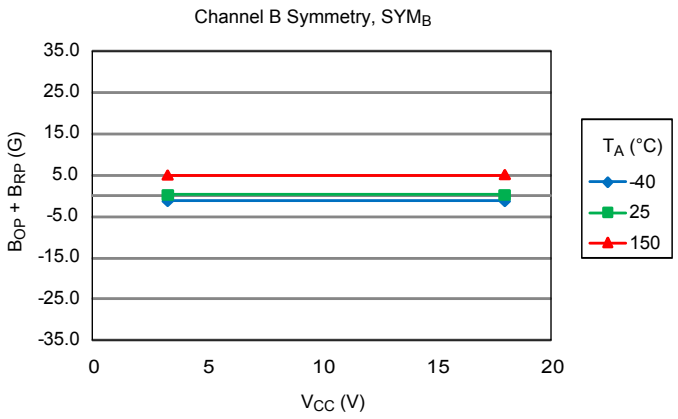

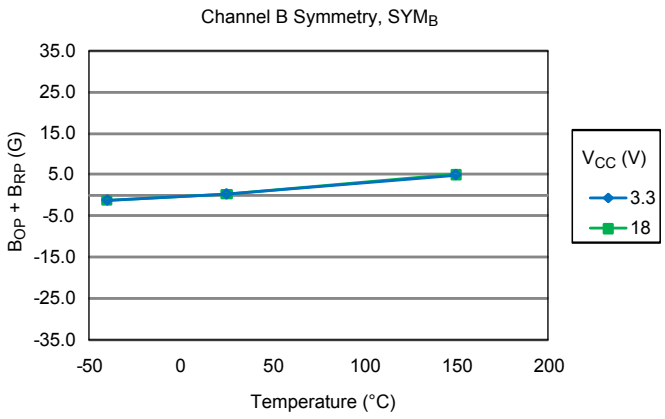

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FUNCTIONAL DESCRIPTION

Chopper-Stabilized Technique

A limiting factor for switch point accuracy when using Hall effect technology is the small signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall IC. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range.

Chopper-stabilization is a unique approach used to minimize Hall offset on the chip. The Allegro technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high frequency signal. Then, using a low-pass filter the signal passes while the modulated DC offset is suppressed.

Allegro's new innovative chopper-stabilization technique uses a high frequency clock. This chopper-stabilization approach desensitizes the IC to temperature and stress. The high-frequency operation also allows a greater sampling rate that produces higher accuracy and faster signal processing capability. Additionally, filtering is more effective and results in a lower noise analog signal at the input to the Schmitt trigger. Therefore, this high-frequency chopping technique reduces jitter, also known as 360° repeatability, can be induced on the output signal. The sample-and-hold process, used by the demodulator to store and recover the signal, can slightly degrade the signal to noise ratio. This is because the process generates replicas of the noise spectrum at the baseband, causing a decrease in jitter performance. However, the improvement in switch point performance, resulting from the reduction of the effects of thermal and mechanical stress, outweighs the degradation in the signal to noise ratio.

This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic integration and sample and hold circuits.

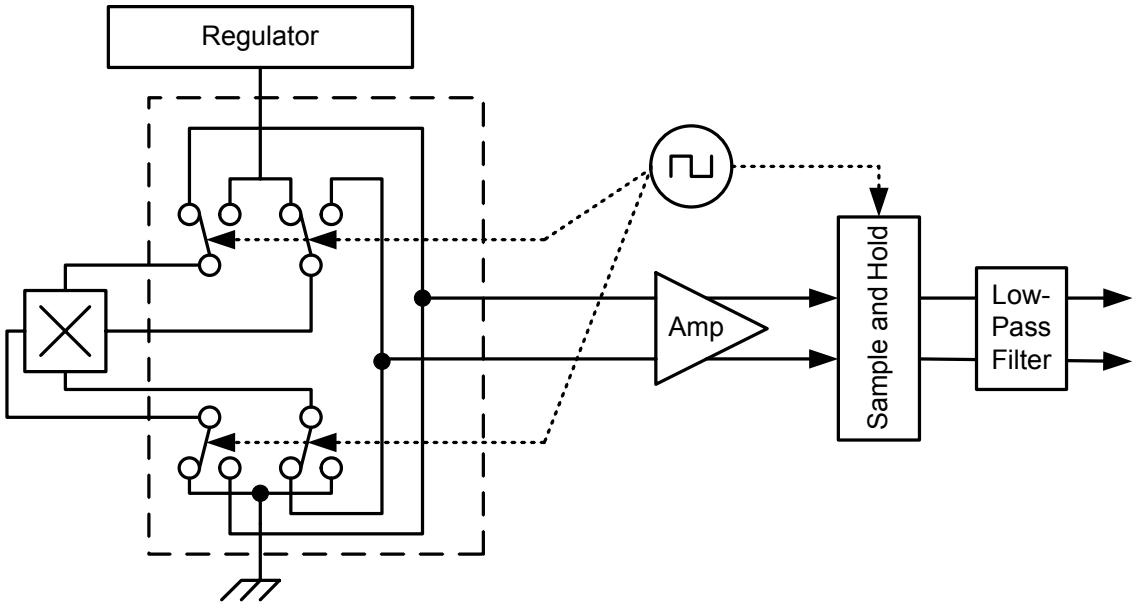

Figure 1: Chopper Stabilization Circuit (Dynamic Quadrature Offset Cancellation)

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TYPICAL APPLICATIONS OPERATION

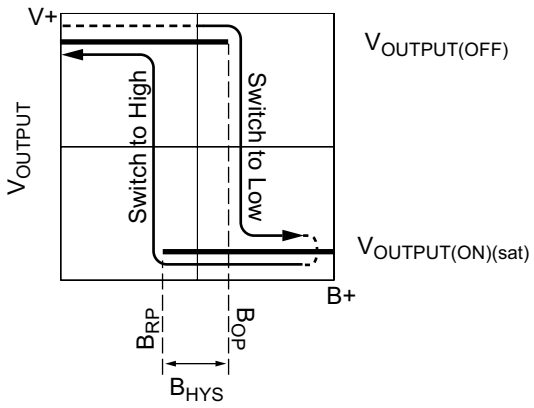

Figure 2: Output Voltage in Relation to Magnetic Flux Density Received.
Output on each channel independently follows the same pattern of transition through B_{OP} followed by transition through B_{RP}.

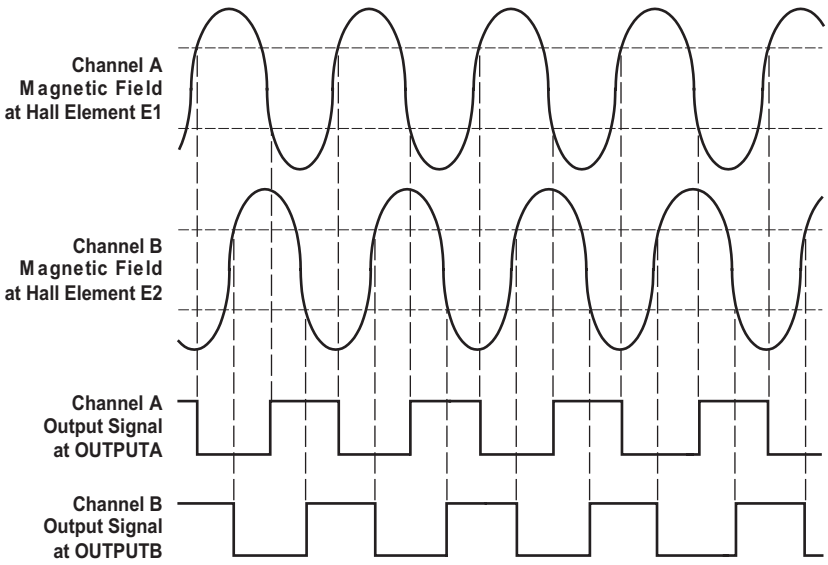

Figure 3:Quadrature Output Signal Configuration.
The outputs of the two output channels have a phase difference of 90º when used with a properly designed magnet that has an optimal pole pitch of twice the Hall element spacing of 1 mm.

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TYPICAL APPLICATIONS CIRCUITS

This device requires minimal protection circuitry during operation with a low-voltage regulated line. The on-chip voltage regulator provides immunity to power supply variations between 3.3 and 18 V. Because the device has open-drain outputs, pull-up resistors must be included.

If protection against coupled and injected noise is required, then a simple low-pass filter on the supply (RC) and a filtering capacitor on each of the outputs may also be needed, as shown in the unregulated supply diagram.

For applications in which the device receives its power from unregulated sources, such as a car battery, full protection is generally required to protect the device against supply-side transients. Specifications for such transients vary for each application, so the design of the protection circuit should be optimized for each application.

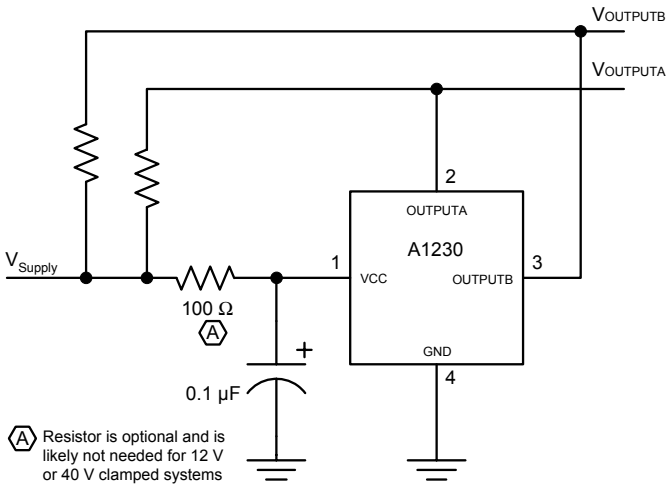

Figure 4: Regulated Supply

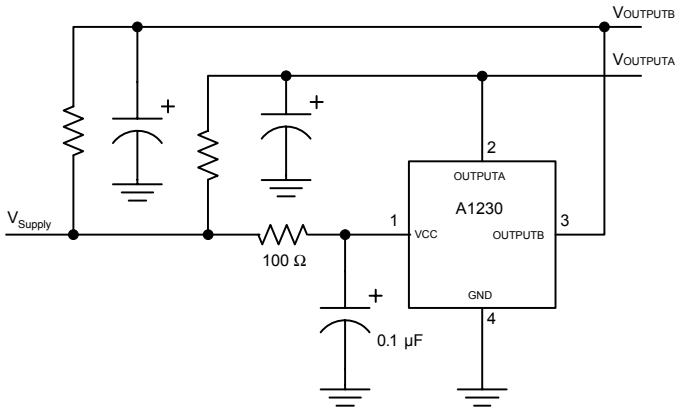

Figure 5: Unregulated Supply

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_J(max)$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4 mA, and $R_{\theta JA}$ = 140 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140\ °C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level, without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package L, using a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=140°C/W, $T_J(max)$ =165°C, $V_{CC}(max)$ = 18 V, and $I_{CC}(max)$ = 6 mA.

Calculate the maximum allowable power level, $P_D(max)$. First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 140°C/W = 107\,mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC}(est) = P_D(max) \div I_{CC}(max) = 107\,mW \div 6\,mA = 18\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC}(est)$.

Compare $V_{CC}(est)$ to $V_{CC}(max)$. If $V_{CC}(est) \leq V_{CC}(max)$, then reliable operation between $V_{CC}(est)$ and $V_{CC}(max)$ requires enhanced $R_{\theta JA}$. If $V_{CC}(est) \geq V_{CC}(max)$, then operation between $V_{CC}(est)$ and $V_{CC}(max)$ is reliable under these conditions.

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PACKAGE OUTLINE DRAWING

For Reference Only - Not for Tooling Use

(Reference DWG-9010)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

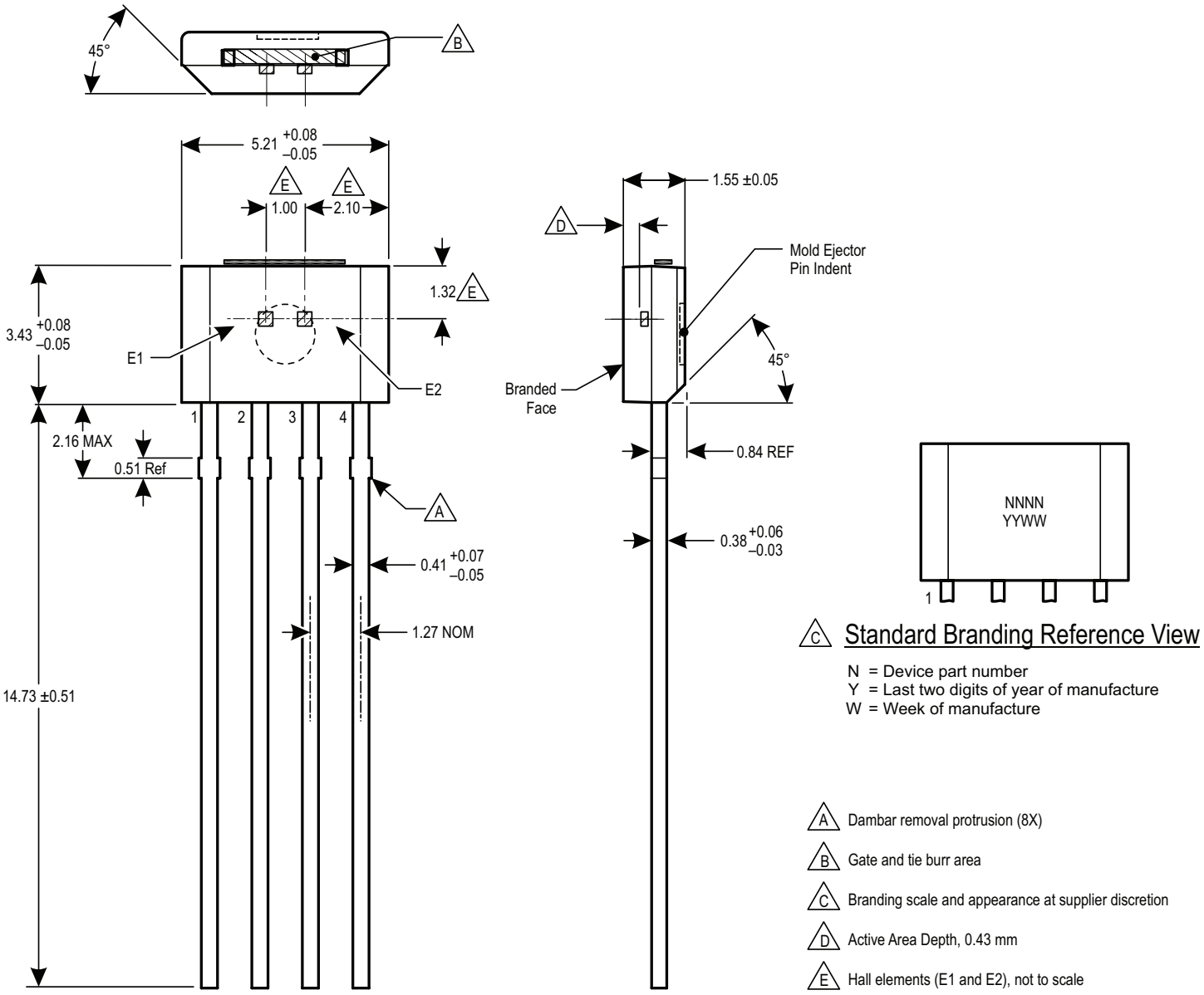

Figure 6: Package K, 4-Pin SIP

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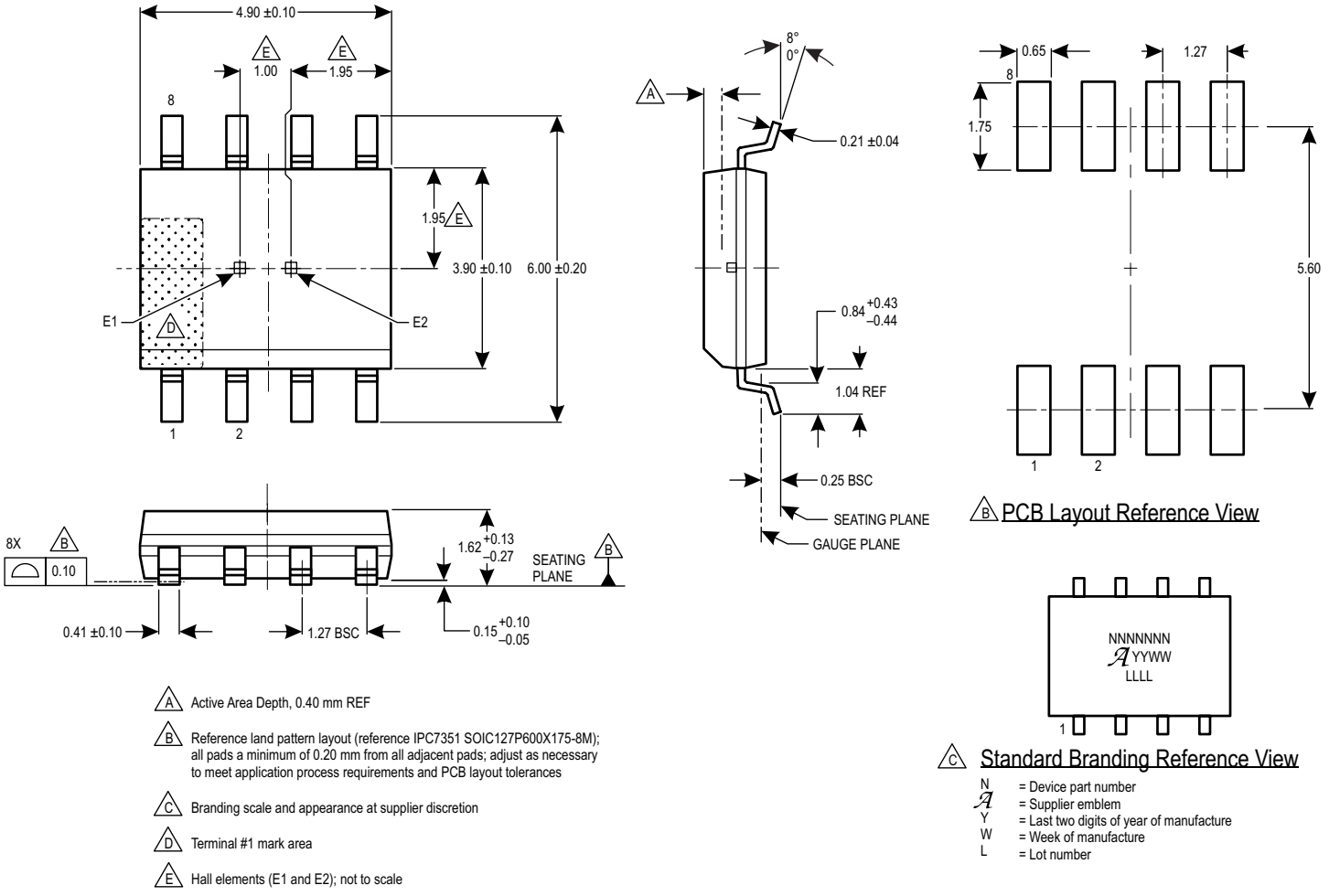
(Reference DWG-9204)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 0.40 mm REF

B Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Terminal #1 mark area

E Hall elements (E1 and E2); not to scale

Figure 7: Package L, 8-Pin SOICN

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Revision History

Number	Date	Description
2	May 6, 2013	Correct packing typographical error
3	June 9, 2014	Correct packing typographical error and reformatted datasheet
4	June 26, 2014	Correct chart labels, table row spacing, and typical application circuits text
5	June 24, 2015	Correct position of Hall elements in upper K package outline drawing
6	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits
7	February 15, 2019	Minor editorial updates
8	February 24, 2020	Minor editorial updates

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