ORDERING INFORMATION

Device	Package	Shipping [†]
74HCT08DR2G	SOIC-14 (Pb-Free)	
74HCT08DR2GH	SOIC-14 (Halide-Free)	2500/Tape & Reel
74HCT08DTR2G	TSSOP-14*	

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V_CC + 0.5	V
l _{in}	DC Input Current, per Pin	±20	mA
l _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	– 65 to + 150	°C
ΤL	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be

tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)			5.5	V
V _{in}	DC Input Voltage (Referenced to GND)	0	5.5	V	
V _{out}	DC Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f) V 5 V 9 V	0 0 0	1000 500 400	ns

				Vcc	Guaranteed Limit			
Symbol	Parameter		(V)	–55 to 25°C	≤85°C	≤125°C	Unit	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1V I _{out} ≤ 20μA		4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage	$\begin{split} V_{out} &= V_{CC} - 0.1V \\ & \left I_{out} \right \leq 20 \mu A \end{split}$		4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IL} I _{out} ≤ 20μA		4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V _{in} = V _{IL}	$ I_{out} \le 4.0 \text{mA}$	4.5	3.98	3.84	3.70	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20μA		4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{in} = V _{IH}	$ I_{out} \le 4.0 \text{mA}$	4.5	0.26	0.33	0.40	
l _{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$		5.5	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0\mu A$		5.5	2.0	20	40	μA
ΔI_{CC}	Additional Quiescent Supply Current	V _{in} = 2.4V, Any On V _{in} = V _{CC} or GND,	•		≥ –55°C	25 to	125°C	
	ouncil	$V_{in} = V_{CC} \text{ of GND},$ $I_{out} = 0\mu A$		5.5	2.9	2	.4	mA

DC CHARACTERISTICS (Voltages Referenced to GND)

1. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

2. Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

AC CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

		V _{CC}	Guaranteed Limit			
Symbol	Parameter	(V)	–55 to 25°C	≤ 85°C	≤125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	4.5	15	19	22	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	4.5	15	19	22	ns
C _{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C _{PD}	Power Dissipation Capacitance (Per Buffer)*	20	pF

* Used to determine the no–load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

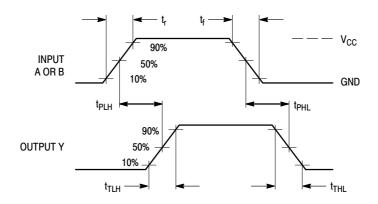
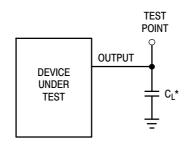


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

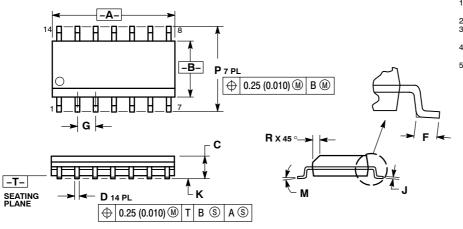
Figure 2. Test Circuit



Figure 3. Expanded Logic Diagram (1/4 of the Device)

PACKAGE DIMENSIONS

SOIC-14 CASE 751A-03 **ISSUE H**

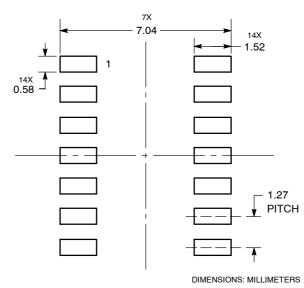


NOTES:

- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE. 5. DIMENSION D. DOCES NOT INCLUDE
- PER SIDE. 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	8.55	8.75	0.337	0.344	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27 BSC		0.050	BSC	
J	0.19	0.25	0.008	0.009	
Κ	0.10	0.25	0.004	0.009	
М	0 °	7 °	0 °	7 °	
Р	5.80	6.20	0.228	0.244	
R	0.25	0.50	0.010	0.019	

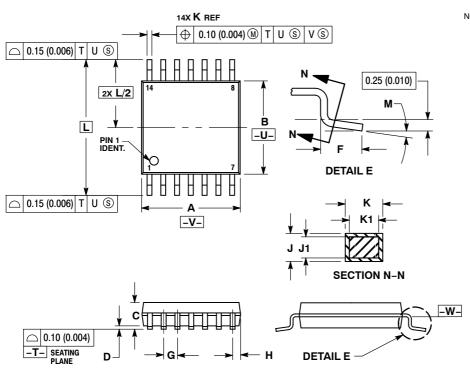
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP-14 CASE 948G-01 **ISSUE B**



NOTES: 1. DIMENSIONING AND TOLERANCING PER

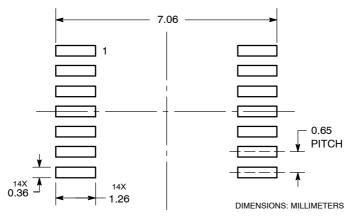
DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION. SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

NOT EXCEED 0.25 (0.010) PER SIDE. 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. 6. TERMINAL NUMBERS ARE SHOWN FOR

REFERENCE ONLY.
DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
К	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40		0.252	BSC
М	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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