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REVISION HISTORY

6/07—Rev. A to Rev. B

Updated Format.....	Universal
Deleted 14-Lead Hermetic DIP/CERDIP	Universal
Changes to Table 1	3
Deleted Table 3; Renumbered Sequentially	3
Changes to Table 2, Layout, Table 3, and Table 4	4
Changes to Table 5 and Table 6.....	5
Changes to Figure 17.....	8
Updated Outline Dimensions	9
Changes to Ordering Guide	9

4/02—Rev. 0 to Rev. A

Change OP-09/OP-11 to OP11	Global
Edits to Pin Connections	1
Edits to Figure 1	1
Edits to Absolute Maximum Ratings	2
Edits to Ordering Guide	2
Edits to Spec Tables	2-4
Deletion of Dice Characteristics.....	5
Deletion of Wafer Test Limits Table	5
Deletion of Typical Electrical Characteristics Table	5

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{OS}	$R_S \leq 10\text{ k}\Omega$		0.3	0.5	mV
Input Offset Current	I_{OS}			5.5	20	nA
Input Bias Current	I_B			180	300	nA
Input Resistance Differential Mode ¹	R_{IN}		0.17	0.29		M Ω
Input Voltage Range	IVR		± 12	± 13		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12\text{ V}$, $R_S \leq 10\text{ k}\Omega$	100	120		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{ V}$ to $\pm 15\text{ V}$, $R_S \leq 10\text{ k}\Omega$		4	32	$\mu\text{V/V}$
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$	± 11	± 13		V
Large Signal Voltage Gain	A_{VO}	$R_L \leq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	100	650		V/mV
Power Consumption ²	P_d	$V_O = 0\text{ V}$		105	180	mW
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.7		$\mu\text{V p-p}$
Input Noise Voltage Density	e_n	$f_0 = 10\text{ Hz}$		18		nV/ $\sqrt{\text{Hz}}$
		$f_0 = 100\text{ Hz}$		14		nV/ $\sqrt{\text{Hz}}$
		$f_0 = 1\text{ kHz}$		12		nV/ $\sqrt{\text{Hz}}$
Input Noise Current	i_n p-p	0.1 Hz to 10 Hz		17		pA p-p
Input Noise Current Density	i_n	$f_0 = 10\text{ Hz}$		1.8		pA/ $\sqrt{\text{Hz}}$
		$f_0 = 100\text{ Hz}$		1.5		pA/ $\sqrt{\text{Hz}}$
		$f_0 = 1\text{ kHz}$		1.2		pA/ $\sqrt{\text{Hz}}$
Channel Separation	CS		100	130		dB
Slew Rate ³	SR		0.7	1.0		V/ μs
Large Signal Bandwidth ³		$V_O = 20\text{ V p-p}$	11	16		kHz
Closed-Loop Bandwidth ⁴	BW	$A_{VCL} = 1$	2.4	3.0		MHz
Rise Time ³	t_r	$A_V = 1$, $V_{IN} = 50\text{ mV}$		110	145	ns
Overshoot ³	OS			15	25	%

¹ Guaranteed by input bias current.

² Total dissipation for all four amplifiers in package.

³ Sample tested.

⁴ Guaranteed by rise time.

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$V_S = \pm 15\text{ V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{OS}	$R_S \leq 10\text{ k}\Omega$		0.4	0.8	mV
Average Input Offset Voltage Drift ¹	TCV_{OS}	$R_S \leq 10\text{ k}\Omega$		2.0	10	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}			14	30	nA
Average Input Offset Current Drift ¹	TCI_{OS}			0.1	0.3	$\text{nA}/^\circ\text{C}$
Input Bias Current	I_B			200	350	nA
Input Voltage Range	IVR		± 12	± 13		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12\text{ V}$, $R_S \leq 10\text{ k}\Omega$	100	120		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{ V}$ to $\pm 15\text{ V}$, $R_S \leq 10\text{ k}\Omega$		4	32	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	50	250		V/mV
Output Voltage Swing	V_O	$R_L \geq 2\text{ k}\Omega$	± 11	± 13		V
Power Consumption ²	P_d	$V_O = 0\text{ V}$		115	200	mW

¹ Guaranteed but not tested.

² Total dissipation for all four amplifiers in package.

MATCHING CHARACTERISTICS

$V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $R_S \leq 100\text{ }\Omega$, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage Match	ΔV_{OS}			0.5	0.75	mV
Common-Mode Rejection	ΔCMRR	$V_{CM} = \pm 12\text{ V}$		1	20	$\mu\text{V}/\text{V}$
Ratio Match		$V_{CM} = \pm 12\text{ V}$	94	120		dB

$V_S = \pm 15\text{ V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $R_S \leq 100\text{ }\Omega$, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage Match	ΔV_{OS}			0.6	1.0	mV
Common-Mode Rejection	ΔCMRR	$V_{CM} = \pm 12\text{ V}$		3.2	20	$\mu\text{V}/\text{V}$
Ratio Match		$V_{CM} = \pm 12\text{ V}$	94	110		dB

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage (V_S)	± 22 V
Differential Input Voltage	± 30 V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous (One Amp Only)
Storage Temperature Range	-65°C to $+125^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	0°C to 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Resistance

Package Type	θ_{JA}^1	θ_{JC}	Unit
14-Lead PDIP (N-14)	83	39	$^{\circ}\text{C/W}$

¹ θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for device in socket for PDIP.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

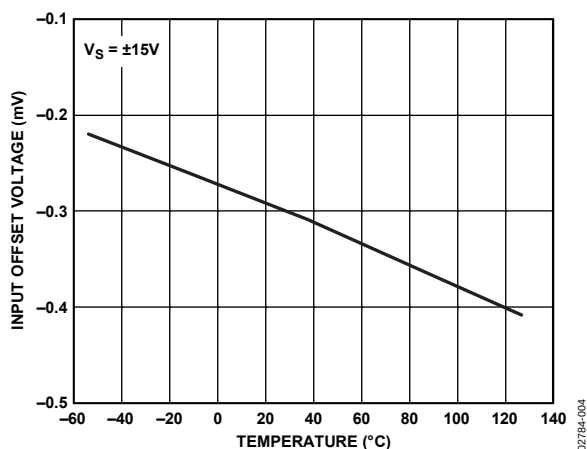


Figure 3. Input Offset Voltage vs. Temperature

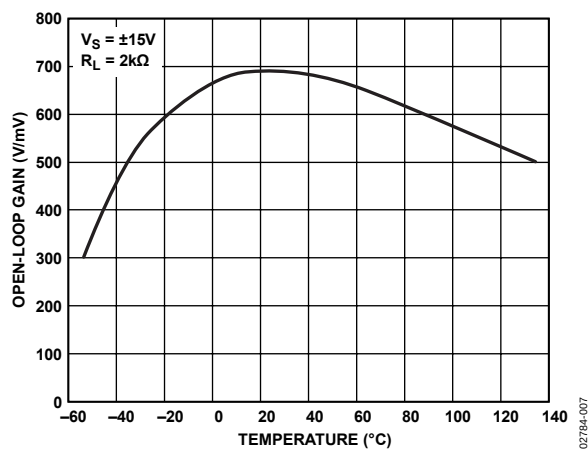


Figure 6. Open-Loop Gain vs. Temperature

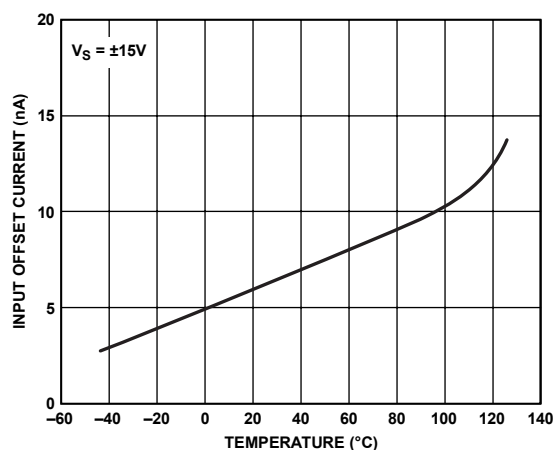


Figure 4. Input Offset Current vs. Temperature

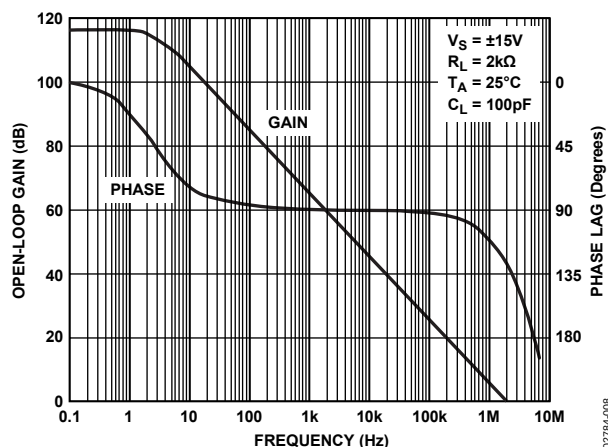


Figure 7. Open-Loop Gain and Phase vs. Frequency

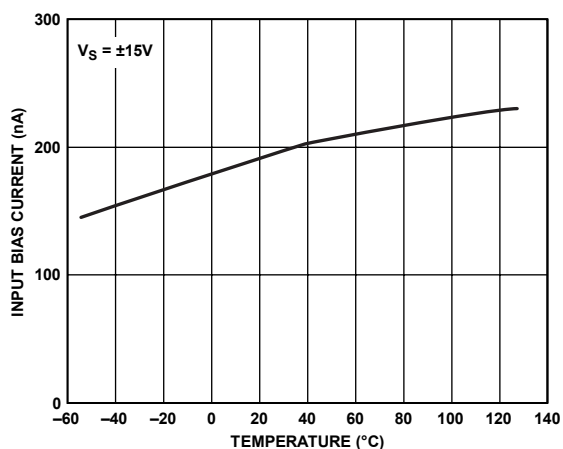


Figure 5. Input Bias Current vs. Temperature

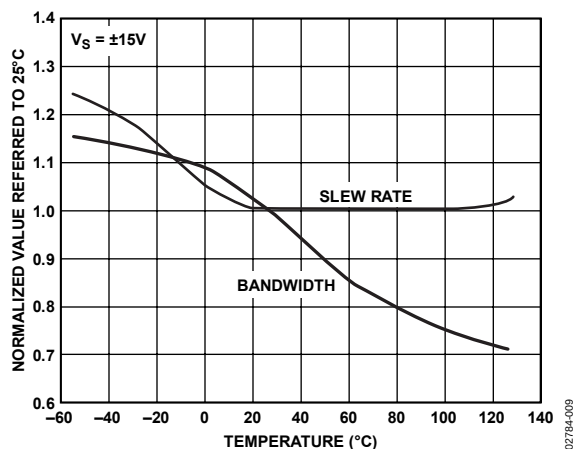


Figure 8. Normalized Slew Rate and Bandwidth vs. Temperature

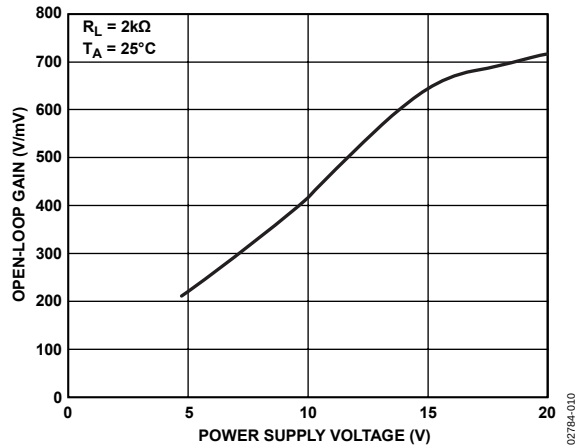


Figure 9. Open-Loop Gain vs. Power Supply Voltage

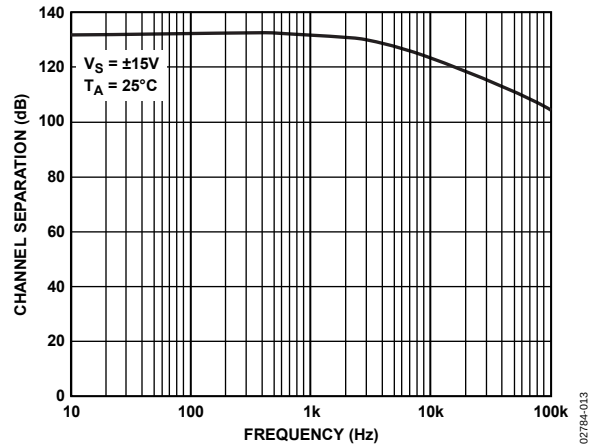


Figure 12. Channel Separation vs. Frequency

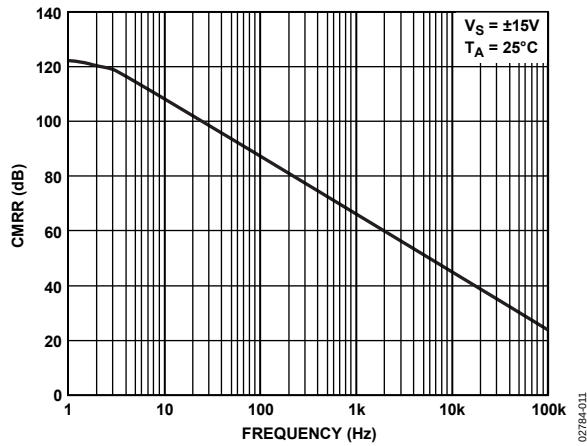


Figure 10. CMRR vs. Frequency

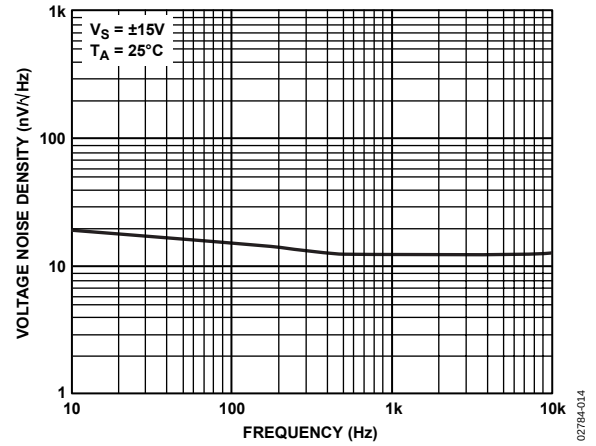


Figure 13. Voltage Noise Density vs. Frequency

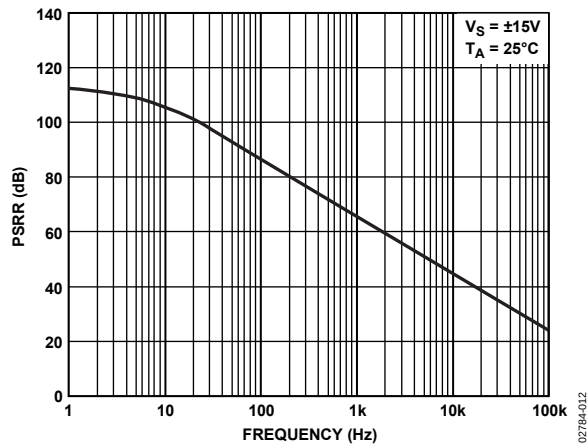


Figure 11. PSRR vs. Frequency

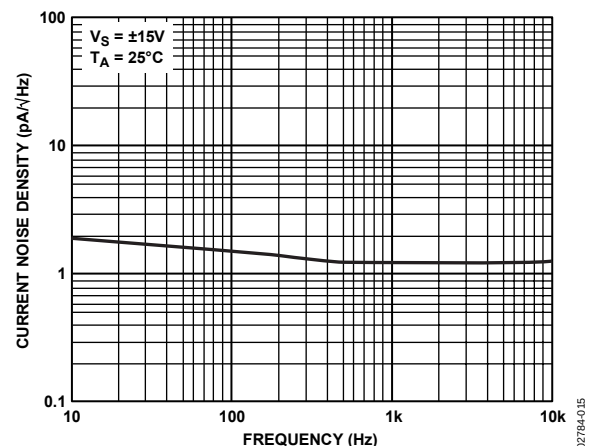


Figure 14. Current Noise Density vs. Frequency

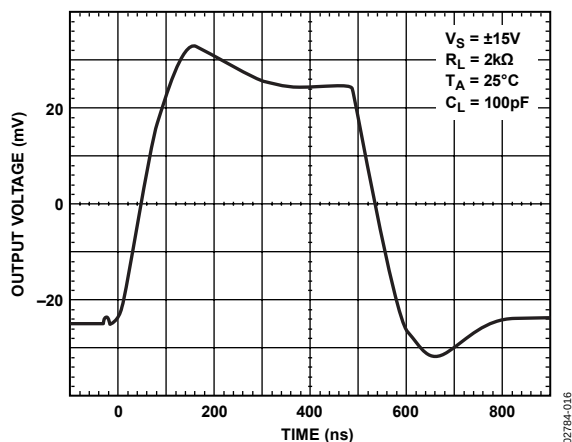


Figure 15. Transient Response

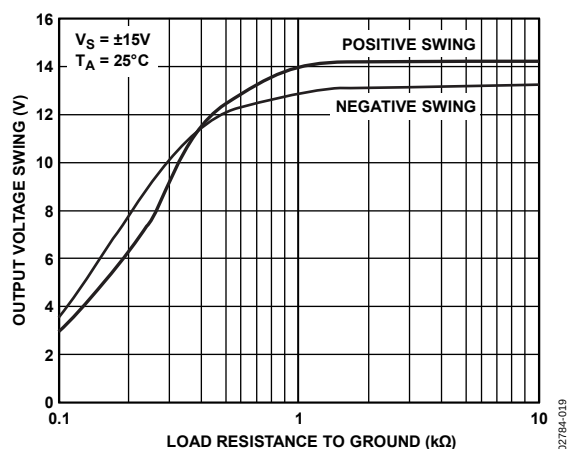


Figure 18. Output Voltage Swing vs. Load Resistance

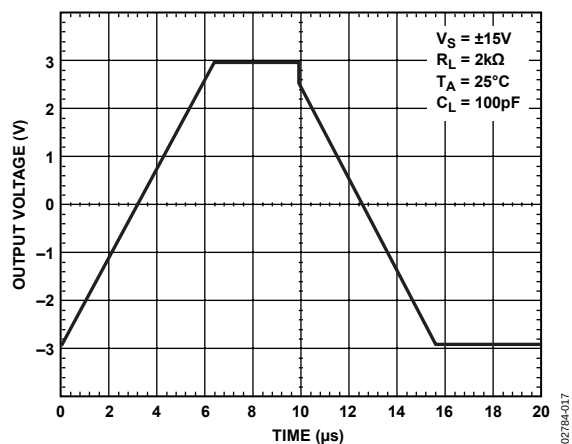


Figure 16. Voltage Follower Pulse Response

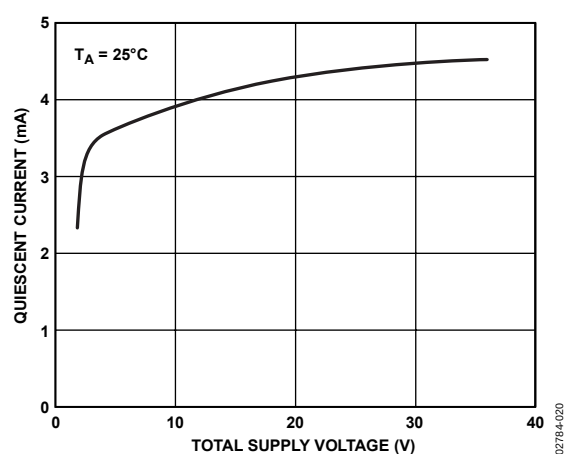


Figure 19. Quiescent Current vs. Total Supply Voltage

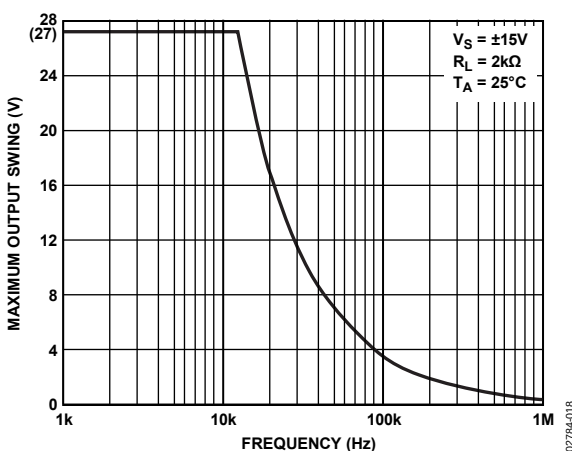


Figure 17. Maximum Output Swing vs. Frequency

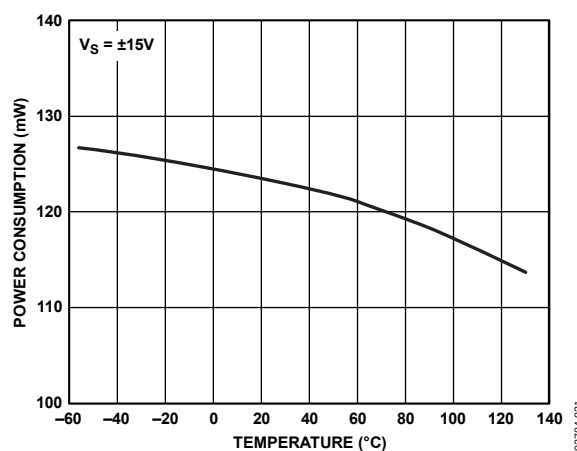
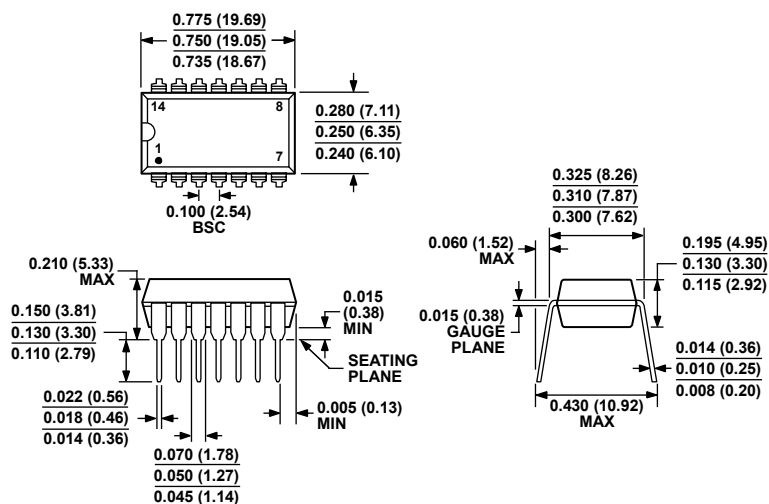


Figure 20. Power Consumption vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 21. 14-Lead Plastic Dual In-Line Package [PDIP]

(N-14)

[P Suffix]

Dimensions shown in inches and (millimeters)

070608-A

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP11EP	0°C to 70°C	14-Lead Plastic Dual In-Line Package (PDIP)	N-14 (P-Suffix)
OP11EPZ ¹	0°C to 70°C	14-Lead Plastic Dual In-Line Package (PDIP)	N-14 (P-Suffix)

¹ Z = RoHS Compliant Part.

For military processed devices, refer to the Standard Microcircuit Drawing (SMD) available at
<http://www.dscclia.mil/downloads/Milspec/Smd/89801.pdf>.

SMD Part Number	Analog Devices, Inc. Equivalent
5962-89801012A	OP11ARCMDA
5962-8980101CA	OP11AYMDA

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