Product names mentioned herein may be trademarks of their respective companies.

Table of Contents

1. Introduction

1.1 Application and References

TMPR46x is a family of Toshiba's ARM based 32-bit RISC microcontrollers, and ASSP (Application Specific Standard Product) suitable for automotive applications. It is designed for a wide range of applications as described below.

- Driver Information Systems,
- Car Infotainment Systems, or
- Car Navigation Systems.

TMPR46x has a built-in ARM Cortex-R4 core which is real-time processor based on the ARMv7-R architecture. The Cortex-R4 processor performs substantially higher performance, real-time responsiveness, reliability and dependability with high error resistance, and offers more features than other similar class processors.

Please refer to the ARM documentation for detailed information about the processor core, including the instruction set.

In addition, TMPR46x ASSP includes peripheral circuits such as Toshiba Security Module (TSM), five stepper motor controllers, two graphics display controllers (GDC), a 2D graphics accelerator (GA), a frame grabber (FG), DMA controller, several serial communication interfaces, CAN bus interfaces, MediaLB® interface, different types of timers, ADC, and many general purpose I/Os.

1.2 Feature Overview

A system-level block diagram can be found in Figure 1-1.

1.2.1 Base-System

- ARM Cortex-R4 CPU with up to 300 MHz nominal operation frequency
  - Little-Endian
  - 32Kbyte Data Cache, 32KByte Instruction Cache, with Error Correction (ECC)
  - 2 x 32KByte Tightly Coupled Memory (TCM), with Error Correction (ECC)
  - Memory Protection Unit (MPU) with 12 MPU Regions
- Internal high performance bus system based on ARM's AMBA-compliant NIC-301 Network Interconnect
- 8 channels 32-bit System Timing Protection Unit (STPU), lockable task protection timers of AutoSAR 4.x SC1.4 class.
- DMA-Controller with 8 channels
- Interrupt Controller with ARM Cortex-R4 compliant VIC port, programmable level or edge sensitivity, and programmable priority levels
- 768KByte embedded SRAM, with Error Correction (ECC). In the case with ECC, parts of the internal memory are used for parity data memory, which is not accessible from the CPU.
- TSM (TOSHIBA Security Module): Hardware Security Module
  - TMPR462/3 only: compliant to "SHE" Specification
  - TMPR460/1 only: with reduced functionality

  TSM support "Secure Boot", AES128 (ECB & CBC) encryption and decryption, and Random number generation.

1.2.2 Memory Connectivity

- 32-bit SDRAM interface
  - For one 32-bit SDRAM device or two 16-bit devices
  - Up to 150MHz interface clock frequency (plus spread spectrum modulation)
- Configurable 32-bit or 16-bit LP-DDR DRAM interface
  - For one 32-bit LP-DDR DRAM device or one 16-bit LP-DDR DRAM device
  - Up to 150MHz interface clock frequency (plus spread spectrum modulation)
- TMPR462 only: internal Quad-SPI Flash (Total 4MByte, 512Kbyte reserved for TSM)
- TMPR463 only: internal Quad-SPI Flash (Total 8MByte, 512Kbyte reserved for TSM)
- 2 channels external Quad-SPI Flash interface
  - Memory mapped directly addressable
  - Main channel with boot support (through IPL, only TMPR460/1)
- 1 channel parallel NOR Flash interface, with boot support (through IPL, only TMPR460/1)
- 1 channel parallel NAND Flash interface, with boot support (through IPL, only TMPR460/1)

1.2.3 Graphics

- 2 independent Graphics Display Controllers (GDC)
  - Based on Graphics Display Controller module in TX4966XBG-280
  - With various enhancements functions, e.g. output dithering unit using Toshiba proprietary method (Magic Square)
- Frame Grabber (Video Input), based on module in TX4966XBG-280
- 2D Graphics Accelerator (GA) Engines
  - Blitting Engine (BE), based on module in TX4966XBG-280
  - Rotation Engine (RE), based on module in TX4966XBG-280, with additional support of perspective projection
  - Transformation Engine (TE), based on module in TX4966XBG-280
  - Drawing Engine (DE) based on module in TX4961XBG-240, with enhanced End-of-Line treatment
- PNG Decoder (PNGDe)
  - Supporting PNG Specification (Second Edition): W3C Recommendation 10 November 2003 (ISO/iEC 15948:2003)
  - for concurrently processing up to 8 independent streams

1.2.4 Peripherals

Communication

- 3 channels Car Area Network (CAN) controller, 32 mailboxes per channel
- 2 channels Extended Serial Expansion Interface (ESEI), compatible with Serial Peripheral Interface (SPI)
- 2 channels Asynchronous Serial Interface (HS-UART)
- 1 channel Serial Bus Interface (SBI) in I²C Bus Mode
- 2 channels Inter-IC Sound (I²S) Bus Interface supporting master and slave Modes
- 1 channel Media Local Bus (MediaLB) Interface, three-pin interface, 6 internal channels

Timer

- Real Time Clock (RTC)
  - Using separate 32kHz crystal oscillator, 10MHz crystal oscillator, or internal 100kHz RC-oscillator
  - Second, minute, hour, day, week, month, and leap year clock/calendar
  - Configurable periodical wake-up alarm
  - Automatic calibration feature (using 10MHz crystal oscillator)
- Watchdog Timer (WDT), running on internal 100kHz RC-oscillator clock
- 24 channels 16-bit PWM Timer
- 4 channels 16-bit High-Speed PWM Timer
- 2 channels 16-bit GDC PWM Timer (GDCPWM for 2 x GDC output), compatible to TX4966XBG-280

- 10 channels 16-bit Complex Timer (6 channels spread spectrum modulated clock and 4 channels non-modulated clock)
- 5 channels Stepper Motor Controller with zero-point and stall detection
    - I/O interface can be operated with 5V or 3.3V

1.2.5 Analog

- PLL for system and peripheral clocks with integrated spread spectrum modulation for low EMI
- Separate PLL for non-modulated system and peripheral clocks
- 5V I/O buffers for Stepper-Motor connection with programmable input comparator
- 14 channels Analog to Digital Converter (ADC). 3.3V, 10-bit resolution, successive approximation type
- Power On Reset (POR). Low Voltage Detection (LVD) for 1.1V and 3.3V power supplies
- Integrated Voltage Regulator for
    - 1.1V main power supply using external pass transistor
    - 1.1V standby power domain (PDS) including 8KByte backup RAM
- 3.3V alarm comparator for external supply voltage supervision
- Internal 100kHz low power RC-Oscillator (used for WDT and clock/system supervision circuits)
- 3.3V / 1.8V LVTTL I/O's with programmable drivability, selectable pull-up/-down resistors, and selectable Schmitt Trigger characteristic
- One-Time Programmable (OTP) electrical Fuses (eFuses) for security usage (within TSM)

1.3 Package options

TMPR46x is available in package options as described in Table 1-1:

Table 1-1: Package options of TMPR46x

Part Number	Package	Description	SIP Flash Size	SHE-compliant TSM
TMPR460XBG-300	BGA-244	Small Package option with reduced set of peripheral functions and restricted I/O multiplexing options.	-	No
TMPR461XBG-300	BGA-328	Standard Package option with full set of peripheral functions and I/O multiplexing options.	-	No
TMPR462XBG-300			32 Mbit	Yes
TMPR463XBG-300			64 Mbit	Yes

Chapter 3. Package offers more information about packaging like ball layout, pin assignment, or dimensions.

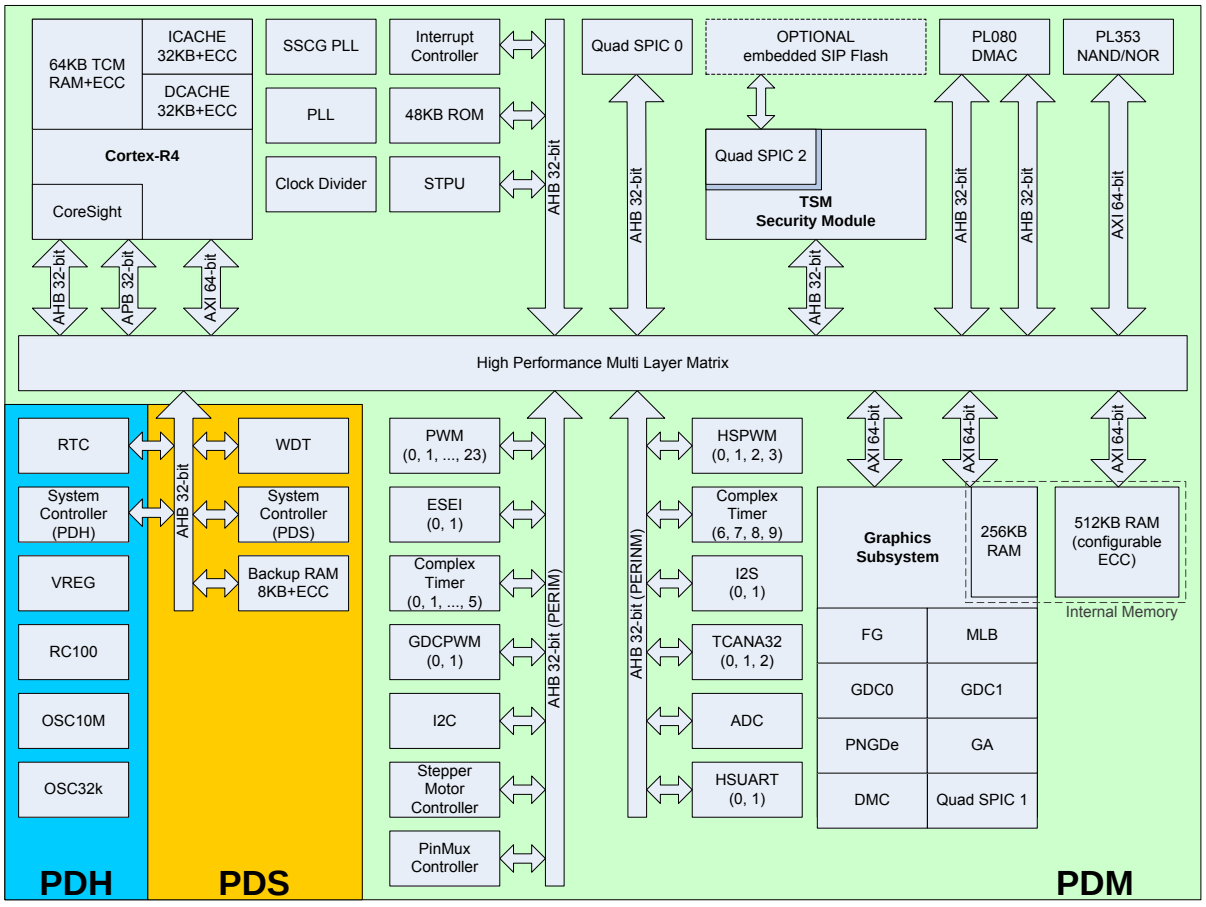

Figure 1-1: System Block Diagram

2. Electrical characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings for all pins

Parameter	Symbol	Min	Typ.	Max	Unit
Core Power Supply (1.1V)	V_{DDC}, PLL_AVD	-0.3	—	1.6	V
I/O & internal 3.3V Power Supply (3.3V)					
VDD33	V_{DD33}	-0.3	—	3.9	V
VDDH_DDRA	V_{DDH_DDRA}	-0.3	—	3.9	V
VDDH_DDRB	V_{DDH_DDRB}	-0.3	—	3.9	V
ADC Power Supply (3.3V)					
ADC33	V_{ADC33}	-0.3	—	3.9	V
Stepper Motor I/O Power Supply (5.0V)					
VDD50	V_{DD50}	-0.3	—	5.55 (note 2)	V
DC Input Voltage	V_{IN}				
3.3V		-0.3	—	V_{DD33} +0.3	V
DDRA I/F (note 1)		-0.3	—	V_{DDH_DDRA}+0.3	V
DDRB I/F (note 1)		-0.3	—	V_{DDH_DDRA}+0.3	V
5V tolerant		-0.3	—	6.7	V
DC Output Voltage (3.3V)	V_{OUT}				
3.3V		-0.3	—	V_{DD33} +0.3	V
DDRA I/F (note 1)		-0.3	—	V_{DDH_DDRA}+0.3	V
DDRB I/F (note 1)		-0.3	—	V_{DDH_DDRA}+0.3	V
DC Input Current on any Input	I_{IN}	—	—	±10	mA
Storage Temperature	T_{STG}	-40	—	+125	°C

(note 1) For details see paragraph 34.2.2 of the Datasheet.

(note 2) This is ONLY allowed under the condition that TMPR46x has been properly powered up into operation mode. Otherwise, VDD50 supply level must NOT exceed 3.9V.

Permanent damage may occur if absolute MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating conditions.

Exposure to higher voltage than recommended for extended periods of time could affect reliability.

2.2 DC Electrical Characteristics

Please see also Package chapter for details about the I/O buffer types, nominal loads, integrated pull-up or -down resistors, Schmitt Trigger functionality, etc.

Table 2-2: DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Core Power Supply (1.1V)	$V_{DDC,}$ PLL_AVD		1.0	1.1	1.2	V
I/O & internal 3.3V Power Supply (3.3V) VDD33	V_{DD33}	 Standard eFuse write	 3.0 3.2	 3.3 3.3	 3.6 3.6	 V V
VDDH_DDRA (note 1)	V_{DDH_DDRA}	SDRAM LP-DDR	3.0 1.7	3.3 1.8	3.6 1.9	V V
VDDH_DDRB (note 1)	V_{DDH_DDRB}	SDRAM LP-DDR	3.0 1.7	3.3 1.8	3.6 1.9	V V
ADC Power Supply (3.3V) ADC33	V_{ADC33}		3.0	3.3	3.6	V
Stepper Motor I/O Power Supply (5.0V) VDD50 (note 2)	V_{DD50}	 3.3V I/F 5.0V I/F	 3.0 4.75	 3.3 5.0	 3.6 5.25	 V V
Operating Current (Normal Mode) VDDC, PLL_AVD	I_{DD11}		—	—	1212.9	mA
VDDH_DDRA/B (note 1 and 3)	I_{DD18}	LP-DDR	—	—	27.6	mA
VDD33 (note 3) VDDH_DDRA/B (note 1 and 3) VADC	I_{DD33}	SDRAM	—	—	168.4 52 0.4	mA mA mA
VDD50	I_{DD50}		—	—	60	mA
Low Level Input Voltage 3.3V 3.3V (Schmitt)	V_{IL}		 — —	 — —	 0.8 0.8	 V V
High Level Input Voltage 3.3V 3.3V (Schmitt) 3.3V (5V tolerant)	V_{IH}		 0.8 x V_{DD33} 0.8 x V_{DD33}	 — — —	 — — 5.5	 V V V
Schmitt-Trigger Hysteresis Range			0.3	—	0.8	V
Low Level Input Current Standard Input Buffer Input Buffer with Pull-up	I_{IL}	$V_{IN} = V_{SS}$	—	—	 10 200	 µA µA
High Level Input Current Standard Input Buffer Input Buffer with Pull-down	I_{IH}	$V_{IN} = V_{DD33}$	—	—	 10 200	 µA µA
Pull-up/pull-down resistance	R_{pull}	@ VDDH/2	20	29	40	kΩ
Low Level Output Voltage	V_{OL}		—	—	0.4	V
High Level Output Voltage	V_{OH}		V_{DD33} – 0.6	—	—	V
Ambient operating temperature	T_a		-40	—	+85 (note 4)	°C

(note 1) For details see paragraph 34.2.2 of the Datasheet.

(note 2) In case of supplying Stepper Motor I/O Supply with 3.3V, only digital (TTL) input buffer functionality is available. Stepper Motor I/O Driver and digital (TTL) output buffer functionality cannot be used.

(note 3) Regarding internal pull-up/pull-down resistors, see paragraph 2.2.1.2 below.

(note 4) For details see paragraph 2.2.1.1 below.

2.2.1 Power Consumption and Power Supply Current Values

Expected typical and worst case power consumption values are as shown in the following tables. Typical values are expected at nominal voltage (V_{DDC} = 1.1V, V_{DD33}/ V_{DDH_DDRA}/V_{DDH_DDRB}/V_{ADC33} = 3.3V, V_{DD50} = 5.0V) and ambient temperature T_a = 25°C. Maximum values can be reached at maximum voltage (V_{DDC} = 1.2V, V_{DD33}/V_{DDH_DDRA}/V_{DDH_DDRB}/V_{ADC33} = 3.6V, V_{DD50} = 5.25V) and ambient temperature T_a = 85°C.

Power consumption values always include (optional) RTC running on OSC32k.

Power consumption in M_PLL mode was estimated with the following use-case:

- CR4 calculating dhrystone algorithm with I$ and D$ enabled,
- PNGDe decoding 8 streams in parallel in loop mode,
- GDC0 and GDC1 displaying 640x480 @ 60Hz and layer A, B, C, D, E are 256x256 pixel,
- all PNLGPP outputting dotclock,
- GA continuously drawing random lines,
- ADC performing conversion in scan mode on all channels,
- SMC running in PWM mode,
- all timer (PWM, HSPWM, CT) running at maximum frequency,
- LPDDR handling all instruction and data read and writes,
- IOs configured to toggle at high rate (e.g. outputting Timer),
- all internal clocks enabled.

STOP Mode

Parameter	Symbol	Condition	Total Typ.	Total Max	Unit
Core Power Supply (1.1V)	VDDC, PLL_AVD		-	-	µA
I/O & internal 3.3V Power Supply (3.3V)	VDD33	TMPR460/1	26.8	151.0	µA
		TMPR462/3	31.8	191.0	µA
LPDDR Power Supply (1.8V)	VDDH_DDRA, VDDH_DDRB		3.2	26.6	µA
ADC Power Supply (3.3V)	VADC33		0.1	7.7	µA
Stepper Motor I/O Power Supply (5.0V)	VDD50		31.8	86.4	µA

STOP_R Mode

Parameter	Symbol	Condition	Total Typ.	Total Max	Unit
Core Power Supply (1.1V)	VDDC, PLL_AVD		-	-	µA
I/O & internal 3.3V Power Supply (3.3V)	VDD33	TMPR460/1	90.3	2253.1	µA
		TMPR462/3	95.3	2293.1	µA
LPDDR Power Supply (1.8V)	VDDH_DDRA, VDDH_DDRB		3.2	26.6	µA
ADC Power Supply (3.3V)	VADC33		0.1	7.7	µA
Stepper Motor I/O Power Supply (5.0V)	VDD50		31.8	86.4	µA

SLP_RC100k Mode

Parameter	Symbol	Condition	Total		Unit
			Typ.	Max	
Core Power Supply (1.1V)	VDDC, PLL_AVD		-	-	μA
I/O & internal 3.3V Power Supply (3.3V)	VDD33	TMPR460/1	97.5	2296.6	μA
		TMPR462/3	102.5	2336.6	μA
LPDDR Power Supply (1.8V)	VDDH_DDRA, VDDH_DDRB		3.2	26.6	μA
ADC Power Supply (3.3V)	VADC33		0.1	7.7	μA
Stepper Motor I/O Power Supply (5.0V)	VDD50		31.8	86.4	μA

SLP_OSC10 Mode

Parameter	Symbol	Condition	Total		Unit
			Typ.	Max	
Core Power Supply (1.1V)	VDDC, PLL_AVD		-	-	μA
I/O & internal 3.3V Power Supply (3.3V)	VDD33	TMPR460/1	2.8	5.8	mA
		TMPR462/3	2.8	5.9	mA
LPDDR Power Supply (1.8V)	VDDH_DDRA, VDDH_DDRB		3.2	26.6	μA
ADC Power Supply (3.3V)	VADC33		0.1	7.7	μA
Stepper Motor I/O Power Supply (5.0V)	VDD50		31.8	86.4	μA

STB_OSC10 Mode

Parameter	Symbol	Condition	Total		Unit
			Typ.	Max	
Core Power Supply (1.1V)	VDDC, PLL_AVD		4.4	480.9	mA
I/O & internal 3.3V Power Supply (3.3V)	VDD33	TMPR460/1	2.6	3.0	mA
		TMPR462/3	2.6	3.0	mA
LPDDR Power Supply (1.8V)	VDDH_DDRA, VDDH_DDRB		3.2	26.6	μA
ADC Power Supply (3.3V)	VADC33		0.1	7.7	μA
Stepper Motor I/O Power Supply (5.0V)	VDD50		31.8	86.4	μA

M_PLL Mode

Parameter	Symbol	Condition	Total		Unit
			Typ.	Max	
Core Power Supply (1.1V)	VDDC, PLL_AVD	TMPR460	120.9	1132.8	mA
		TMPR461/2/3	178.6	1212.9	mA
I/O & internal 3.3V Power Supply (3.3V)	VDD33	TMPR460	96.0	106.7	mA
		TMPR461	120.0	133.3	mA
		TMPR462/3	145.1	168.4	mA
LPDDR Power Supply (1.8V)	VDDH_DDRA, VDDH_DDRB		24.6	27.6	mA
ADC Power Supply (3.3V)	VADC33		0.2	0.4	mA
Stepper Motor I/O Power Supply (5.0V)	VDD50	TMPR460	45.8	48.1	mA
		TMPR461/2/3	57.2	60.1	mA

2.2.1.1 Maximum Ambient Temperature

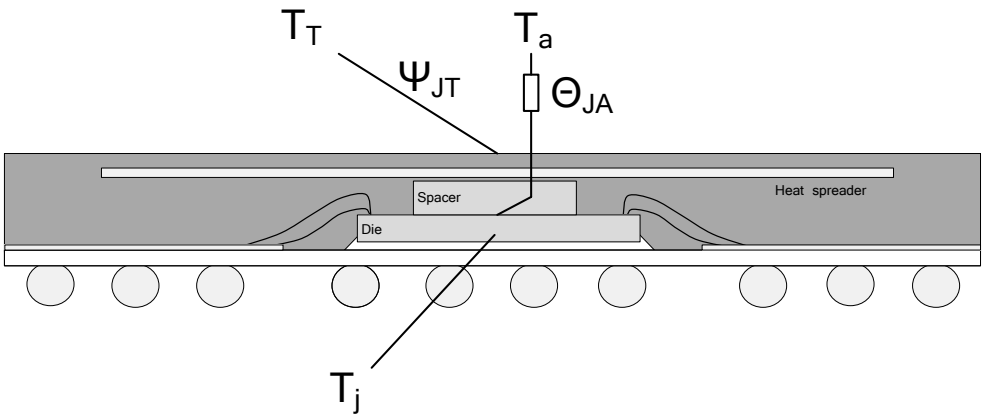

Figure 2-1: Definition of thermal parameters

Θ_{JA} is the thermal resistance between ambient temperature (T_a) and the junction temperature (T_j).

Ψ_{JT} is the thermal resistance between the junction temperature (T_j) and the top of package temperature (T_T).

In order to keep stable operation of the device, the silicon die junction temperature T_j must not exceed 125°C. This limits the maximum allowed ambient temperature $T_{a,max}$ and the maximum allowed case temperature measured at the top-center of the package $T_{T,max}$. The maximum power consumption of the device (dynamic and leakage) $P_{max}(T)$ [W] has to be controlled in a way that the following formula is fulfilled for all conditions:

$$T_{a,\max} \le 125°C - P_{\max}(T) * \Theta_{JA} \quad \text{and} \quad T_{T,\max} \le 125°C - P_{\max}(T) * \Psi_{JT}$$

Table 2-3: Thermal resistance values for JEDEC 4 layer board

Parameter	TMPR460	TMPR461/2/3
Θ_{JA}	16.4 $\frac{°C}{W}$	15.8 $\frac{°C}{W}$
Ψ_{JT}	3.5 $\frac{°C}{W}$	3.6 $\frac{°C}{W}$

When $P_{max}(T)$ is measured, both ambient temperature T_a and top package temperature T_T has to be considered, as overall power consumption has a strong temperature correlation.

2.2.1.2 Integrated Pull-up/Pull-down Resistors

Most I/O buffers have (optional/programmable) internal pull-up\Pull-down resistors which are partly activated by default. These should be deactivated according to the application to save power. This is especially important for power consumption in Low Power Modes.

3. Package

3.1 Package Types

TMPR46x have various package options:

- TMPR460XBG-300: P-BGA244-2323-1.00-001
  See paragraph 3.2.
- TMPR461XBG-300: P-BGA328-2323-1.00-001
  See paragraph 3.3.
- TMPR462XBG-300: The package for this is same as TMPR461XBG-300, but with 32Mbit SIP Flash.
  See paragraph 3.3.
- TMPR463XBG-300: The package for this is same as TMPR461XBG-300, but with 64Mbit SIP Flash.
  See paragraph 3.3.

3.2 TMPR460XBG-300

3.2.1 Package Dimensions of P-BGA244-2323-1.00-001

Unit: mm

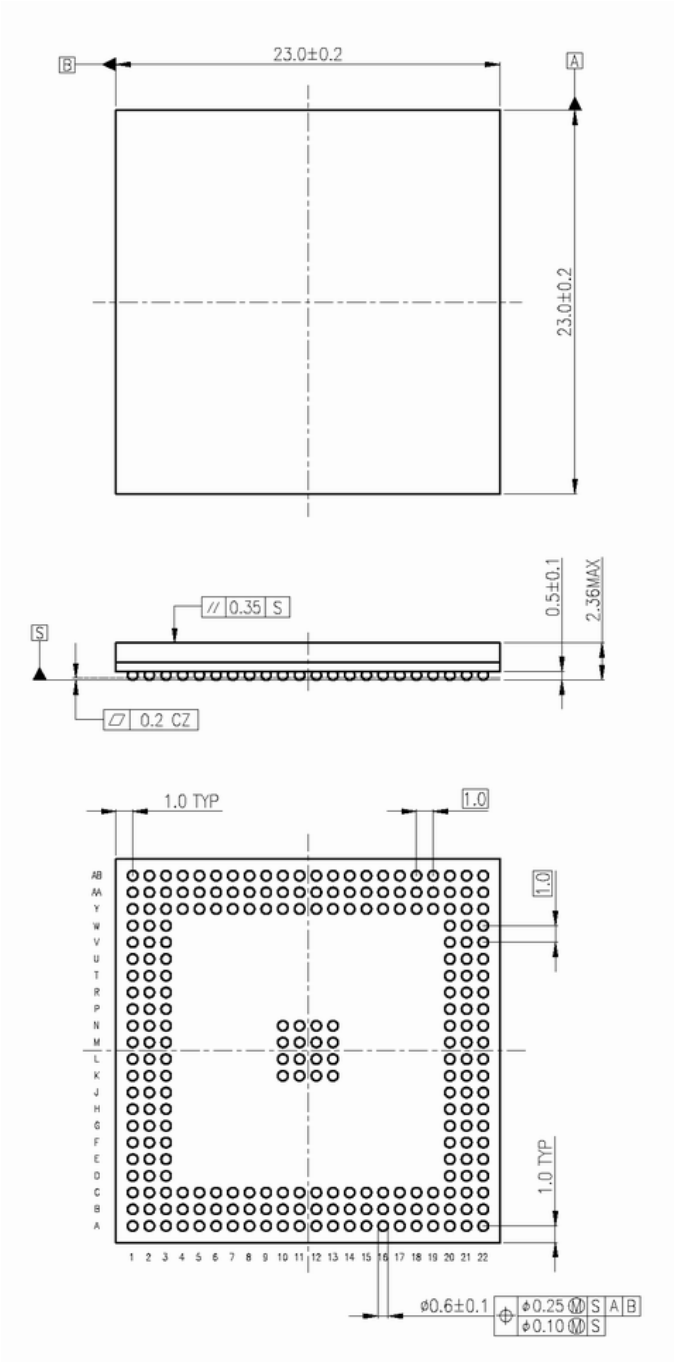

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Figure 3-1: BGA244 Package Dimensions: Top View, Side View, and Bottom View

Note: This picture is a reference. Please ask our sales representative for dimensions not described here.

3.2.2 Ball Layout of TMPR460

	A	B	C	D	E	F	G	H	J	K	L
22	PG1	QSPI0_SIO1	CANRX1	CANRX0	DDR_DQS3	DDR_DM3	DDR_DQ30	DDR_DQ28	DDR_DQ26	DDR_DQ24	DDR_DQ23
21	QSPI0_SIO2	QSPI0_SIO3	QSPI0_SIO0	CANTX1	CANTX0	PG6	DDR_DQ31	DDR_DQ29	DDR_DQ27	DDR_DQ25	DDR_DQS2
20	QSPI0_CS0	QSPI0_SCLK	PG3	PG2	PG1	PG3	PG1	PG2	PG1	PG6	PG1
19	PG7	PG1	PG7								
18	SC0_C0_RIGHT	SC0_C0_LEFT	PG1								
17	SC0_C1_RIGHT	SC0_C1_LEFT	PG7								
16	SC1_C0_RIGHT	SC1_C0_LEFT	PG1								
15	SC1_C1_RIGHT	SC1_C1_LEFT	PG7								
14	SC2_C0_RIGHT	SC2_C0_LEFT	PG1								
13	SC2_C1_RIGHT	SC2_C1_LEFT	PG1							PG4	PG4
12	SC3_C0_RIGHT	SC3_C0_LEFT	PG7							PG4	PG4
11	SC3_C1_RIGHT	SC3_C1_LEFT	PG1							PG4	PG4
10	PG7	PG1	PG7							PG4	PG4
9	NMI	RESETN	PG3								
8	DSU_JTAG_SEL	HSPWM0	PG2								
7	DSU_GTDI	DSU_GTMS	PG1								
6	DSU_TPC0_GTDO	DSU_GTCK	PG3								
5	VREG_PASSTR	DSU_GTRST	PG2								
4	VREG_SENSE	VREG_VSS	PG1								
3	ALARM_SENSE	I2CDATA	PG3	PG1	PG2	PG1	PG2	PG1	PG3	PG1	PLL_AVD
2	I2CCLK	VREG_CAP11	ADC_IN6	ADC_IN4	ADC_IN3	ADC_IN1	ADC_AVDD33	XTAL10M_OUT	XTAL32K_OUT	D0HDISP	D0HSYNC
1	PG1	ADC_IN7	ADC_IN5	ADC_IN2	ADC_IN0	ADC_AVSS33	PG1	XTAL10M_IN	XTAL32K_IN	PG3	D0VSYNC
	A	B	C	D	E	F	G	H	J	K	L

Figure 3-2: TMPR460 Ball Layout Part-1

M	N	P	R	T	U	V	W	Y	AA	AB	
DDR_DQ19	DDR_DQ22	DDR_DQ20	DDR_DQ16	DDR_A11	DDR_A8	DDR_A13	DDR_A9	DDR_A5	DDR_A3	PG1	22
DDR_DM2	DDR_DQ21	DDR_DQ17	DDR_DQ18	PG6	DDR_A12	DDR_A10	DDR_A7	DDR_A6	PG1	DDR_A1	21
PG2	PG1	PG6	PG1	PG2	PG1	PG5	PG1	PG5	DDR_A4	DDR_A2	20
								PG1	DDR_A0	DDR_CKN	19
								PG2	DDR_CK	PG5	18
								PG1	DDR_CKE	DDR_BA1	17
								PG5	DDR_BA0	DDR_CS	16
								PG1	DDR_CAS	DDR_RAS	15
								PG2	DDR_WE	DDR_DQS1	14
PG4	PG4							PG1	DDR_DM1	DDR_DQ15	13
PG4	PG4							PG5	DDR_DQ14	DDR_DQ13	12
PG4	PG4							PG1	DDR_DQ11	DDR_DQ12	11
PG4	PG4							PG2	DDR_DQ9	DDR_DQ10	10
								PG1	DDR_DQS0	DDR_DQ8	9
								PG5	DDR_DQ7	DDR_DM0	8
								PG1	DDR_DQ6	DDR_DQ5	7
								PG3	DDR_DQ4	DDR_DQ3	6
								PG1	DDR_DQ2	DDR_DQ1	5
								PG2	PG5	DDR_DQ0	4
PG2	PG2	PG1	PG3	PG1	PG2	PG1	PG3	PG1	D0RGB18	D0RGB23	3
D0DOTCLK	PNLGPP2	D0RGB2	D0RGB5	D0RGB7	D0RGB11	D0RGB10	D0RGB14	D0RGB15	D0RGB13	D0RGB20	2
PNLGPP3	PNLGPP0	PNLGPP1	D0RGB3	D0RGB4	D0RGB6	D0RGB12	D0RGB19	D0RGB21	D0RGB22	PG1	1
M	N	P	R	T	U	V	W	Y	AA	AB	

Figure 3-3: TMPR460 Ball Layout Part-2

The following list gives an explanation of the names used for power related signals in the tables:

Table 3-1: TMPR460 Package Power Planes

Pin Name	Function	Description
PG1/PG4	VSS	Common ground (internal logic, I/O buffers, Analog IP's)
PG2	VDDC	1.1V Power Supply for internal logic
PG3	VDD33	3.3V Power Supply for internal logic and I/O Buffers
PG5	VDDH_DDRA	3.3V or 1.8V Power Supply for DRAM I/O Buffers
PG6	VDDH_DDRB	3.3V or 1.8V Power Supply for DRAM I/O Buffers
PG7	VDD50	5V Power Supply for Stepper Motor I/O Buffers

3.2.3 Pin Assignment

The table in this section lists the pins of TMPR460 and additional details for each pin, such as default pull up/down, impedance, direction and PORT MUX settings.

The following abbreviations are used

a) in the Comments column

- **IN**: Standard input multipurpose buffer, selectable Schmitt-trigger function, and selectable pull-up/down feature.
- **INA**: Standard Schmitt-trigger input buffer with analog feed through, power down, and selectable pull-up/down feature.
- **BD-37.5OHM**: Standard bi-directional multipurpose buffer with typical impedance settings between 37.5 Ω and 150 Ω, selectable pull-up/down feature, and selectable Schmitt-trigger function.
- **BD-50OHM**: Standard bi-directional multipurpose buffer with typical impedance settings between 50 Ω and 100 Ω, selectable pull-up/down feature, and selectable Schmitt-trigger function.
- **BD-5VTOL:** Standard bi-directional 5V tolerant push/pull buffer with selectable pull-up/down feature
- **Alarm Comp:** Analog 3.3V bidirectional pin used for Alarm Comparator Input, see paragraph 8.9 "Alarm Comparator" of the Datasheet.
- **OSC10M:** Oscillator cell for 10MHz crystal, see paragraph 34.4 "Crystal Oscillators" of the Datasheet.
- **OSC32K:** Oscillator cell for 32kHz crystal, see paragraph 34.4 "Crystal Oscillators" of the Datasheet.
- **SMC:** 5V Stepper Motor IO Driver,
  optionally usable as
  - 5V digital (TTL) output buffer (Caution: **The output driver has a very low impedance of about 5 Ω**. The maximum allowed DC current is 50mA per buffer and 100mA for all 4 buffers of one group. Apply external series resistor to limit the maximum current.)
  - 5V or 3.3V Schmitt-trigger digital (TTL) input buffer (5V tolerant)
    3.3V operation is possible if VDD50 (PG7) Stepper Motor I/O Power Supply is 3.3V. In this case, only digital (TTL) input buffer functionality is available. Stepper Motor I/O Driver and digital (TTL) output buffer functionality cannot be used by any of these buffers.

- **VREG:** Special pins for VREGs, see paragraph 8.3 “Voltage Regulators (VREG)” of the Datasheet.
  - **VREG_SENSE:** Analog 1.1V input used for main 1.1V power supply monitoring.
    Please connect this pin directly to 1.1V VDDC (PG2) Core Power Supply
  - **VREG_PASSTR:** Analog/Digital 3.3V output used to control external pass transistor or external VREG.
  - **VREG_CAP11:** Analog 1.1V supply pin used to connect a stabilization capacitance for standby power domain (supplied by internal 1.1V VREG).
    Please connect a 1nF stabilization capacitor to this pin.
  - **VREG_VSS:** Analog Ground pin, internally (on die) connected to VSS common ground.
    Please connect this pin directly to VSS (PG1/PG4) Common Ground.
- **PLL_AVD:** Analog 1.1V supply pin used for dedicated 1.1V PLL Power Supply.

  Please connect this pin to a PLL-exclusive 1.1V power supply which is separated from other 1.1V power supplies by an appropriate filter circuit.
- **ADC_AVDD33:** Analog 3.3V supply pin used for dedicated 3.3V ADC Power Supply.

  Please connect this pin to an ADC-exclusive 3.3V power supply which is separated from other 3.3V power supplies by an appropriate filter circuit.
- **ADC_AVSS33:** Analog Ground pin used for dedicated ADC ground (separated from common ground internally).

  Please connect this pin directly to VSS (PG1/PG4) Common Ground
- **Power Related**: Signals related to power, refer to Table 3-1: TMPR460 Package Power Planes.

b) in the direction column

- **In:** Input direction
- **ADC:** ADC inputs
- **SM-In:** Stepper motor input

The abbreviations used for the headings are,

- **PU** – Default Pull-Up setting
- **PD** – Default Pull-Down setting
- **IMP0/1** – Default output buffer impedance setting
- **SMT** – Default Schmitt-Trigger setting
- **DIR** – Default direction
- **Default MUX** – Default Port Multiplexer selection after the reset removal

Table 3-2: TMPR460 Pin Assignment

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
A1	PG1	Power Related	-	-	-	-	-	-	-
A2	I2CCLK	BD-50OHM	1	0	1	1	1	In	GPIO Input
A3	ALARM_SENSE	Alarm Comp	-	-	-	-	-	-	-
A4	VREG_SENSE	VREG	-	-	-	-	-	-	-
A5	VREG_PASSTR	VREG	-	-	-	-	-	-	-

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
A6	DSU_TPC0_GTDO	BD-50OHM	1	0	1	1	0	In	Dedicated
A7	DSU_GTDI	IN	1	0	-	-	1	-	Dedicated
A8	DSU_JTAG_SEL	IN	0	1	-	-	1	-	Dedicated
A9	NMI	IN	1	0	-	-	1	-	Dedicated
A10	PG7	Power Related	-	-	-	-	-	-	-
A11	SC3_C1_RIGHT	SMC	-	-	-	-	-	SM-In	SC3_C1_RIGHT
A12	SC3_C0_RIGHT	SMC	-	-	-	-	-	SM-In	SC3_C0_RIGHT
A13	SC2_C1_RIGHT	SMC	-	-	-	-	-	SM-In	SC2_C1_RIGHT
A14	SC2_C0_RIGHT	SMC	-	-	-	-	-	SM-In	SC2_C0_RIGHT
A15	SC1_C1_RIGHT	SMC	-	-	-	-	-	SM-In	SC1_C1_RIGHT
A16	SC1_C0_RIGHT	SMC	-	-	-	-	-	SM-In	SC1_C0_RIGHT
A17	SC0_C1_RIGHT	SMC	-	-	-	-	-	SM-In	SC0_C1_RIGHT
A18	SC0_C0_RIGHT	SMC	-	-	-	-	-	SM-In	SC0_C0_RIGHT
A19	PG7	Power Related	-	-	-	-	-	-	-
A20	QSPI0_CS0	BD-50OHM	1	0	1	1	0	In	GPIO Input
A21	QSPI0_SIO2	BD-50OHM	0	1	1	1	0	In	GPIO Input
A22	PG1	Power Related	-	-	-	-	-	-	-
B1	ADC_IN7	INA	0	1	-	-	-	ADC	ADC_IN7
B2	VREG_CAP11	VREG	-	-	-	-	-	-	-
B3	I2CDATA	BD-50OHM	1	0	1	1	0	In	GPIO Input
B4	VREG_VSS	VREG	-	-	-	-	-	-	-
B5	DSU_GTRST	IN	1	0	-	-	1	-	Dedicated
B6	DSU_GTCK	IN	0	1	-	-	1	-	Dedicated
B7	DSU_GTMS	BD-50OHM	1	0	1	1	1	In	Dedicated
B8	HSPWM0	BD-50OHM	0	1	1	1	0	In	GPIO Input
B9	RESETN	IN	1	0	-	-	1	-	Dedicated
B10	PG1	Power Related	-	-	-	-	-	-	-
B11	SC3_C1_LEFT	SMC	-	-	-	-	-	SM-In	SC3_C1_LEFT
B12	SC3_C0_LEFT	SMC	-	-	-	-	-	SM-In	SC3_C0_LEFT
B13	SC2_C1_LEFT	SMC	-	-	-	-	-	SM-In	SC2_C1_LEFT
B14	SC2_C0_LEFT	SMC	-	-	-	-	-	SM-In	SC2_C0_LEFT
B15	SC1_C1_LEFT	SMC	-	-	-	-	-	SM-In	SC1_C1_LEFT
B16	SC1_C0_LEFT	SMC	-	-	-	-	-	SM-In	SC1_C0_LEFT
B17	SC0_C1_LEFT	SMC	-	-	-	-	-	SM-In	SC0_C1_LEFT
B18	SC0_C0_LEFT	SMC	-	-	-	-	-	SM-In	SC0_C0_LEFT
B19	PG1	Power Related	-	-	-	-	-	-	-
B20	QSPI0_SCLK	BD-50OHM	0	1	1	1	0	In	GPIO Input
B21	QSPI0_SIO3	BD-50OHM	0	1	1	1	0	In	GPIO Input
B22	QSPI0_SIO1	BD-50OHM	0	1	1	1	0	In	GPIO Input
C1	ADC_IN5	INA	0	1	-	-	-	ADC	ADC_IN5
C2	ADC_IN6	INA	0	1	-	-	-	ADC	ADC_IN6
C3	PG3	Power Related	-	-	-	-	-	-	-
C4	PG1	Power Related	-	-	-	-	-	-	-
C5	PG2	Power Related	-	-	-	-	-	-	-
C6	PG3	Power Related	-	-	-	-	-	-	-
C7	PG1	Power Related	-	-	-	-	-	-	-
C8	PG2	Power Related	-	-	-	-	-	-	-
C9	PG3	Power Related	-	-	-	-	-	-	-

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
C10	PG7	Power Related	-	-	-	-	-	-	-
C11	PG1	Power Related	-	-	-	-	-	-	-
C12	PG7	Power Related	-	-	-	-	-	-	-
C13	PG1	Power Related	-	-	-	-	-	-	-
C14	PG1	Power Related	-	-	-	-	-	-	-
C15	PG7	Power Related	-	-	-	-	-	-	-
C16	PG1	Power Related	-	-	-	-	-	-	-
C17	PG7	Power Related	-	-	-	-	-	-	-
C18	PG1	Power Related	-	-	-	-	-	-	-
C19	PG7	Power Related	-	-	-	-	-	-	-
C20	PG3	Power Related	-	-	-	-	-	-	-
C21	QSPI0_SIO0	BD-50OHM	0	1	1	1	0	In	GPIO Input
C22	CANRX1	BD-5VTOL	0	1	-	-	-	In	GPIO Input
D1	ADC_IN2	INA	0	1	-	-	-	ADC	ADC_IN2
D2	ADC_IN4	INA	0	1	-	-	-	ADC	ADC_IN4
D3	PG1	Power Related	-	-	-	-	-	-	-
D20	PG2	Power Related	-	-	-	-	-	-	-
D21	CANTX1	BD-50OHM	1	0	1	1	0	In	GPIO Input
D22	CANRX0	BD-5VTOL	0	1	-	-	-	In	GPIO Input
E1	ADC_IN0	INA	0	1	-	-	-	ADC	ADC_IN0
E2	ADC_IN3	INA	0	1	-	-	-	ADC	ADC_IN3
E3	PG2	Power Related	-	-	-	-	-	-	-
E20	PG1	Power Related	-	-	-	-	-	-	-
E21	CANTX0	BD-50OHM	1	0	1	1	0	In	GPIO Input
E22	DDR_DQS3	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
F1	ADC_AVSS33	ADC_AVSS33	-	-	-	-	-	-	-
F2	ADC_IN1	INA	0	1	-	-	-	ADC	ADC_IN1
F3	PG1	Power Related	-	-	-	-	-	-	-
F20	PG3	Power Related	-	-	-	-	-	-	-
F21	PG6	Power Related	-	-	-	-	-	-	-
F22	DDR_DM3	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
G1	PG1	Power Related	-	-	-	-	-	-	-
G2	ADC_AVDD33	ADC_AVDD33	-	-	-	-	-	-	-
G3	PG2	Power Related	-	-	-	-	-	-	-
G20	PG1	Power Related	-	-	-	-	-	-	-
G21	DDR_DQ31	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
G22	DDR_DQ30	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
H1	XTAL10M_IN	OSC10M	-	-	-	-	-	In	-
H2	XTAL10M_OUT	OSC10M	-	-	-	-	-	Out	-
H3	PG1	Power Related	-	-	-	-	-	-	-
H20	PG2	Power Related	-	-	-	-	-	-	-
H21	DDR_DQ29	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
H22	DDR_DQ28	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
J1	XTAL32K_IN	OSC32K	-	-	-	-	-	In	-
J2	XTAL32K_OUT	OSC32K	-	-	-	-	-	Out	-
J3	PG3	Power Related	-	-	-	-	-	-	-
J20	PG1	Power Related	-	-	-	-	-	-	-
J21	DDR_DQ27	BD-37.5OHM	0	1	0	0	0	In	GPIO Input

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
J22	DDR_DQ26	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
K1	PG3	Power Related	-	-	-	-	-	-	-
K2	D0HDISP	BD-50OHM	0	1	1	1	0	In	GPIO Input
K3	PG1	Power Related	-	-	-	-	-	-	-
K10	PG4	Power Related	-	-	-	-	-	-	-
K11	PG4	Power Related	-	-	-	-	-	-	-
K12	PG4	Power Related	-	-	-	-	-	-	-
K13	PG4	Power Related	-	-	-	-	-	-	-
K20	PG6	Power Related	-	-	-	-	-	-	-
K21	DDR_DQ25	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
K22	DDR_DQ24	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
L1	D0VSYNC	BD-50OHM	0	1	1	1	0	In	GPIO Input
L2	D0HSYNC	BD-50OHM	0	1	1	1	0	In	GPIO Input
L3	PLL_AVD	PLL_AVD	-	-	-	-	-	-	-
L10	PG4	Power Related	-	-	-	-	-	-	-
L11	PG4	Power Related	-	-	-	-	-	-	-
L12	PG4	Power Related	-	-	-	-	-	-	-
L13	PG4	Power Related	-	-	-	-	-	-	-
L20	PG1	Power Related	-	-	-	-	-	-	-
L21	DDR_DQS2	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
L22	DDR_DQ23	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
M1	PNLGPP3	BD-50OHM	1	0	1	1	0	In	TSM_GTRST
M2	D0DOTCLK	BD-50OHM	0	1	1	1	0	In	GPIO Input
M3	PG2	Power Related	-	-	-	-	-	-	-
M10	PG4	Power Related	-	-	-	-	-	-	-
M11	PG4	Power Related	-	-	-	-	-	-	-
M12	PG4	Power Related	-	-	-	-	-	-	-
M13	PG4	Power Related	-	-	-	-	-	-	-
M20	PG2	Power Related	-	-	-	-	-	-	-
M21	DDR_DM2	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
M22	DDR_DQ19	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
N1	PNLGPP0	BD-50OHM	1	0	1	1	0	In	TSM_GTMS
N2	PNLGPP2	BD-50OHM	0	1	1	1	0	In	TSM_GTCK
N3	PG2	Power Related	-	-	-	-	-	-	-
N10	PG4	Power Related	-	-	-	-	-	-	-
N11	PG4	Power Related	-	-	-	-	-	-	-
N12	PG4	Power Related	-	-	-	-	-	-	-
N13	PG4	Power Related	-	-	-	-	-	-	-
N20	PG1	Power Related	-	-	-	-	-	-	-
N21	DDR_DQ21	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
N22	DDR_DQ22	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
P1	PNLGPP1	BD-50OHM	1	0	1	1	0	In	TSM_GTDI
P2	D0RGB2	BD-50OHM	0	1	1	1	0	In	GPIO Input
P3	PG1	Power Related	-	-	-	-	-	-	-
P20	PG6	Power Related	-	-	-	-	-	-	-
P21	DDR_DQ17	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
P22	DDR_DQ20	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
R1	D0RGB3	BD-50OHM	0	1	1	1	0	In	GPIO Input

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
R2	D0RGB5	BD-50OHM	0	1	1	1	0	In	GPIO Input
R3	PG3	Power Related	-	-	-	-	-	-	-
R20	PG1	Power Related	-	-	-	-	-	-	-
R21	DDR_DQ18	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
R22	DDR_DQ16	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
T1	D0RGB4	BD-50OHM	0	1	1	1	0	In	GPIO Input
T2	D0RGB7	BD-50OHM	0	1	1	1	0	In	GPIO Input
T3	PG1	Power Related	-	-	-	-	-	-	-
T20	PG2	Power Related	-	-	-	-	-	-	-
T21	PG6	Power Related	-	-	-	-	-	-	-
T22	DDR_A11	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
U1	D0RGB6	BD-50OHM	0	1	1	1	0	In	GPIO Input
U2	D0RGB11	BD-50OHM	0	1	1	1	0	In	GPIO Input
U3	PG2	Power Related	-	-	-	-	-	-	-
U20	PG1	Power Related	-	-	-	-	-	-	-
U21	DDR_A12	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
U22	DDR_A8	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
V1	D0RGB12	BD-50OHM	0	1	1	1	0	In	GPIO Input
V2	D0RGB10	BD-50OHM	0	1	1	1	0	In	GPIO Input
V3	PG1	Power Related	-	-	-	-	-	-	-
V20	PG5	Power Related	-	-	-	-	-	-	-
V21	DDR_A10	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
V22	DDR_A13	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W1	D0RGB19	BD-50OHM	0	1	1	1	0	In	GPIO Input
W2	D0RGB14	BD-50OHM	0	1	1	1	0	In	GPIO Input
W3	PG3	Power Related	-	-	-	-	-	-	-
W20	PG1	Power Related	-	-	-	-	-	-	-
W21	DDR_A7	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W22	DDR_A9	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
Y1	D0RGB21	BD-50OHM	0	1	1	1	0	In	GPIO Input
Y2	D0RGB15	BD-50OHM	0	1	1	1	0	In	TSM_TPC0_GTDO
Y3	PG1	Power Related	-	-	-	-	-	-	-
Y4	PG2	Power Related	-	-	-	-	-	-	-
Y5	PG1	Power Related	-	-	-	-	-	-	-
Y6	PG3	Power Related	-	-	-	-	-	-	-
Y7	PG1	Power Related	-	-	-	-	-	-	-
Y8	PG5	Power Related	-	-	-	-	-	-	-
Y9	PG1	Power Related	-	-	-	-	-	-	-
Y10	PG2	Power Related	-	-	-	-	-	-	-
Y11	PG1	Power Related	-	-	-	-	-	-	-
Y12	PG5	Power Related	-	-	-	-	-	-	-
Y13	PG1	Power Related	-	-	-	-	-	-	-
Y14	PG2	Power Related	-	-	-	-	-	-	-
Y15	PG1	Power Related	-	-	-	-	-	-	-
Y16	PG5	Power Related	-	-	-	-	-	-	-
Y17	PG1	Power Related	-	-	-	-	-	-	-
Y18	PG2	Power Related	-	-	-	-	-	-	-
Y19	PG1	Power Related	-	-	-	-	-	-	-

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
Y20	PG5	Power Related	-	-	-	-	-	-	-
Y21	DDR_A6	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
Y22	DDR_A5	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA1	D0RGB22	BD-50OHM	0	1	1	1	0	In	GPIO Input
AA2	D0RGB13	BD-50OHM	0	1	1	1	0	In	GPIO Input
AA3	D0RGB18	BD-50OHM	0	1	1	1	0	In	GPIO Input
AA4	PG5	Power Related	-	-	-	-	-	-	-
AA5	DDR_DQ2	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA6	DDR_DQ4	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA7	DDR_DQ6	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA8	DDR_DQ7	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA9	DDR_DQS0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA10	DDR_DQ9	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA11	DDR_DQ11	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA12	DDR_DQ14	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA13	DDR_DM1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA14	DDR_WE	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA15	DDR_CAS	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA16	DDR_BA0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA17	DDR_CKE	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA18	DDR_CK	BD-37.5OHM	0	1	0	0	0	In	Dedicated
AA19	DDR_A0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA20	DDR_A4	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA21	PG1	Power Related	-	-	-	-	-	-	-
AA22	DDR_A3	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB1	PG1	Power Related	-	-	-	-	-	-	-
AB2	D0RGB20	BD-50OHM	0	1	1	1	0	In	GPIO Input
AB3	D0RGB23	BD-50OHM	0	1	1	1	0	In	GPIO Input
AB4	DDR_DQ0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB5	DDR_DQ1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB6	DDR_DQ3	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB7	DDR_DQ5	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB8	DDR_DM0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB9	DDR_DQ8	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB10	DDR_DQ10	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB11	DDR_DQ12	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB12	DDR_DQ13	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB13	DDR_DQ15	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB14	DDR_DQS1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB15	DDR_RAS	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB16	DDR_CS	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB17	DDR_BA1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB18	PG5	Power Related	-	-	-	-	-	-	-
AB19	DDR_CKN	BD-37.5OHM	0	1	0	0	0	In	Dedicated
AB20	DDR_A2	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB21	DDR_A1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB22	PG1	Power Related	-	-	-	-	-	-	-

3.3 TMPR461XBG-300 / TMPR462XBG-300 / TMPR463XBG-300

3.3.1 Package Dimensions of P-BGA328-2323-1.00-001

Unit: mm

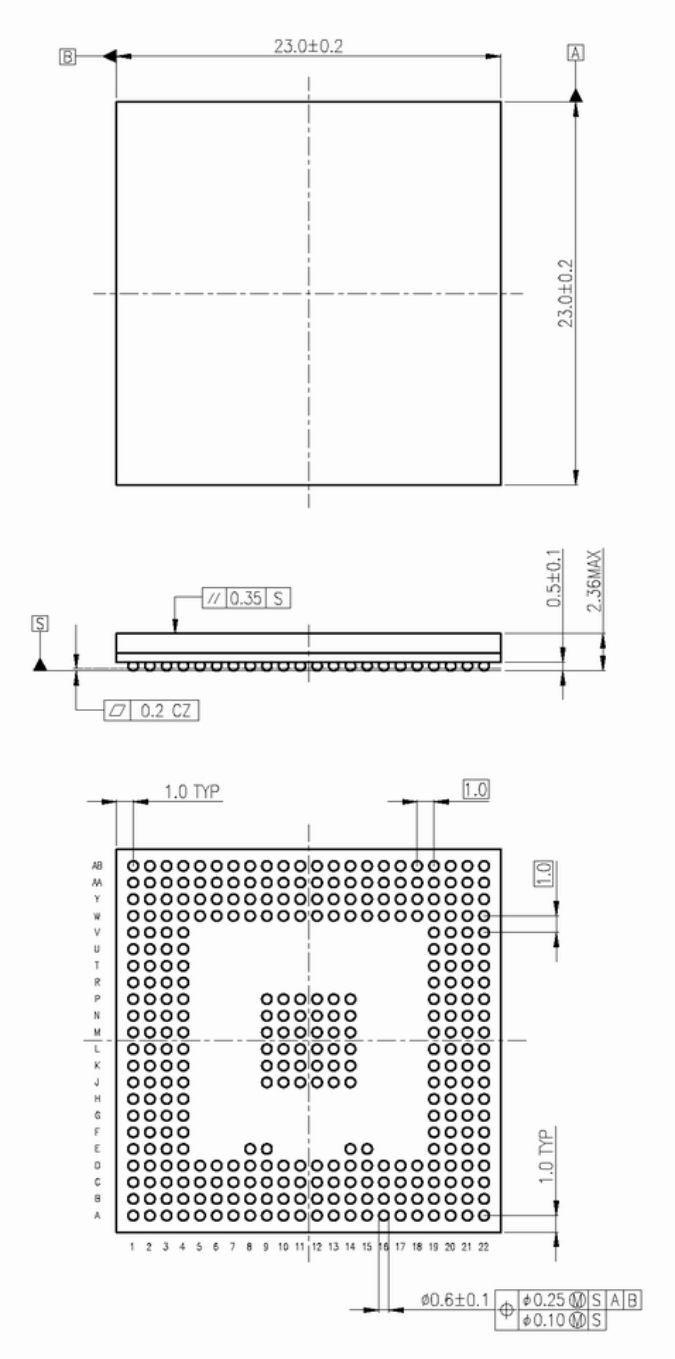

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Figure 3-4: BGA328 Package Dimensions: Top View, Side View, and Bottom View

Note: This picture is a reference. Please ask our sales representative for dimensions not described here.

3.3.2 Ball Layout TMPR461 / TMPR462 / TMPR463

	A	B	C	D	E	F	G	H	J	K	L
22	PG1	CMY7	UART0RX	UART0TX	CMVSYNC	CMY2	CMCBCR7	CMCBCR3	CMCBCR4	CMCBCR0	DDR_DQ31
21	CMRGB5	PG3	CMRGB1	CMY5	CMY1	PG3	CMY0	CMHDISP	CMCBCR6	PG3	DDR_DQS3
20	CANTX0	CANRX0	CMRGB6	CMRGB3	CMRGB0	CMY3	PG1	CMHSYNC	CMCBCR5	CMCBCR1	PG1
19	QSPI0_SIO2	CANTX1	CANRX1	CMRGB7	CMRGB4	CMRGB2	CMY6	CMY4	CMFODD	CMCLK	CMCBCR2
18	QSPI0_SIO3	QSPI0_CS0	QSPI0_SIO1	QSPI0_SIO0							
17	PG3	PG2	QSPI0_SCLK	PWMOUT00							
16	SC0_C1_RIGHT	SC0_C1_LEFT	SC0_C0_LEFT	SC0_C0_RIGHT							
15	PG1	PG7	PG1	PG7	SCLK						
14	SC1_C1_RIGHT	SC1_C1_LEFT	SC1_C0_LEFT	SC1_C0_RIGHT	SIP_QSPI_SCLK				PG2	PG4	PG2
13	SC2_C1_RIGHT	SC2_C1_LEFT	SC2_C0_LEFT	SC2_C0_RIGHT					PG4	PG4	PG4
12	SC3_C1_RIGHT	SC3_C1_LEFT	SC3_C0_LEFT	SC3_C0_RIGHT					PG2	PG4	PG4
11	PG1	PG7	PG1	PG7					PG2	PG4	PG4
10	SC4_C1_RIGHT	SC4_C1_LEFT	SC4_C0_LEFT	SC4_C0_RIGHT					PG4	PG4	PG2
9	PG3	PG1	NMI	RESETN	CS				PG2	PG4	PG2
8	HSPWM1N	HSPWM1	HSPWM0N	HSPWM0	SIP_QSPI_CS						
7	ESEI0MOSI	ESEI0MISO	ESEI0SCLK	DSU_JTAG_SEL							
6	VREG_VSS	ESEI0SSOI	DSU_GTCK	DSU_GTMS							
5	VREG_CAP11	VREG_SENSE	PG3	DSU_GTDI							
4	VREG_PASSTR	PG1	DSU_GTRST	DSU_TPC0_GTDO	ALARM_SENSE	ADC_IN13	ADC_IN7	ADC_IN10	PNLGPP7	D0HDISP	PNLGPP2
3	I2CDATA	I2S0WS	I2S0CLK	I2SMCLK	I2S0SD	ADC_IN5	ADC_IN6	ADC_IN0	D0VSYNC	PNLGPP3	D0HSYNC
2	I2CCLK	PG3	ADC_IN11	ADC_IN12	ADC_IN1	ADC_IN4	ADC_AVDD33	PG3	PNLGPP0	XTAL10M_IN	XTAL32K_IN
1	PG1	ADC_IN9	ADC_IN3	ADC_IN8	ADC_IN2	ADC_AVSS33	PLL_AVD	PG1	PG1	XTAL10M_OUT	XTAL32K_OUT
	A	B	C	D	E	F	G	H	J	K	L

Figure 3-5: TMPR461/2/3 Ball Layout Part-1

M	N	P	R	T	U	V	W	Y	AA	AB	
DDR_DQ27	DDR_DQ28	DDR_DQ26	DDR_DQ21	DDR_DQ20	DDR_DQ17	DDR_A12	DDR_A8	DDR_A6	DDR_A2	PG1	22
PG6	DDR_DQ30	DDR_DQ24	DDR_DM2	PG6	DDR_DQ18	DDR_A10	DDR_A7	DDR_A3	PG5	DDR_BA1	21
DDR_DM3	PG1	DDR_DQS2	DDR_DQ19	PG1	DDR_A13	DDR_A9	DDR_A4	DDR_CKN	DDR_CK	DDR_CKE	20
DDR_DQ29	DDR_DQ25	DDR_DQ23	DDR_DQ22	DDR_DQ16	DDR_A11	DDR_A5	DDR_A1	PG1	DDR_BA0	DDR_RAS	19
							DDR_A0	DDR_CS	PG5	DDR_DM1	18
							DDR_CAS	DDR_WE	DDR_DQ15	DDR_DQ14	17
							DDR_DQS1	PG1	DDR_DQ12	DDR_DQ11	16
							DDR_DQ13	DDR_DQ10	PG5	DDR_DQ8	15
PG2	PG4	PG2					DDR_DQ9	DDR_DQS0	DDR_DQ7	DDR_DM0	14
PG2	PG4	PG4					DDR_DQ6	PG1	DDR_DQ5	DDR_DQ4	13
PG4	PG4	PG2					DDR_DQ1	DDR_DQ2	PG5	DDR_DQ3	12
PG4	PG4	PG2					D1RGB21	D1RGB23	D1RGB22	DDR_DQ0	11
PG4	PG4	PG4					D1RGB17	D1RGB18	D1RGB19	D1RGB20	10
PG2	PG4	PG2					D1RGB13	PG1	D1RGB15	D1RGB16	9
							D1RGB12	MLBCLK	PG3	D1RGB14	8
							D1RGB5	D1RGB10	MLBDAT_IO	MLBSIG_IO	7
							D1RGB2	D1RGB6	D1RGB9	D1RGB11	6
							D1VSYNC	PG1	D1RGB7	D1RGB8	5
D0DOTCLK	D0RGB3	PNLGPP5	D0RGB8	D0RGB10	D0RGB11	D0RGB18	D0RGB23	D1DOTCLK	PG3	D1RGB4	4
PG1	D0RGB5	D0RGB4	D0RGB16	PG1	D0RGB1	D0RGB13	D0RGB21	D1HSYNC	D1RGB0	D1RGB3	3
PG3	D0RGB2	DOTCLKIN	PNLGPP6	D0RGB9	PG3	D0RGB12	D0RGB19	D0RGB22	PG3	D1RGB1	2
PNLGPP1	D0RGB7	D0RGB6	D0RGB0	PNLGPP4	D0RGB17	D0RGB14	D0RGB15	D0RGB20	D1HDISP	PG1	1
M	N	P	R	T	U	V	W	Y	AA	AB	

Figure 3-6: TMPR461/2/3 Ball Layout Part-2

The following table gives an explanation of the names used for power related signals.

Table 3-3: TMPR461/2/3 Package Power Planes

Pin Name	Function	Description
PG1/PG4	VSS	Common ground (internal logic, I/O buffers, Analog IP's)
PG2	VDDC	1.1V Power Supply for internal logic
PG3	VDD33	3.3V Power Supply for internal logic and I/O Buffers
PG5	VDDH_DDRA	3.3V or 1.8V Power Supply for DRAM I/O Buffers
PG6	VDDH_DDRB	3.3V or 1.8V Power Supply for DRAM I/O Buffers
PG7	VDD50	5V Power Supply for Stepper Motor I/O Buffers

3.3.3 Pin Assignment

The table in this section lists the pins of TMPR461/2/3 and additional details for each pin, such as default pull up/down, impedance, direction and PORT MUX settings.

Explanations for the abbreviations used in the comments column, in the direction column, and for the table headings are given in paragraph 3.2.3 above.

Table 3-4: TMPR461/2/3 Pin Assignment

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
A1	PG1	Power Related	-	-	-	-	-	-	-
A2	I2CCLK	BD-50OHM	1	0	1	1	1	In	GPIO Input
A3	I2CDATA	BD-50OHM	1	0	1	1	0	In	GPIO Input
A4	VREG_PASSTR	VREG	-	-	-	-	-	-	-
A5	VREG_CAP11	VREG	-	-	-	-	-	-	-
A6	VREG_VSS	VREG	-	-	-	-	-	-	-
A7	ESEI0MOSI	BD-5VTOL	0	1	-	-	-	In	GPIO Input
A8	HSPWM1N	BD-50OHM	1	0	1	1	0	In	GPIO Input
A9	PG3	Power Related	-	-	-	-	-	-	-
A10	SC4_C1_RIGHT	SMC	-	-	-	-	-	SM-In	SC4_C1_RIGHT
A11	PG1	Power Related	-	-	-	-	-	-	-
A12	SC3_C1_RIGHT	SMC	-	-	-	-	-	SM-In	SC3_C1_RIGHT
A13	SC2_C1_RIGHT	SMC	-	-	-	-	-	SM-In	SC2_C1_RIGHT
A14	SC1_C1_RIGHT	SMC	-	-	-	-	-	SM-In	SC1_C1_RIGHT
A15	PG1	Power Related	-	-	-	-	-	-	-
A16	SC0_C1_RIGHT	SMC	-	-	-	-	-	SM-In	SC0_C1_RIGHT
A17	PG3	Power Related	-	-	-	-	-	-	-
A18	QSPI0_SIO3	BD-50OHM	0	1	1	1	0	In	GPIO Input
A19	QSPI0_SIO2	BD-50OHM	0	1	1	1	0	In	GPIO Input
A20	CANTX0	BD-50OHM	1	0	1	1	0	In	GPIO Input
A21	CMRGB5	BD-50OHM	1	0	1	1	0	In	CMRGB5
A22	PG1	Power Related	-	-	-	-	-	-	-
B1	ADC_IN9	INA	0	1	-	-	-	ADC	ADC_IN9
B2	PG3	Power Related	-	-	-	-	-	-	-
B3	I2S0WS	BD-50OHM	0	1	1	1	0	In	GPIO Input
B4	PG1	Power Related	-	-	-	-	-	-	-
B5	VREG_SENSE	VREG	-	-	-	-	-	-	-
B6	ESEI0SSOI	BD-5VTOL	1	0	-	-	-	In	GPIO Input

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
B7	ESEI0MISO	BD-5VTOL	0	1	-	-	-	In	GPIO Input
B8	HSPWM1	BD-50OHM	0	1	1	1	0	In	GPIO Input
B9	PG1	Power Related	-	-	-	-	-	-	-
B10	SC4_C1_LEFT	SMC	-	-	-	-	-	SM-In	SC4_C1_LEFT
B11	PG7	Power Related	-	-	-	-	-	-	-
B12	SC3_C1_LEFT	SMC	-	-	-	-	-	SM-In	SC3_C1_LEFT
B13	SC2_C1_LEFT	SMC	-	-	-	-	-	SM-In	SC2_C1_LEFT
B14	SC1_C1_LEFT	SMC	-	-	-	-	-	SM-In	SC1_C1_LEFT
B15	PG7	Power Related	-	-	-	-	-	-	-
B16	SC0_C1_LEFT	SMC	-	-	-	-	-	SM-In	SC0_C1_LEFT
B17	PG2	Power Related	-	-	-	-	-	-	-
B18	QSPI0_CS0	BD-50OHM	1	0	1	1	0	In	GPIO Input
B19	CANTX1	BD-50OHM	1	0	1	1	0	In	GPIO Input
B20	CANRX0	BD-5VTOL	0	1	-	-	-	In	GPIO Input
B21	PG3	Power Related	-	-	-	-	-	-	-
B22	CMY7	BD-50OHM	0	1	1	1	0	In	CMY7
C1	ADC_IN3	INA	0	1	-	-	-	ADC	ADC_IN3
C2	ADC_IN11	INA	0	1	-	-	-	ADC	ADC_IN11
C3	I2S0CLK	BD-50OHM	0	1	1	1	0	In	GPIO Input
C4	DSU_GTRST	IN	1	0	-	-	1	-	Dedicated
C5	PG3	Power Related	-	-	-	-	-	-	-
C6	DSU_GTCK	IN	0	1	-	-	1	-	Dedicated
C7	ESEI0SCLK	BD-5VTOL	0	1	-	-	-	In	GPIO Input
C8	HSPWM0N	BD-50OHM	0	1	1	1	0	In	GPIO Input
C9	NMI	IN	1	0	-	-	1	-	Dedicated
C10	SC4_C0_LEFT	SMC	-	-	-	-	-	SM-In	SC4_C0_LEFT
C11	PG1	Power Related	-	-	-	-	-	-	-
C12	SC3_C0_LEFT	SMC	-	-	-	-	-	SM-In	SC3_C0_LEFT
C13	SC2_C0_LEFT	SMC	-	-	-	-	-	SM-In	SC2_C0_LEFT
C14	SC1_C0_LEFT	SMC	-	-	-	-	-	SM-In	SC1_C0_LEFT
C15	PG1	Power Related	-	-	-	-	-	-	-
C16	SC0_C0_LEFT	SMC	-	-	-	-	-	SM-In	SC0_C0_LEFT
C17	QSPI0_SCLK	BD-50OHM	0	1	1	1	0	In	GPIO Input
C18	QSPI0_SIO1	BD-50OHM	0	1	1	1	0	In	GPIO Input
C19	CANRX1	BD-5VTOL	0	1	-	-	-	In	GPIO Input
C20	CMRGB6	BD-50OHM	0	1	1	1	0	In	CMRGB6
C21	CMRGB1	BD-50OHM	0	1	1	1	0	In	CMRGB1
C22	UART0RX	BD-50OHM	0	1	1	1	0	In	GPIO Input
D1	ADC_IN8	INA	0	1	-	-	-	ADC	ADC_IN8
D2	ADC_IN12	INA	0	1	-	-	-	ADC	ADC_IN12
D3	I2SMCLK	BD-50OHM	1	0	1	1	1	In	GPIO Input
D4	DSU_TPC0_GTDO	BD-50OHM	1	0	1	1	0	In	Dedicated
D5	DSU_GTDI	IN	1	0	-	-	1	-	Dedicated
D6	DSU_GTMS	BD-50OHM	1	0	1	1	1	In	Dedicated
D7	DSU_JTAG_SEL	IN	0	1	-	-	1	-	Dedicated
D8	HSPWM0	BD-50OHM	0	1	1	1	0	In	GPIO Input
D9	RESETN	IN	1	0	-	-	1	-	Dedicated
D10	SC4_C0_RIGHT	SMC	-	-	-	-	-	SM-In	SC4_C0_RIGHT
D11	PG7	Power Related	-	-	-	-	-	-	-
D12	SC3_C0_RIGHT	SMC	-	-	-	-	-	SM-In	SC3_C0_RIGHT
D13	SC2_C0_RIGHT	SMC	-	-	-	-	-	SM-In	SC2_C0_RIGHT
D14	SC1_C0_RIGHT	SMC	-	-	-	-	-	SM-In	SC1_C0_RIGHT
D15	PG7	Power Related	-	-	-	-	-	-	-
D16	SC0_C0_RIGHT	SMC	-	-	-	-	-	SM-In	SC0_C0_RIGHT

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
D17	PWMOUT00	BD-50OHM	0	1	1	1	0	In	GPIO Input
D18	QSPI0_SIO0	BD-50OHM	0	1	1	1	0	In	GPIO Input
D19	CMRGB7	BD-50OHM	1	0	1	1	0	In	CMRGB7
D20	CMRGB3	BD-50OHM	1	0	1	1	0	In	CMRGB3
D21	CMY5	BD-50OHM	0	1	1	1	0	In	CMY5
D22	UART0TX	BD-50OHM	1	0	1	1	0	In	GPIO Input
E1	ADC_IN2	INA	0	1	-	-	-	ADC	ADC_IN2
E2	ADC_IN1	INA	0	1	-	-	-	ADC	ADC_IN1
E3	I2S0SD	BD-50OHM	0	1	1	1	0	In	GPIO Input
E4	ALARM_SENSE	Alarm Comp	-	-	-	-	-	-	-
E8	SIP_QSPI_CS	BD-50OHM	1	0	1	1	0	In	Dedicated
E9	CS	Please check Note1 below	-	-	-	-	-	-	-
E14	SIP_QSPI_SCLK	BD-50OHM	0	1	1	1	0	In	Dedicated
E15	SCLK	Please check Note2 below	-	-	-	-	-	-	-
E19	CMRGB4	BD-50OHM	0	1	1	1	0	In	CMRGB4
E20	CMRGB0	BD-50OHM	0	1	1	1	0	In	CMRGB0
E21	CMY1	BD-50OHM	0	1	1	1	0	In	CMY1
E22	CMVSYNC	BD-50OHM	0	1	1	1	0	In	CMVSYNC
F1	ADC_AVSS33	ADC_AVSS33	-	-	-	-	-	-	-
F2	ADC_IN4	INA	0	1	-	-	-	ADC	ADC_IN4
F3	ADC_IN5	INA	0	1	-	-	-	ADC	ADC_IN5
F4	ADC_IN13	INA	0	1	-	-	-	ADC	ADC_IN13
F19	CMRGB2	BD-50OHM	0	1	1	1	0	In	CMRGB2
F20	CMY3	BD-50OHM	0	1	1	1	0	In	CMY3
F21	PG3	Power Related	-	-	-	-	-	-	-
F22	CMY2	BD-50OHM	0	1	1	1	0	In	CMY2
G1	PLL_AVD	PLL_AVD	-	-	-	-	-	-	-
G2	ADC_AVDD33	ADC_AVDD33	-	-	-	-	-	-	-
G3	ADC_IN6	INA	0	1	-	-	-	ADC	ADC_IN6
G4	ADC_IN7	INA	0	1	-	-	-	ADC	ADC_IN7
G19	CMY6	BD-50OHM	1	0	1	1	0	In	CMY6
G20	PG1	Power Related	-	-	-	-	-	-	-
G21	CMY0	BD-50OHM	0	1	1	1	0	In	CMY0
G22	CMCBCR7	BD-50OHM	0	1	1	1	0	In	CMCBCR7
H1	PG1	Power Related	-	-	-	-	-	-	-
H2	PG3	Power Related	-	-	-	-	-	-	-
H3	ADC_IN0	INA	0	1	-	-	-	ADC	ADC_IN0
H4	ADC_IN10	INA	0	1	-	-	-	ADC	ADC_IN10
H19	CMY4	BD-50OHM	0	1	1	1	0	In	CMY4
H20	CMHSYNC	BD-50OHM	0	1	1	1	0	In	CMHSYNC
H21	CMHDISP	BD-50OHM	0	1	1	1	0	In	CMHDISP
H22	CMCBCR3	BD-50OHM	1	0	1	1	0	In	CMCBCR3
J1	PG1	Power Related	-	-	-	-	-	-	-
J2	PNLGPP0	BD-50OHM	1	0	1	1	0	In	TSM_GTMS
J3	D0VSYNC	BD-50OHM	0	1	1	1	0	In	GPIO Input
J4	PNLGPP7	BD-50OHM	0	1	1	1	0	In	GPIO Input
J9	PG2	Power Related	-	-	-	-	-	-	-
J10	PG4	Power Related	-	-	-	-	-	-	-
J11	PG2	Power Related	-	-	-	-	-	-	-
J12	PG2	Power Related	-	-	-	-	-	-	-
J13	PG4	Power Related	-	-	-	-	-	-	-
J14	PG2	Power Related	-	-	-	-	-	-	-
J19	CMFODD	BD-50OHM	1	0	1	1	0	In	CMFODD

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
J20	CMCBCR5	BD-50OHM	0	1	1	1	0	In	CMCBCR5
J21	CMCBCR6	BD-50OHM	0	1	1	1	0	In	CMCBCR6
J22	CMCBCR4	BD-50OHM	0	1	1	1	0	In	CMCBCR4
K1	XTAL10M_OUT	OSC10M	-	-	-	-	-	Out	-
K2	XTAL10M_IN	OSC10M	-	-	-	-	-	In	-
K3	PNLGPP3	BD-50OHM	1	0	1	1	0	In	TSM_GTRST
K4	D0HDISP	BD-50OHM	0	1	1	1	0	In	GPIO Input
K9	PG4	Power Related	-	-	-	-	-	-	-
K10	PG4	Power Related	-	-	-	-	-	-	-
K11	PG4	Power Related	-	-	-	-	-	-	-
K12	PG4	Power Related	-	-	-	-	-	-	-
K13	PG4	Power Related	-	-	-	-	-	-	-
K14	PG4	Power Related	-	-	-	-	-	-	-
K19	CMCLK	BD-50OHM	0	1	1	1	1	In	CMCLK
K20	CMCBCR1	BD-50OHM	1	0	1	1	0	In	CMCBCR1
K21	PG3	Power Related	-	-	-	-	-	-	-
K22	CMCBCR0	BD-50OHM	0	1	1	1	0	In	CMCBCR0
L1	XTAL32K_OUT	OSC32K	-	-	-	-	-	Out	-
L2	XTAL32K_IN	OSC32K	-	-	-	-	-	In	-
L3	D0HSYNC	BD-50OHM	0	1	1	1	0	In	GPIO Input
L4	PNLGPP2	BD-50OHM	0	1	1	1	0	In	TSM_GTCK
L9	PG2	Power Related	-	-	-	-	-	-	-
L10	PG2	Power Related	-	-	-	-	-	-	-
L11	PG4	Power Related	-	-	-	-	-	-	-
L12	PG4	Power Related	-	-	-	-	-	-	-
L13	PG4	Power Related	-	-	-	-	-	-	-
L14	PG2	Power Related	-	-	-	-	-	-	-
L19	CMCBCR2	BD-50OHM	0	1	1	1	0	In	CMCBCR2
L20	PG1	Power Related	-	-	-	-	-	-	-
L21	DDR_DQS3	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
L22	DDR_DQ31	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
M1	PNLGPP1	BD-50OHM	1	0	1	1	0	In	TSM_GTDI
M2	PG3	Power Related	-	-	-	-	-	-	-
M3	PG1	Power Related	-	-	-	-	-	-	-
M4	D0DOTCLK	BD-50OHM	0	1	1	1	0	In	GPIO Input
M9	PG2	Power Related	-	-	-	-	-	-	-
M10	PG4	Power Related	-	-	-	-	-	-	-
M11	PG4	Power Related	-	-	-	-	-	-	-
M12	PG4	Power Related	-	-	-	-	-	-	-
M13	PG2	Power Related	-	-	-	-	-	-	-
M14	PG2	Power Related	-	-	-	-	-	-	-
M19	DDR_DQ29	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
M20	DDR_DM3	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
M21	PG6	Power Related	-	-	-	-	-	-	-
M22	DDR_DQ27	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
N1	D0RGB7	BD-50OHM	0	1	1	1	0	In	GPIO Input
N2	D0RGB2	BD-50OHM	0	1	1	1	0	In	GPIO Input
N3	D0RGB5	BD-50OHM	0	1	1	1	0	In	GPIO Input
N4	D0RGB3	BD-50OHM	0	1	1	1	0	In	GPIO Input
N9	PG4	Power Related	-	-	-	-	-	-	-
N10	PG4	Power Related	-	-	-	-	-	-	-
N11	PG4	Power Related	-	-	-	-	-	-	-
N12	PG4	Power Related	-	-	-	-	-	-	-
N13	PG4	Power Related	-	-	-	-	-	-	-

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
N14	PG4	Power Related	-	-	-	-	-	-	-
N19	DDR_DQ25	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
N20	PG1	Power Related	-	-	-	-	-	-	-
N21	DDR_DQ30	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
N22	DDR_DQ28	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
P1	D0RGB6	BD-50OHM	0	1	1	1	0	In	GPIO Input
P2	DOTCLKIN	BD-50OHM	1	0	1	1	1	In	GPIO Input
P3	D0RGB4	BD-50OHM	0	1	1	1	0	In	GPIO Input
P4	PNLGPP5	BD-50OHM	0	1	1	1	0	In	GPIO Input
P9	PG2	Power Related	-	-	-	-	-	-	-
P10	PG4	Power Related	-	-	-	-	-	-	-
P11	PG2	Power Related	-	-	-	-	-	-	-
P12	PG2	Power Related	-	-	-	-	-	-	-
P13	PG4	Power Related	-	-	-	-	-	-	-
P14	PG2	Power Related	-	-	-	-	-	-	-
P19	DDR_DQ23	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
P20	DDR_DQS2	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
P21	DDR_DQ24	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
P22	DDR_DQ26	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
R1	D0RGB0	BD-50OHM	0	1	1	1	0	In	GPIO Input
R2	PNLGPP6	BD-50OHM	0	1	1	1	0	In	GPIO Input
R3	D0RGB16	BD-50OHM	0	1	1	1	0	In	GPIO Input
R4	D0RGB8	BD-50OHM	0	1	1	1	0	In	GPIO Input
R19	DDR_DQ22	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
R20	DDR_DQ19	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
R21	DDR_DM2	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
R22	DDR_DQ21	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
T1	PNLGPP4	BD-50OHM	0	1	1	1	0	In	GPIO Input
T2	D0RGB9	BD-50OHM	0	1	1	1	0	In	GPIO Input
T3	PG1	Power Related	-	-	-	-	-	-	-
T4	D0RGB10	BD-50OHM	0	1	1	1	0	In	GPIO Input
T19	DDR_DQ16	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
T20	PG1	Power Related	-	-	-	-	-	-	-
T21	PG6	Power Related	-	-	-	-	-	-	-
T22	DDR_DQ20	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
U1	D0RGB17	BD-50OHM	0	1	1	1	0	In	GPIO Input
U2	PG3	Power Related	-	-	-	-	-	-	-
U3	D0RGB1	BD-50OHM	0	1	1	1	0	In	GPIO Input
U4	D0RGB11	BD-50OHM	0	1	1	1	0	In	GPIO Input
U19	DDR_A11	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
U20	DDR_A13	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
U21	DDR_DQ18	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
U22	DDR_DQ17	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
V1	D0RGB14	BD-50OHM	0	1	1	1	0	In	GPIO Input
V2	D0RGB12	BD-50OHM	0	1	1	1	0	In	GPIO Input
V3	D0RGB13	BD-50OHM	0	1	1	1	0	In	GPIO Input
V4	D0RGB18	BD-50OHM	0	1	1	1	0	In	GPIO Input
V19	DDR_A5	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
V20	DDR_A9	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
V21	DDR_A10	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
V22	DDR_A12	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W1	D0RGB15	BD-50OHM	0	1	1	1	0	In	TSM_TPC0_GTDO
W2	D0RGB19	BD-50OHM	0	1	1	1	0	In	GPIO Input
W3	D0RGB21	BD-50OHM	0	1	1	1	0	In	GPIO Input

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
W4	D0RGB23	BD-50OHM	0	1	1	1	0	In	GPIO Input
W5	D1VSYNC	BD-50OHM	0	1	1	1	0	In	GPIO Input
W6	D1RGB2	BD-50OHM	0	1	1	1	0	In	GPIO Input
W7	D1RGB5	BD-50OHM	0	1	1	1	0	In	GPIO Input
W8	D1RGB12	BD-50OHM	0	1	1	1	0	In	GPIO Input
W9	D1RGB13	BD-50OHM	0	1	1	1	0	In	GPIO Input
W10	D1RGB17	BD-50OHM	0	1	1	1	0	In	GPIO Input
W11	D1RGB21	BD-50OHM	0	1	1	1	0	In	GPIO Input
W12	DDR_DQ1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W13	DDR_DQ6	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W14	DDR_DQ9	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W15	DDR_DQ13	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W16	DDR_DQS1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W17	DDR_CAS	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W18	DDR_A0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W19	DDR_A1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W20	DDR_A4	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W21	DDR_A7	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
W22	DDR_A8	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
Y1	D0RGB20	BD-50OHM	0	1	1	1	0	In	GPIO Input
Y2	D0RGB22	BD-50OHM	0	1	1	1	0	In	GPIO Input
Y3	D1HSYNC	BD-50OHM	0	1	1	1	0	In	GPIO Input
Y4	D1DOTCLK	BD-50OHM	0	1	1	1	0	In	GPIO Input
Y5	PG1	Power Related	-	-	-	-	-	-	-
Y6	D1RGB6	BD-50OHM	0	1	1	1	0	In	GPIO Input
Y7	D1RGB10	BD-50OHM	0	1	1	1	0	In	GPIO Input
Y8	MLBCLK	IN	0	1	-	-	1	-	Dedicated
Y9	PG1	Power Related	-	-	-	-	-	-	-
Y10	D1RGB18	BD-50OHM	0	1	1	1	0	In	GPIO Input
Y11	D1RGB23	BD-50OHM	0	1	1	1	0	In	GPIO Input
Y12	DDR_DQ2	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
Y13	PG1	Power Related	-	-	-	-	-	-	-
Y14	DDR_DQS0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
Y15	DDR_DQ10	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
Y16	PG1	Power Related	-	-	-	-	-	-	-
Y17	DDR_WE	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
Y18	DDR_CS	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
Y19	PG1	Power Related	-	-	-	-	-	-	-
Y20	DDR_CKN	BD-37.5OHM	0	1	0	0	0	In	Dedicated
Y21	DDR_A3	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
Y22	DDR_A6	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA1	D1HDISP	BD-50OHM	0	1	1	1	0	In	GPIO Input
AA2	PG3	Power Related	-	-	-	-	-	-	-
AA3	D1RGB0	BD-50OHM	0	1	1	1	0	In	GPIO Input
AA4	PG3	Power Related	-	-	-	-	-	-	-
AA5	D1RGB7	BD-50OHM	0	1	1	1	0	In	GPIO Input
AA6	D1RGB9	BD-50OHM	0	1	1	1	0	In	GPIO Input
AA7	MLBDAT_IO	BD-50OHM	0	1	1	1	0	In	Dedicated
AA8	PG3	Power Related	-	-	-	-	-	-	-
AA9	D1RGB15	BD-50OHM	0	1	1	1	0	In	GPIO Input
AA10	D1RGB19	BD-50OHM	0	1	1	1	0	In	GPIO Input
AA11	D1RGB22	BD-50OHM	1	0	1	1	0	In	GPIO Input
AA12	PG5	Power Related	-	-	-	-	-	-	-
AA13	DDR_DQ5	BD-37.5OHM	0	1	0	0	0	In	GPIO Input

Pin number	Signal name	Comment	PU	PD	IMP1	IMP0	SMT	DIR	Default MUX
AA14	DDR_DQ7	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA15	PG5	Power Related	-	-	-	-	-	-	-
AA16	DDR_DQ12	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA17	DDR_DQ15	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA18	PG5	Power Related	-	-	-	-	-	-	-
AA19	DDR_BA0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AA20	DDR_CK	BD-37.5OHM	0	1	0	0	0	In	Dedicated
AA21	PG5	Power Related	-	-	-	-	-	-	-
AA22	DDR_A2	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB1	PG1	Power Related	-	-	-	-	-	-	-
AB2	D1RGB1	BD-50OHM	1	0	1	1	0	In	GPIO Input
AB3	D1RGB3	BD-50OHM	0	1	1	1	0	In	GPIO Input
AB4	D1RGB4	BD-50OHM	0	1	1	1	0	In	GPIO Input
AB5	D1RGB8	BD-50OHM	0	1	1	1	0	In	GPIO Input
AB6	D1RGB11	BD-50OHM	0	1	1	1	0	In	GPIO Input
AB7	MLBSIG_IO	BD-50OHM	0	1	1	1	0	In	Dedicated
AB8	D1RGB14	BD-50OHM	0	1	1	1	0	In	GPIO Input
AB9	D1RGB16	BD-50OHM	0	1	1	1	0	In	GPIO Input
AB10	D1RGB20	BD-50OHM	0	1	1	1	0	In	GPIO Input
AB11	DDR_DQ0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB12	DDR_DQ3	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB13	DDR_DQ4	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB14	DDR_DM0	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB15	DDR_DQ8	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB16	DDR_DQ11	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB17	DDR_DQ14	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB18	DDR_DM1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB19	DDR_RAS	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB20	DDR_CKE	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB21	DDR_BA1	BD-37.5OHM	0	1	0	0	0	In	GPIO Input
AB22	PG1	Power Related	-	-	-	-	-	-	-

Note1: The pin E9 (CS) has to be shorted to pin E8 (SIP_QSPI_CS) in TMPR462 / TMPR463;
In TMPR461, these pins may be N.C. or shorted together.

Note2: The pin E15 (SCLK) has to be shorted to pin E14 (SIP_QSPI_SCLK) in TMPR462 / TMPR463;
In TMPR461, these pins may be N.C. or shorted together.

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