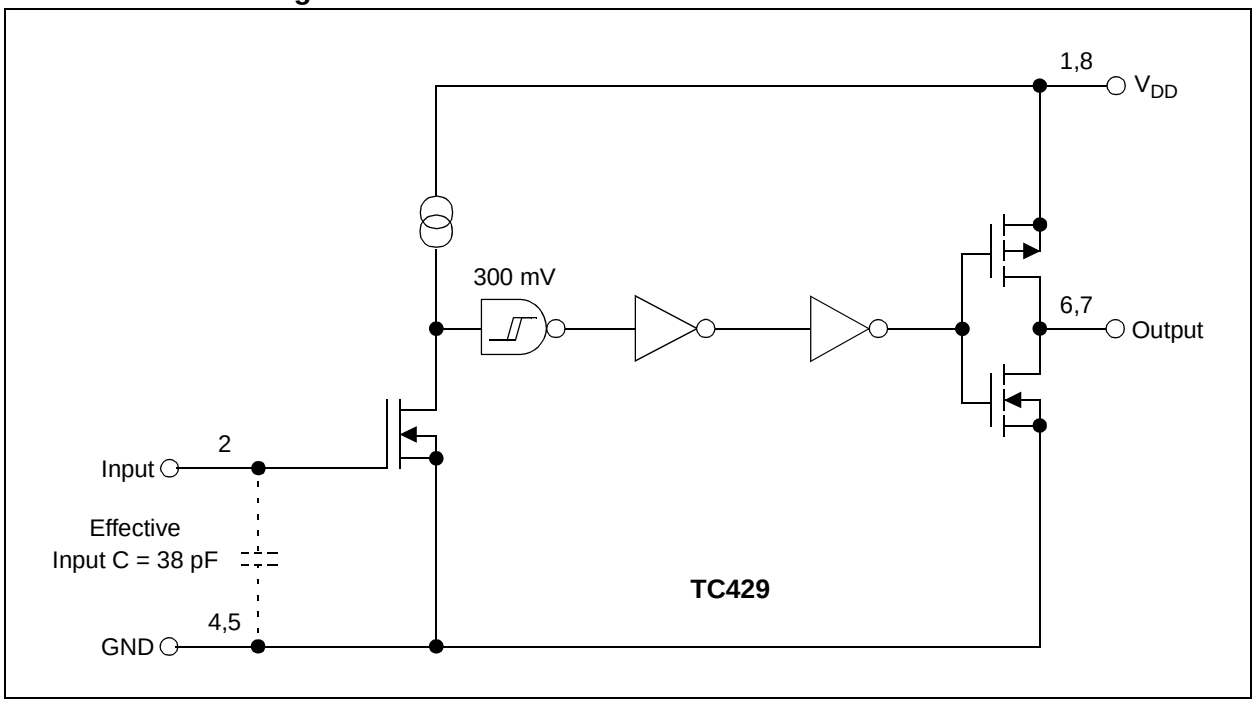
Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... +20V

Input Voltage, Any Terminal
..... V_{DD} + 0.3V to GND – 0.3V

Power Dissipation ($T_A \leq 70°C$)
PDIP ..... 730 mW
CERDIP ..... 800 mW
SOIC ..... 470 mW

Storage Temperature Range ..... -65°C to +150°C

Maximum Junction Temperature, T_J ..... +150°C

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Symbol	Description
V_{DD}	Supply input, 7V to 18V
INPUT	Control input. TTL/CMOS compatible logic input
NC	No connection
GND	Ground
GND	Ground
$\overline{\text{OUTPUT}}$	CMOS push-pull, common to pin 7
$\overline{\text{OUTPUT}}$	CMOS push-pull, common to pin 6
V_{DD}	Supply input, 7V to 18V

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C with 7V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	1.8	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Current	I_{IN}	-10	—	10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance	R_O	—	1.8	2.5	Ω	V_{IN} = 0.8V, V_{OUT} = 10 mA, V_{DD} = 18V
		—	1.5	2.5		V_{IN} = 2.4V, V_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	6.0	—	A	V_{DD} = 18V, **Figure 4-4**
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	0.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µsec, V_{DD} = 16V
Switching Time (Note 1)						
Rise Time	t_R	—	23	35	nsec	C_L = 2500 pF, **Figure 4-1**
Fall Time	t_F	—	25	35	nsec	C_L = 2500 pF, **Figure 4-1**
Delay Time	t_{D1}	—	53	75	nsec	**Figure 4-1**
Delay Time	t_{D2}	—	60	75	nsec	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	—	3.5	5.0	mA	V_{IN} = 3V
		—	0.3	0.5		V_{IN} = 0V

Note 1: Switching times ensured by design.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, over operating temperature range with 7V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-10	—	10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance	R_O	—	—	5.0	Ω	V_{IN} = 0.8V, V_{OUT} = 10 mA, V_{DD} = 18V
		—	—	5.0		V_{IN} = 2.4V, V_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	—	70	nsec	C_L = 2500 pF, **Figure 4-1**
Fall Time	t_F	—	—	70	nsec	C_L = 2500 pF, **Figure 4-1**
Delay Time	t_{D1}	—	—	100	nsec	**Figure 4-1**
Delay Time	t_{D2}	—	—	120	nsec	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	—	—	12	mA	V_{IN} = 3V
		—	—	1.0		V_{IN} = 0V

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C with 7V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (C)	T_A	0	—	+70	ºC	
Specified Temperature Range (E)	T_A	-40	—	+85	ºC	
Specified Temperature Range (M)	T_A	-55	—	+125	ºC	
Maximum Junction Temperature	T_J	—	—	+150	ºC	
Storage Temperature Range	T_A	-65	—	+150	ºC	
Package Thermal Resistances						
Thermal Resistance, 8L-CERDIP	θ_{JA}	—	150	—	ºC/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	125	—	ºC/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	155	—	ºC/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 7V ≤ V_{DD} ≤ 18V.

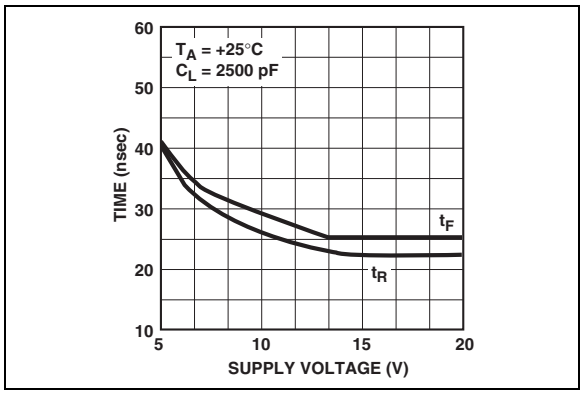


FIGURE 2-1: *Rise/Fall Times vs. Supply Voltage.*

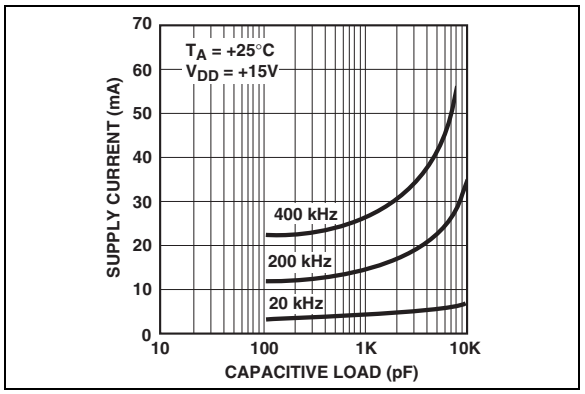


FIGURE 2-4: *Supply Current vs. Capacitive Load.*

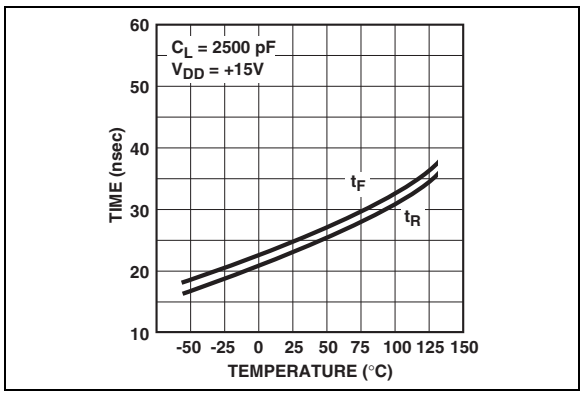


FIGURE 2-2: *Rise/Fall Times vs. Temperature.*

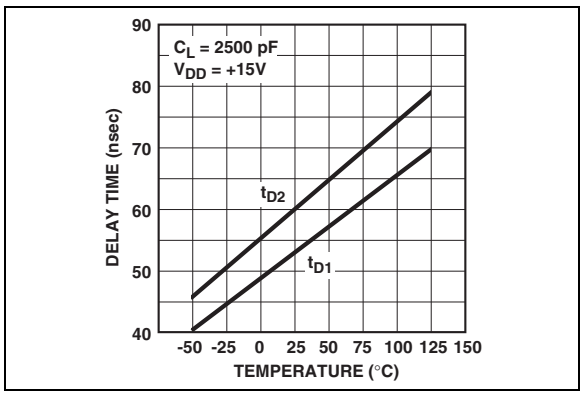


FIGURE 2-5: *Delay Times vs. Temperature.*

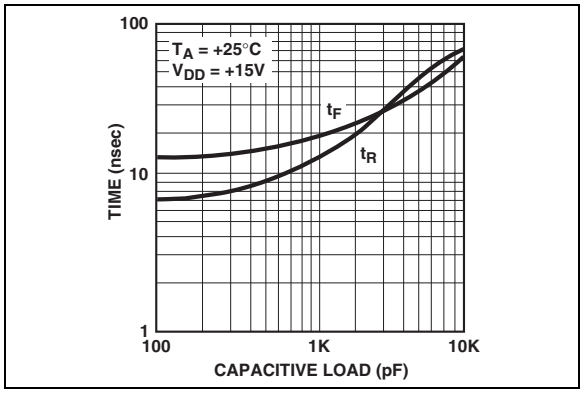


FIGURE 2-3: *Rise/Fall Times vs. Capacitive Load.*

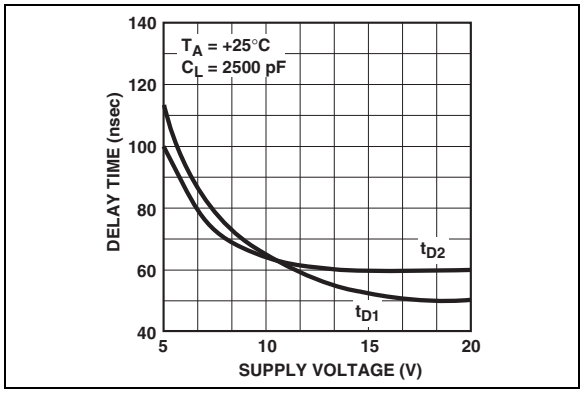


FIGURE 2-6: *Delay Times vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 7V ≤ V_{DD} ≤ 18V.

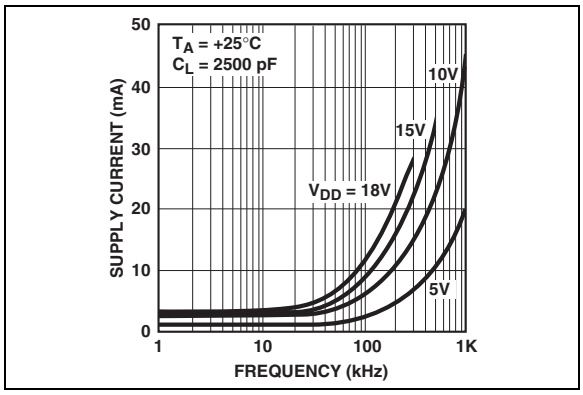


FIGURE 2-7: *Supply Current vs. Frequency.*

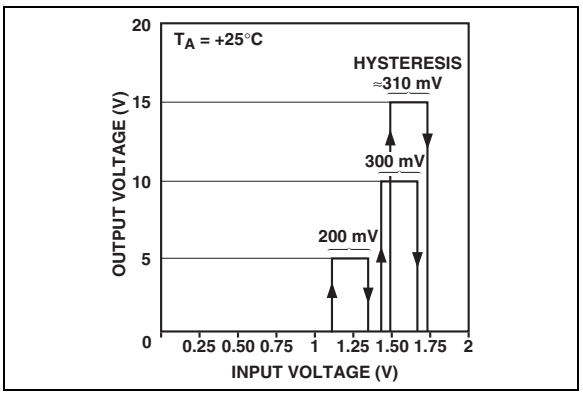


FIGURE 2-10: *Voltage Transfer Characterstics.*

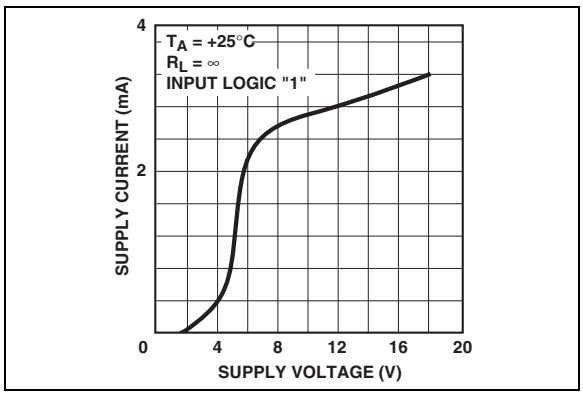


FIGURE 2-8: *Supply Current vs. Supply Voltage.*

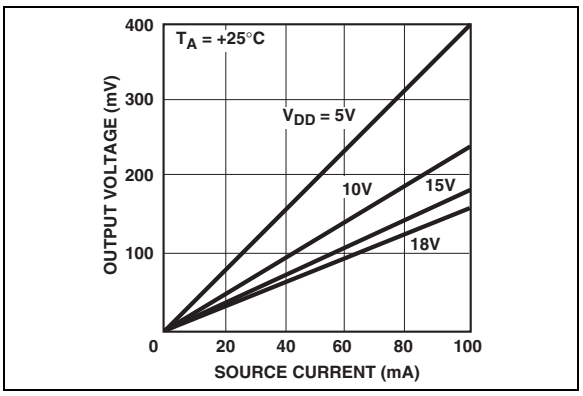


FIGURE 2-11: *High Output Voltage (V_{DD}-V_{OH}) vs. Output Source Current.*

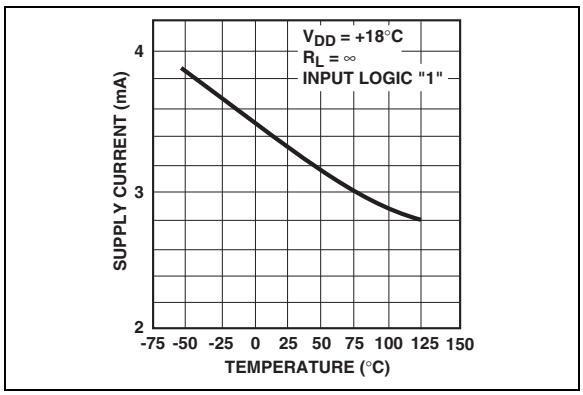


FIGURE 2-9: *Supply Current vs. Temperature.*

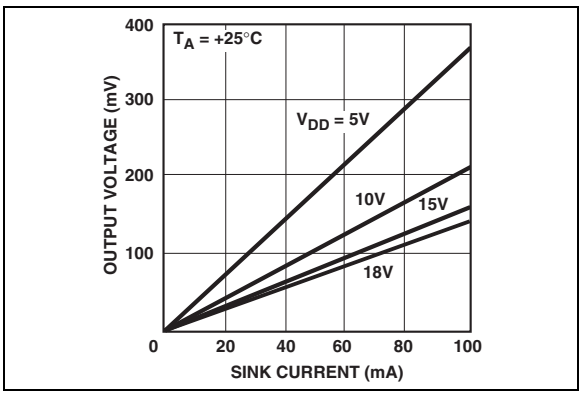


FIGURE 2-12: *Low Output Voltage vs. Output Sink Current.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Symbol	Description
1	V_{DD}	Supply input, 7V to 18V
2	INPUT	Control input. TTL/CMOS compatible logic input
3	NC	No connection
4	GND	Ground
5	GND	Ground
6	$\overline{\text{OUTPUT}}$	CMOS push-pull output, common to pin 7
7	$\overline{\text{OUTPUT}}$	CMOS push-pull output, common to pin 6
8	V_{DD}	Supply input, 7V to 18V

3.1 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 7.0V to 18V with respect to the ground pin. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A value of 1.0 µF is suggested.

3.2 Control Input (INPUT)

The MOSFET driver input is a high-impedance, TTL/CMOS compatible input. The input also has 300 mV of hysteresis between the high and low thresholds that prevents output glitching even when the rise and fall time of the input signal is very slow.

3.3 CMOS Push-Pull Output (OUTPUT)

The MOSFET driver output is a low-impedance, CMOS push-pull style output, capable of driving a capacitive load with 6.0A peak currents.

3.4 Ground (GND)

The ground pins are the return path for the bias current and for the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

3.5 No Connect (NC)

No connection.

4.0 APPLICATIONS INFORMATION

4.1 Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500 pF load to 18V in 25 nsec requires a 1.8A current from the device's power supply.

To ensure low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (< 0.5 in.) should be used. A 1 µF film capacitor in parallel with one or two 0.1 µF ceramic disk capacitors normally provides adequate bypassing.

4.2 Grounding

The high-current capability of the TC429 demands careful PC board layout for best performance. Since the TC429 is an inverting driver, any ground lead impedance will appear as negative feedback that can degrade switching speed. The feedback is especially noticeable with slow rise-time inputs, such as those produced by an open-collector output with resistor pull-up. The TC429 input structure includes about 300 mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 4-3 shows the feedback effect in detail. As the TC429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. A PC trace resistance of as little as 0.05Ω can produce hundreds of millivolts at the TC429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillations may result.

To ensure optimum device performance, separate ground traces should be provided for the logic and power connections. Connecting logic ground directly to the TC429 GND pins ensures full logic drive to the input and fast output switching. Both GND pins should be connected to power ground.

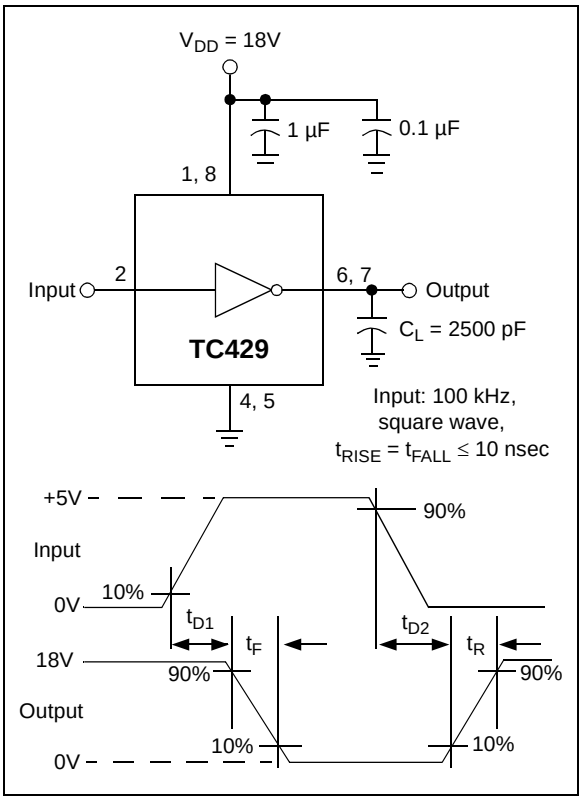


FIGURE 4-1: *Inverting Driver Switching Time Test Circuit.*

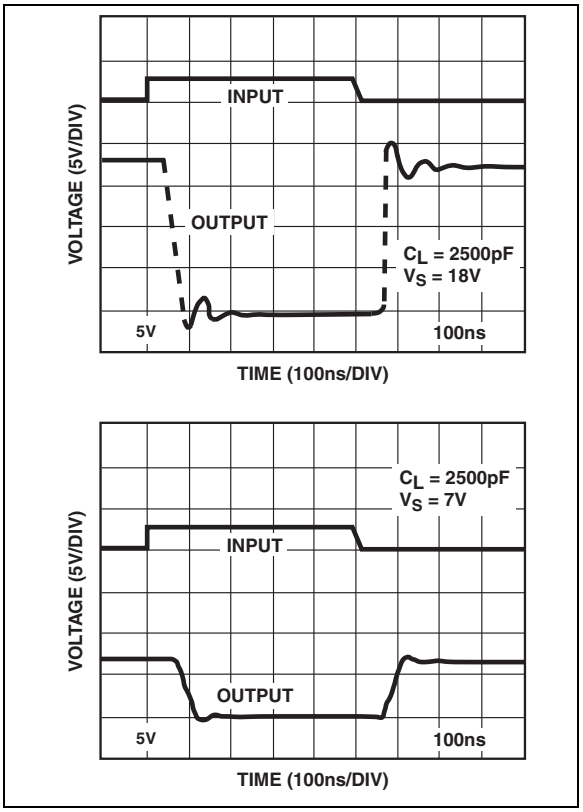


FIGURE 4-2: *Switching Speed.*

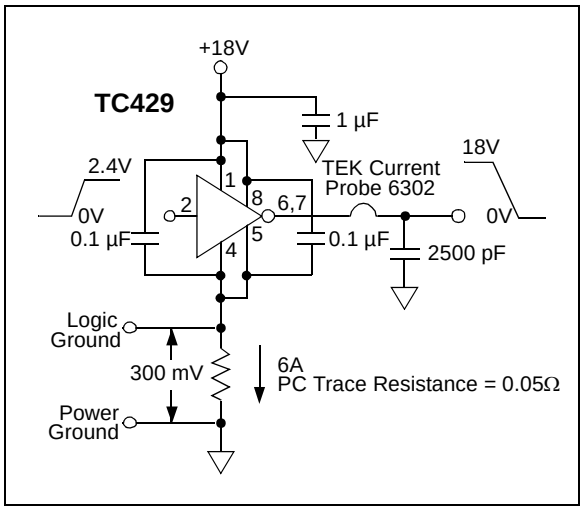


FIGURE 4-3: *Switching Time Degradation Due To Negative Feedback.*

4.3 Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 3 mA current source load. With a logic '1' input, the maximum quiescent supply current is 5 mA. Logic '0' input level signals reduce quiescent current to 500 µA maximum.

The TC429 input is designed to provide 300 mV of hysteresis, providing clean transitions and minimizing output stage current spiking when changing states. Input voltage levels are approximately 1.5V, making the device TTL-compatible over the 7V to 18V operating supply range. Input pin current draw is less than 10 µA over this range.

The TC429 can be directly driven by TL494, SG1526/1527, SG1524, SE5560 or similar switch-mode power supply integrated circuits. By off-loading the power-driving duties to the TC429, the power supply controller can operate at lower dissipation, improving performance and reliability.

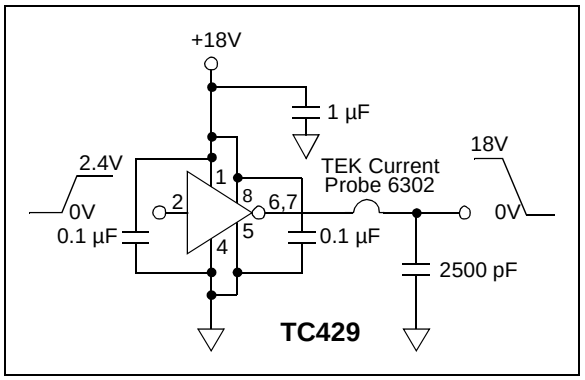


FIGURE 4-4: *Peak Output Current Test Circuit.*

4.4 Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as the 4000 and 74C have outputs that can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The TC429, however, can source or sink several amperes and drive large capacitive loads at high frequency. Since the package power dissipation limit can easily be exceeded, some attention should be given to power dissipation when driving low-impedance loads and/or operating at high frequency.

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. Table 4-1 lists the maximum operating frequency for several power supply voltages when driving a 2500 pF load. More accurate power dissipation figures can be obtained by summing the three components that make up the total device power dissipation.

Input signal duty cycle, power supply voltage and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operation temperature is easily calculated. The 8-pin CERDIP junction-to-ambient thermal resistance is 150°C/W. At +25°C, the package is rated at 800 mW maximum dissipation. Maximum allowable junction temperature is +150°C.

Three components make up total package power dissipation:

- Capacitive load dissipation (P_C)
- Quiescent power (P_Q)
- Transition power (P_T)

The capacitive load-caused dissipation is a direct function of frequency, capacitive load and supply voltage.

The device capacitive load dissipation is:

EQUATION

$$P_C = fCV_S^2$$

Where:

f = Switching frequency
C = Capacitive load
V_S = Supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low-power dissipation mode with only 0.5 mA total current drain. Logic-high signals raise the current to 5 mA maximum.

The quiescent power dissipation is:

EQUATION

$$P_Q = V_S(D(I_H) + (1-D)I_L)$$

Where:

I_H = Quiescent current with input high (5 mA max)
I_L = Quiescent current with input low (0.5 mA max)
D = Duty cycle

Transition power dissipation arises because the output stage N- and P-channel MOS transistors are ON simultaneously for a very short period when the output changes.

The device transition power dissipation is approximately:

EQUATION

$$P_T = fV_S(3.3 \times 10^{-9} A \bullet Sec)$$

An example shows the relative magnitude for each item.

C = 2500 pF
V_S = 15V
D = 50%
f = 200 kHz
P_D = Package power dissipation:
= $P_C + P_T + P_Q$
= 113 mW + 10 mW + 41 mW
= 164 mW

Maximum ambient operating temperature:
= $T_J - \theta_{JA}(P_D)$
= 150ºC - (150ºC/W)(0.164W)
= 125°C

Where:

T_J = Maximum allowable junction temperature (+150°C)
θ_{JA} = Junction-to-ambient thermal resistance (150°C/W, CERDIP)

Note: Ambient operating temperature should not exceed +85ºC for EPA or EOA devices or +125ºC for MJA devices.

TABLE 4-1: MAXIMUM OPERATING FREQUENCIES

V_S	f_{MAX}
18V	500 kHz
15V	700 kHz
10V	1.3 MHz
5V	>2 MHz

Conditions:

1. CERDIP Package (θ_{JA} =150°C/W)
2. T_A = +25°C
3. C_L = 2500 pF

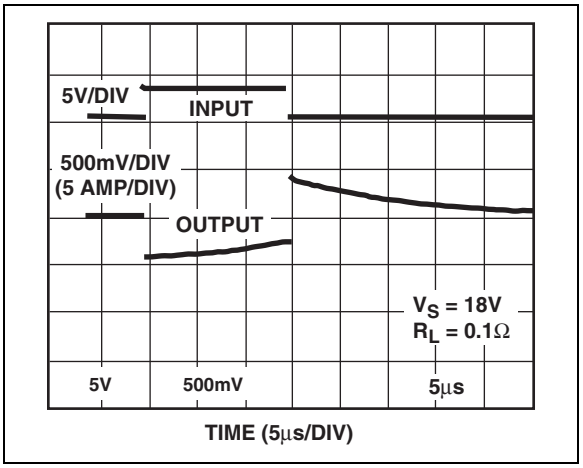


FIGURE 4-5: *Peak Output Current Capability.*

4.5 POWER-ON OSCILLATION

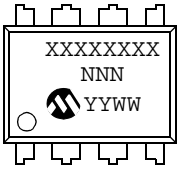
Note: It is extremely important that all MOSFET driver applications be evaluated for the possibility of having high-power oscillations occur during the power-on cycle.

Power-on oscillations are due to trace size, layout and component placement. A ‘quick fix’ for most applications that exhibit power-on oscillation problems is to place approximately 10 kΩ in series with the input of the MOSFET driver.

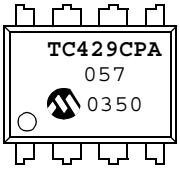
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

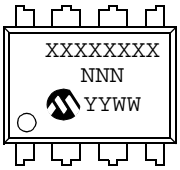
8-Lead PDIP (300 mil)



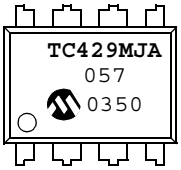
Example:



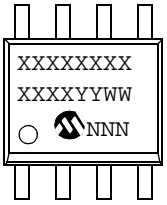
8-Lead CERDIP (300 mil)



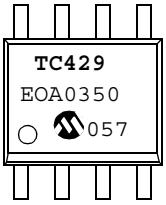
Example:



8-Lead SOIC (150 mil)



Example:

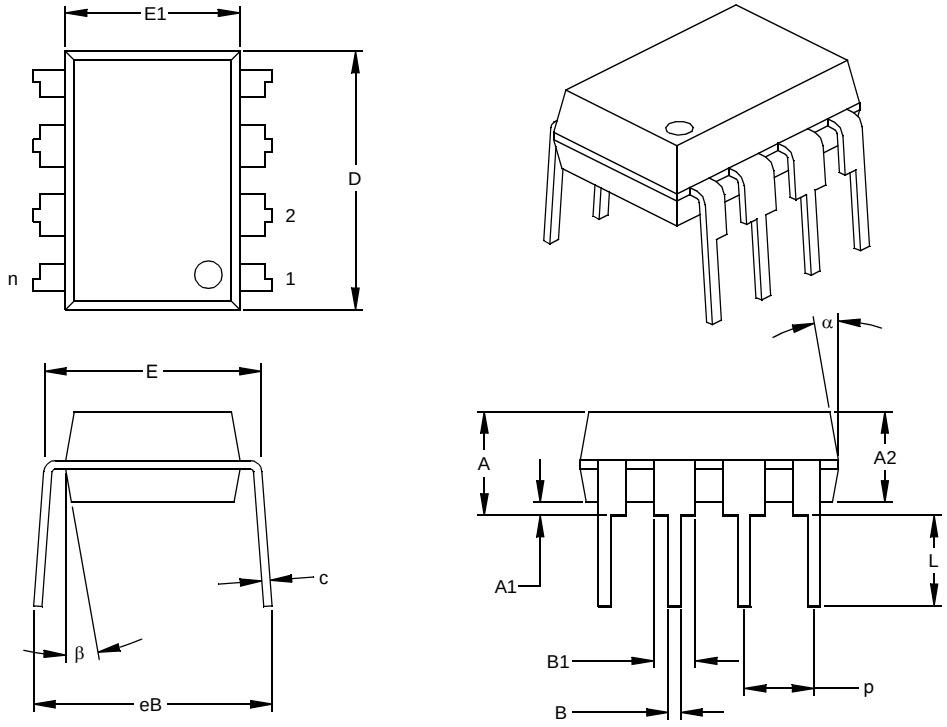


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-line (PA) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



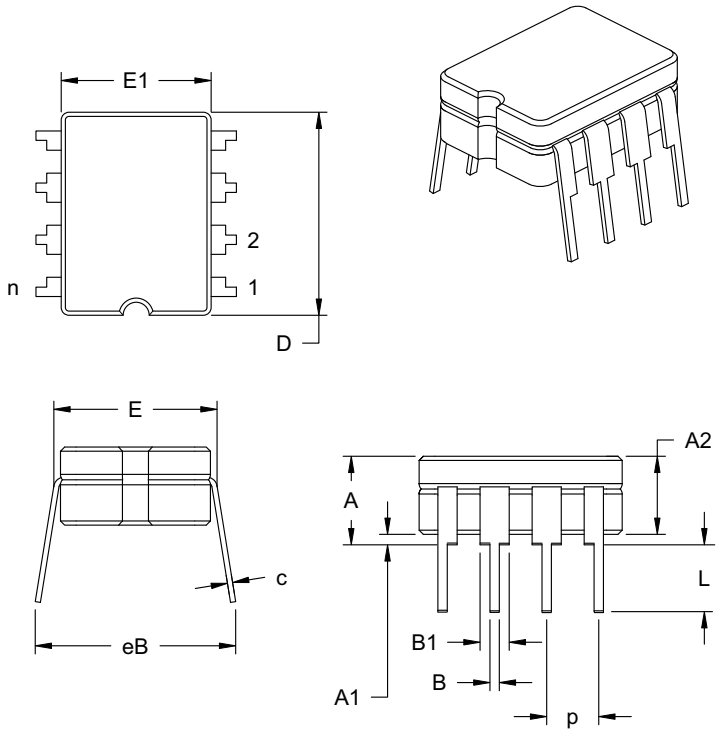
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	a	5	10	15	5	10	15
Mold Draft Angle Bottom	b	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Ceramic Dual In-line – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	B	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eB	.320	.360	.400	8.13	9.15	10.16

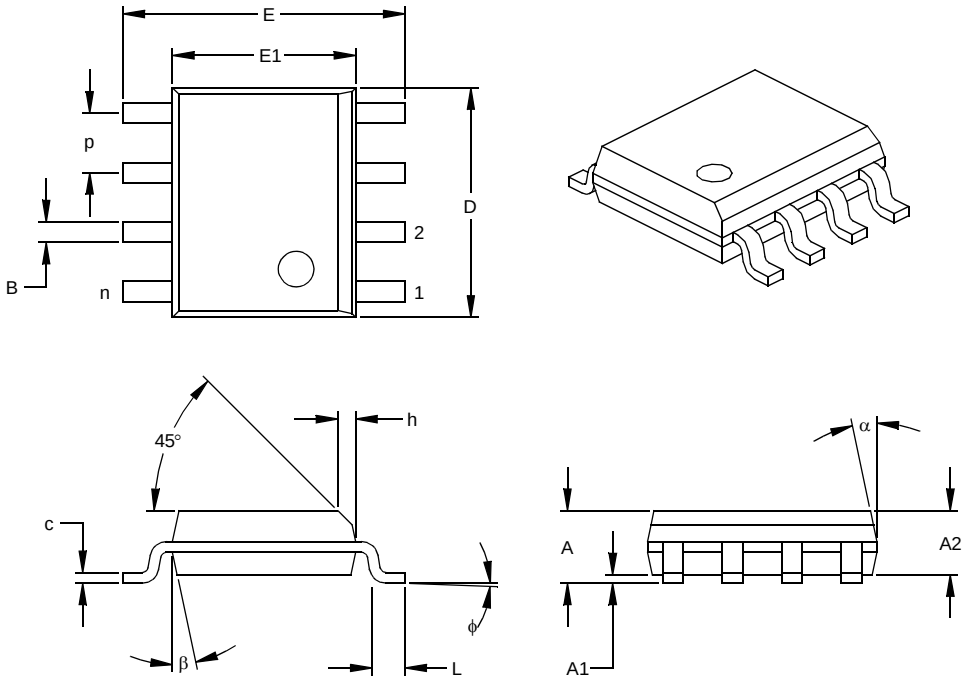
*Controlling Parameter

JEDEC Equivalent: MS-030

Drawing No. C04-010

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

6.0 REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	TC429:	6A Single MOSFET Driver
Temperature Range:	C =	0°C to +70°C
	E =	-40°C to +85°C
	M =	-55°C to +125°C (CERDIP only)
Package:	JA =	Plastic CERDIP, (300 mil Body), 8-lead
	OA =	Plastic SOIC, (150 mil Body), 8-lead *
	OA713 =	Plastic SOIC, (150 mil Body), 8-lead * (Tape and Reel)
	PA =	Plastic DIP (300 mil Body), 8-lead

* SOIC package offered in E-Temp only

Examples:

a) TC429CPA: 6A Single MOSFET driver, PDIP package, 0°C to +70°C.

b) TC429MJA: 6A Single MOSFET driver, CERDIP package, -55°C to +125°C.

c) TC429EPA: 6A Single MOSFET driver, PDIP package, -40°C to +85°C.

d) TC429EOA713: Tape and Reel, 6A Single MOSFET driver, SOIC package, -40°C to +85°C.

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2. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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