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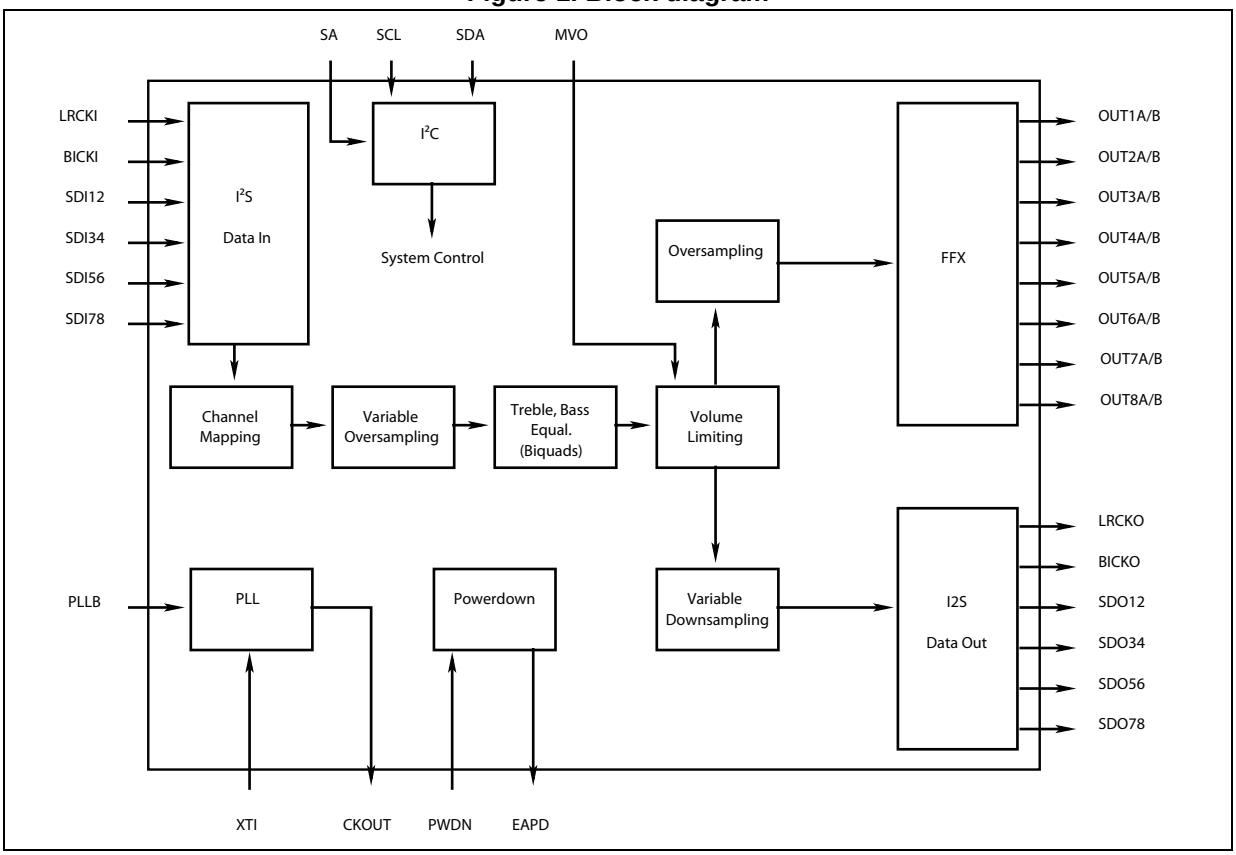
1 Description

The STA311B is a single-chip solution for digital audio processing and control in multichannel applications and provides output capabilities for FFX™ (full flexible amplification). In conjunction with an FFX™ power device, it provides high-quality, high-efficiency, all digital amplification. The device is extremely versatile, allowing for input of most digital formats including 6.1/7.1-channel and 192 kHz, 24-bit DVD-audio, DSD/SACD. In the 5.1 application the additional 2 channels can be used for audio line-out or headphone drive.

2 Device overview

2.1 Block diagram

Figure 1. Block diagram



2.2 Pin description

Figure 2. Pin connections VFQFPN-56 (top view)

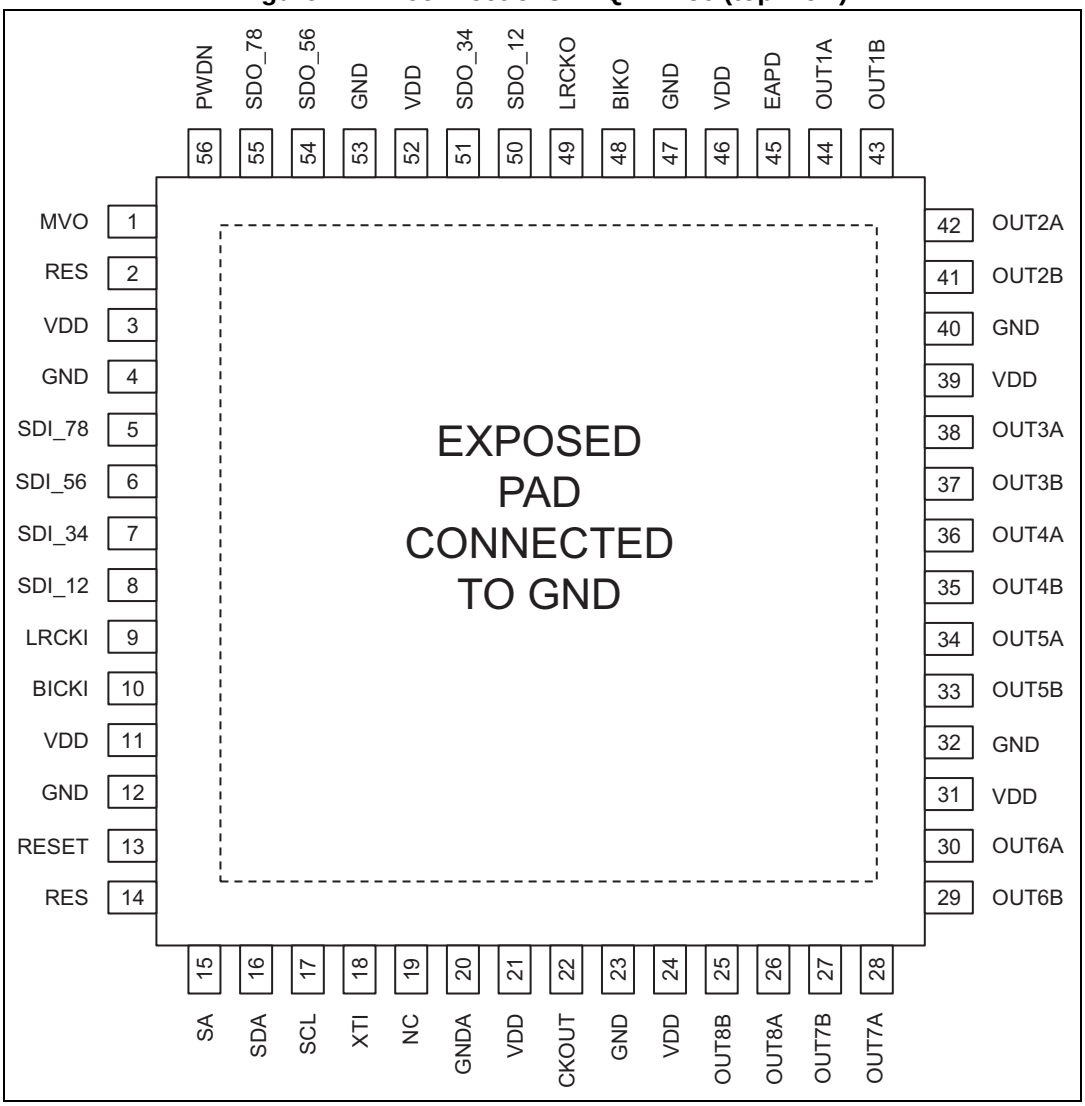


Table 2. Pin description

Pin	Type	Name	Description
1	5-V tolerant TTL input buffer	MVO/DSD_CLK	Master volume override/ DSD input clock
2	Reserved	RES	Connect to GND
5	5-V tolerant TTL input buffer	SDI_78/DSD_6	Input serial data channels 7 & 8/ DSD input channel 6
6	5-V tolerant TTL input buffer	SDI_56/DSD_5	Input serial data channels 5 & 6/ DSD input channel 5
7	5-V tolerant TTL input buffer	SDI_34/DSD_4	Input serial data channels 3 & 4/ DSD input channel 4
8	5-V tolerant TTL input buffer	SDI_12/DSD_3	Input serial data channels 1 & 2/ DSD input channel 3
9	5-V tolerant TTL input buffer	LRCKI/DSD_2	Input left/right clock/ DSD input channel 2
10	5-V tolerant TTL input buffer	BICKI/DSD_1	Input serial clock/ DSD input channel 1
18	5-V tolerant TTL Schmitt trigger input buffer	RESETN	Global reset
14	Reserved	RES	Connect to GND
15	1.8V CMOS input buffer with pull-down	SA	Select address (I²C)
16	Bidirectional buffer: 5-V tolerant TTL Schmitt trigger input; 3.3-V capable 2 mA slew-rate controlled output.	SDA	Serial data (I²C)
17	5-V tolerant TTL Schmitt trigger input buffer	SCL	Serial clock (I²C)
18	5-V tolerant TTL Schmitt trigger input buffer	XTI	Crystal oscillator input (clock input)
19	Not connected	NC	Reserved
20	Analog ground	GNDA	PLL ground
22	3.3-V capable TTL tristate 4 mA output buffer	CKOUT	Clock output
25	3.3-V capable TTL 2 mA output buffer	OUT8B	PWM channel 8 output B
26	3.3-V capable TTL 2 mA output buffer	OUT8A	PWM channel 8 output A
27	3.3-V capable TTL 2 mA output buffer	OUT7B	PWM channel 7 output B
28	3.3-V capable TTL 2 mA output buffer	OUT7A	PWM channel 7 output A
29	3.3-V capable TTL 2 mA output buffer	OUT6B	PWM channel 6 output B
30	3.3-V capable TTL 2 mA output buffer	OUT6A	PWM channel 6 output A
33	3.3-V capable TTL 2 mA output buffer	OUT5B	PWM channel 5 output B
34	3.3-V capable TTL 2 mA output buffer	OUT5A	PWM channel 5 output A
35	3.3-V capable TTL 2 mA output buffer	OUT4B	PWM channel 4 output B

Table 2. Pin description (continued)

Pin	Type	Name	Description
36	3.3-V capable TTL 2 mA output buffer	OUT4A	PWM channel 4 output A
37	3.3-V capable TTL 2 mA output buffer	OUT3B	PWM channel 3 output B
38	3.3-V capable TTL 2 mA output buffer	OUT3A	PWM channel 3 output A
41	3.3-V capable TTL 2 mA output buffer	OUT2B	PWM channel 2 output B
42	3.3-V capable TTL 2 mA output buffer	OUT2A	PWM channel 2 output A
43	3.3-V capable TTL 2 mA output buffer	OUT1B	PWM channel 1 output B
44	3.3-V capable TTL 2 mA output buffer	OUT1A	PWM channel 1 output A
45	3.3-V capable TTL 4 mA output buffer	EAPD	External amp power-down
48	3.3-V capable TTL 2 mA output buffer	BICKO	Output serial clock
49	3.3-V capable TTL 2 mA output buffer	LRCKO	Output left/right clock
50	3.3-V capable TTL 2 mA output buffer	SDO_12	Output serial data channels 1&2
51	3.3-V capable TTL 2 mA output buffer	SDO_34	Output serial data channels 3&4
54	3.3-V capable TTL 2 mA bidirectional buffer	SDO_56	Output serial data channels 5&6 External power bridge fault input
55	3.3-V capable TTL 2mA output buffer	SDO_78	Output serial data channels 7&8 External power bridge tristate signal (‘0’ = tristate)
56	5-V tolerant TTL Schmitt trigger input buffer	PWDN	Device power-down
3, 11,21,24, 31, 39, 46, 52	3.3-V digital supply voltage	VDD	3.3-V supply
4, 12, 23, 32, 40, 47, 53	Digital ground	GND	Ground

Master volume override (MVO)

This pin enables the user to bypass the volume control on all channels. When MVO is pulled high, the master volume register is set to 0x00, which corresponds to its full-scale setting. The master volume register setting offsets the individual channel volume settings, which default to 0 dB.

Serial data in (SDI_12, SDI_34, SDI_56, SDI_78)

Audio information enters the device here. Six format choices are available including I²S, left-justified or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

RESET

Driving this pin low turns off the outputs and returns all settings to their defaults.

I²C bus

The SA, SDA and SCL pins operate per the Phillips I²C specification. See *Section 7: I²C bus operation on page 23*.

Phase-locked loop (PLL)

The phase-locked loop section provides the system timing signals and CKOUT.

Clock output (CKOUT)

System synchronization and master clocks are provided by CKOUT.

PWM outputs (OUT1 through OUT8)

The PWM outputs provide the input signal for the power devices.

External amplifier power-down (EAPD)

This signal can be used to control the power-down of the FFX power devices.

Serial data out (SDO_12, SDO_34, SDO_56, SDO_78)

When the pop-noise removal feature is disabled, these are the outputs for the audio information. Six different formats are available including I²S, left-or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

However, when the pop-noise removal feature is enabled, SDO_12 and SDO_34 output the audio information, whereas SDO_56 is used as the external power bridge fault input and SDO_78 as the external power bridge tristate signal.

Device power-down (PWDN)

Pulling PWDN low begins the power-down sequence which puts the STA311B into a low-power state. EAPD goes low approximately 30 ms later.

Frequency sampling autodetection

The system clock is generated by PLL using XTI or BICKI input, and the ratio (IR) between the frequency sampling (Fs) of the audio serial and the PLL clock has to be set in the appropriate registers via the I²C interface. If the Fs autodetection function has been enabled, the IR parameter will be set automatically based on the Fs input (see *Fs autodetection on page 32*).

3 Electrical characteristics

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	3.3-V I/O power supply	-0.5		4	V
V_i	Voltage on input pins	-0.5		VDD + 0.5	V
V_o	Voltage on output pins	-0.5		VDD + 0.3	V
VSA	Voltage on SA pin 15	-0.5		2.0	V
T_{stg}	Storage temperature	-40		150	°C
T_{amb}	Ambient operating temperature	-40		90	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj\text{-}amb}$	Thermal resistance, junction to ambient		85		°C/W

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	I/O power supply	3.0	3.3	3.6	V
VSA	Voltage on SA pin 15	0.0	1.8	1.95	V
T_j	Operating junction temperature	-40	25	125	°C

3.4 Electrical specifications

The following specifications are valid for V_{DD} =3.3 V ± 0.3 V, VSA=0V and T_{amb} = 25 °C, unless otherwise stated.

Table 6. General interface electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low-level input, no pull-up	V_i = 0 V			1	µA
I_{ih}	High-level input, no pull-down	$V_i = V_{DD}$			2	µA
I_{OZ}	Tristate output leakage without pull-up/down	$V_i = V_{DD}$			2	µA
V_{esd}	Electrostatic protection (human body model)	Leakage < 1 µA	2000			V

Table 7. DC electrical characteristics: 3.3-V buffers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
V_{ILhyst}	Low-level threshold	Input falling	0.8		1.35	V
V_{IHhyst}	High-level threshold	Input rising	1.3		2.0	V
V_{hyst}	Schmitt trigger hysteresis		0.3		0.8	V
V_{ol}	Low-level output	I_{ol} = 100 µA			0.2	V
V_{oh}	High-level output	I_{oh} = -100 µA	VDD-0.2			V
		I_{oh} = -2 mA	2.4			V
Idd	Quiescent current	Reset conditions		15		mA
		Normal conditions with CKOUT		60		mA
f_{CKOUT}		Reset=1 PWDN=1		2.85		MHz

4 Serial audio interface

The STA311B audio serial input interfaces with standard digital audio components and accepts a number of serial data formats. The STA311B always acts as a slave when receiving audio input from standard digital audio components. Serial data for eight channels is provided using 6 input pins: left/right clock LRCKI, serial clock BICKI, serial data 1 and 2 SDI_12, serial data 3 and 4 SDI_34, serial data 5 and 6 SDI_56, and serial data 7 and 8 SDI_78. The SAI/SAIFB register (configuration register B, address 0x01) is used to specify the serial data format. The default serial data format is I²S, MSB-first.

4.1 Timings

In the STA311B, the BICKI and LRCKI pins are configured as inputs and they must be supplied by the external peripheral.

Figure 3. Timing diagram for SAI interface

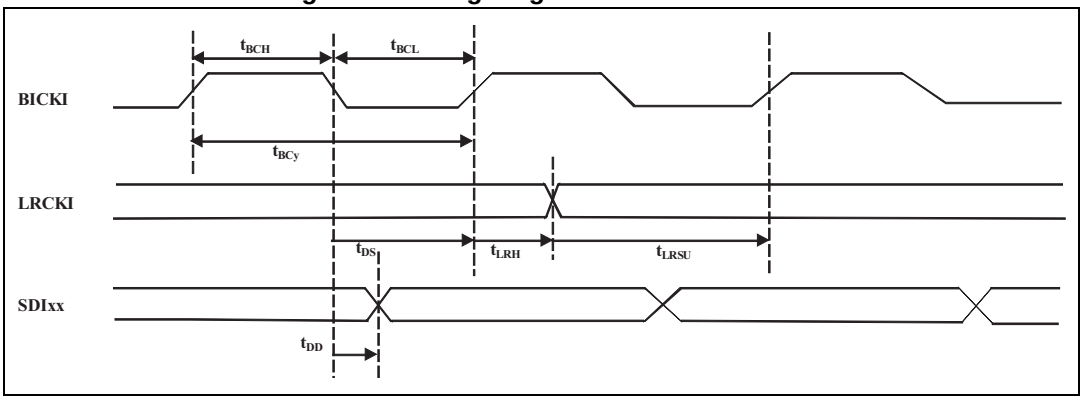


Table 8. Timing parameters for slave mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{BCy}	BICK cycle time	50	-	-	ns
t_{BCH}	BICK pulse width high	20	-	-	ns
t_{BCL}	BICK pulse width low	20	-	-	ns
t_{LRSU}	LRCKI setup time to BICKI strobing edge	10	-	-	ns
t_{LRH}	LRCKI hold time to BICKI strobing edge	10	-	-	ns
t_{DD}	SDI propagation delay from BICKI active edge	0	-	10	ns

4.2 Serial data formats

Available formats are shown in the following tables.

Table 9. Serial data bit first

Bit	RW	RST	Name	Description
4	RW	0	SAIFB	Determines MSB or LSB first for all SAO formats: 0: MSB first 1: LSB first

Note: Serial input and output formats are specified separately

For example, SAI = 1110 and SAIFB = 1 would specify right-justified 16-bit data, LSB-first.

The table below lists the serial audio input formats supported by the STA311B as related to BICKI = 32 * fs, 48 * fs, 64 * fs, where the sampling rate, fs = 32, 44.1, 48, 88.2, 96, 176.4, 192 kHz.

Table 10. Serial audio input formats according to sampling rate

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	1100	X	I²SI²S 15-bit data
	1110	X	Left/right-justified 16-bit data
48 * fs	0100	X	I²S 23-bit data
	0100	X	I²S 20-bit data
	1000	X	I²S 18-bit data
	0100	0	MSB-first I²S 16-bit data
	1100	1	LSB-first I²S 16-bit data
	0001	X	Left-justified 24-bit data
	0101	X	Left-justified 20-bit data
	1001	X	Left-justified 18-bit data
	1101	X	Left-justified 16-bit data
	0010	X	Right-justified 24-bit data
	0110	X	Right-justified 20-bit data
	1010	X	Right-justified 18-bit data
	1110	X	Right-justified 16-bit data

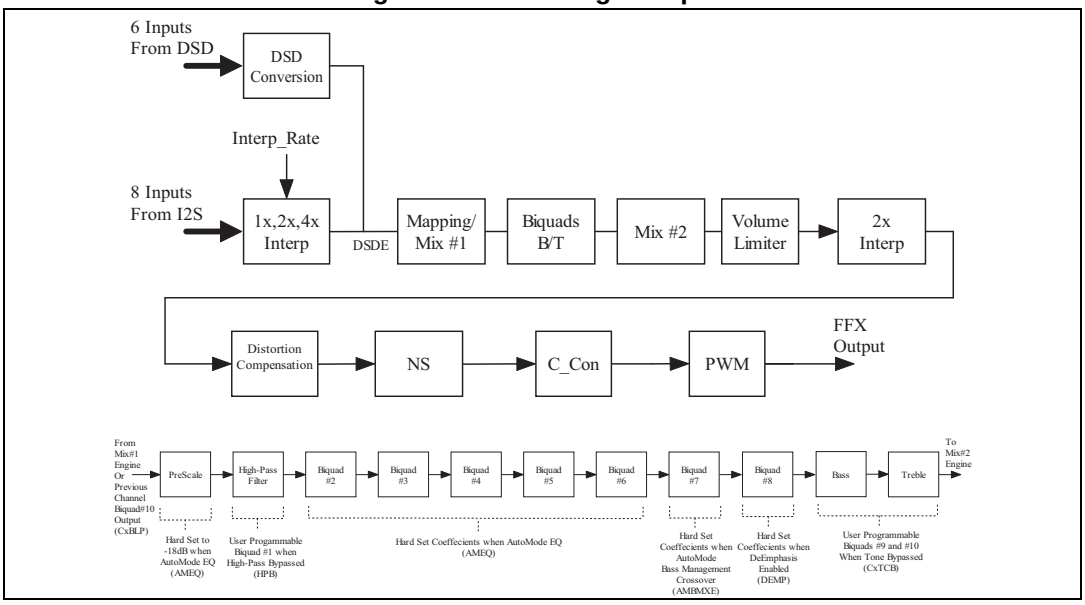
Table 10. Serial audio input formats according to sampling rate (continued)

BICKI	SAI [3:0]	SAIFB	Interface format
64 * fs	0000	X	I²S 24-bit data
	0100	X	I²S 20-bit data
	1000	X	I²S 18-bit data
	0000	0	MSB-first I²S 16-bit data
	1100	1	LSB-first I²S 16-bit data
	0001	X	Left-justified 24-bit data
	0101	X	Left-justified 20-bit data
	1001	X	Left-justified 18-bit data
	1101	X	Left-justified 16-bit data
	0010	X	Right-justified 24-bit data
	0110	X	Right-justified 20-bit data
	1010	X	Right-justified 18-bit data
	1110	X	Right-justified 16-bit data

4.3 Processing data paths

The whole STA311B processing chain is depicted in *Figure 4*. A programmable rate conversion algorithm is applied to the incoming digital audio data (x3,x2,x1,/2) resampling it to the processing rate. A dual-channel plus line out processing is then implemented, with mixing, EQ capability followed by a Volume/DRC block and final DC cut filter. The final oversampling stage and post scaler will provide the output data stream to the PWM modulators. Three different DRC configurations can be used, single-band, dual-band or enhanced dual-band DRC, as shown below.

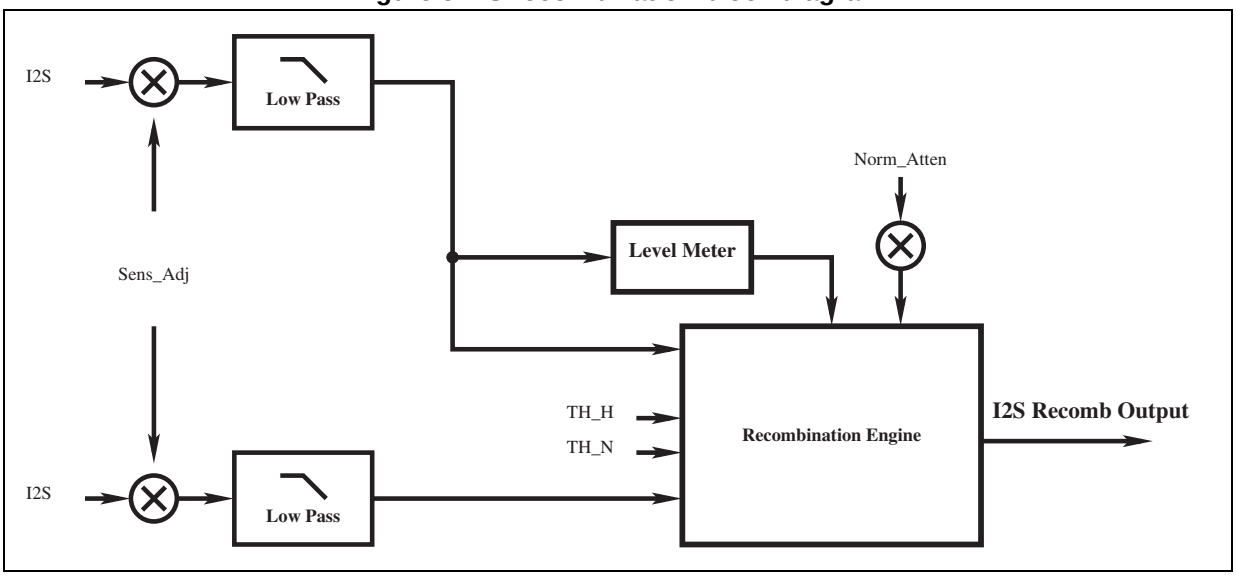
Figure 4. Processing data path



5 I²S recombination interface

The I²S recombination interface shares the same controls for thresholds and gains. However, the low-pass filter is not present and thus the I²S signals coming from the outside should be correctly filtered and conditioned for a correct recombination.

Figure 5. I²S recombination block diagram



6 Startup/shutdown pop noise removal in SE application

Click and pop can generally be defined as undesired audible transients generated by the amplifier system not coming from the system input signal. Such transients can be generated when the amplifier system changes its operating mode: system power-up/power-down, mute/unmute. Every time the PWM starts or stops, if no soft charge method is applied, the result is an audible pop noise.

The STA311B integrates a “pop-elimination” circuitry that removes undesired audible pop noise at the PWM switching start and stop either in single-ended or single-ended virtual ground configurations.

In particular the pop elimination circuit receives as inputs the PWMs generated by the modulator (PWMs_in) and it generates both a delayed version of the PWMs (PWMs_out) and a tristate signal that are sent to the Power stages to attenuate the audible pop at the power up/down.

6.1 PWM start

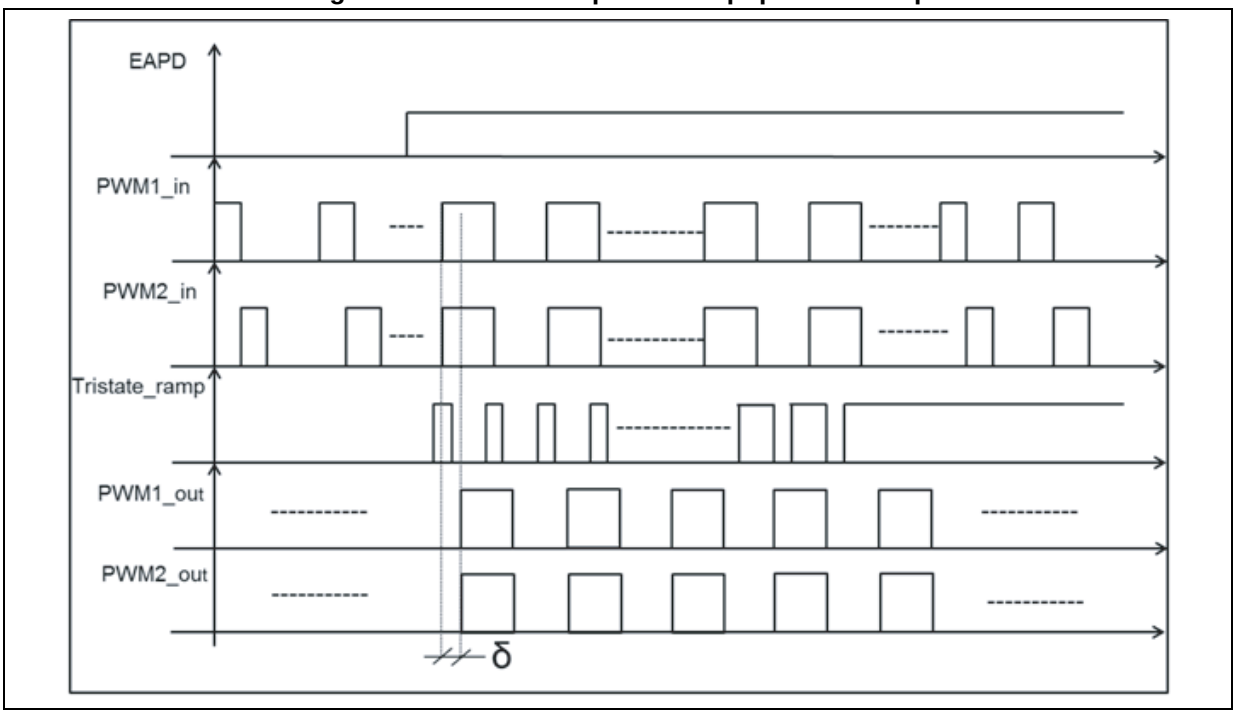
At power-up as soon as the external amplifier power-down (EAPD) is set to one, if at least one channel at the output of the modulator is in binary mode, the pop elimination circuit selects the related PWM input which exhibits the lower PWM timing delay (set using the I²C registers 0x33, 0x34,0x35, 0x36), and it uses it as a PWM reference to synchronize the remaining PWMs_in whose channels are set in binary mode (synchronization phase).

Moreover, during the synchronization phase the modulator is internally muted by setting the audio input signal to

zero. At the end of this phase, all the PWMs_in are synchronous with the PWM reference and they have a duty cycle of 50%.

At each rising edge of the PWM reference, twoTristate_ramp pulses with increasing duty cycle are generated. As depicted in *Figure 10*, where for the sake of simplicity, only two PWMs_in (PWM1_in and PWM2_in) are shown, each pulse is centered with respect to both the rising and falling edges of the PWM reference, and their duty cycle initially set to 21.87% increases gradually and becomes equal to 100% at the end of theTristate_ramp.

Figure 6. Power-on sequence for pop-free startup



Moreover in order to compensate an internal delay between the tristate signal and the PWM present in the Power stage devices, the pop noise removal circuit generates a delayed version of the PWM_in with respect to the Tristate_ramp signal named PWM1_out and PWM2_out in *Figure 6*. The delay value delta between the Tristate_ramp and the PWM_in is programmable using the I²C register 0x80 and the default value is 290 ns.

Finally when the Tristate_ramp duty cycle is equal to 100%, during the de-synchronization phase the PWM time slots, equal for all the PWMs outputs, are changed so that the final channel shift will be the one configured by registers 0x33, 0x34, 0x35 and 0x36. At this point the PWM modulator is automatically un-muted so that the processing outputs can be played.

6.2 PWM stop

When the EAPD signal is set to zero, the modulator is stopped internally, forcing the input audio signal, used to feed the modulator, to zero. After that, the PWM which exhibits the lower PWM timing delay is internally selected and used as a reference. Using the PWM reference, all the PWMs are re-synchronized, and as soon as all PWMs are aligned, at each rising edge of a PWM reference, a reverse tristate_ramp signal is generated. As during startup, the reverse tristate_ramp pulses are centered with respect to the rising and falling edge of the PWM reference, but in this case the starting duty cycle is equal to 100% and gradually becomes equal to zero when the reverse tristate_ramp finishes.

In the STA311B the pop-elimination circuit is activated only when at least one channel is set in binary mode, and the PWMs out speed is set to 384 kHz. In all the other cases the no pop-free PWM switching start/stop procedure is adopted.

7 I²C bus operation

The STA311B supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master).

This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver.

The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA311B is always a slave device in all of its communications.

7.1 Communication protocol

7.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. An SDA transition while the clock is high is used to identify a START or STOP condition.

7.1.2 Start condition

START is identified by a high-to-low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

7.1.3 Stop condition

STOP is identified by a low-to-high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the STA311B and the bus master.

7.1.4 Data input

During the data input the STA311B samples the SDA signal on the rising edge of clock SCL.

For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

7.2 Device addressing

To start communication between the master and the Omega FFX core, the master must initiate with a start condition. Following this, the master sends 8 bits onto the SDA line (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA311B the I²C interface has two device addresses depending on the SA port configuration, 0x40 or 0100000x when SA = 0, and 0x42 or 0100001x when SA = 1.

The 8^{th} bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA311B identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9^{th}-bit time. The byte following the device identification byte is the internal space address.

7.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA311B acknowledges this and the writes for the byte of internal address.

After receiving the internal byte address the STA311B again responds with an acknowledgement.

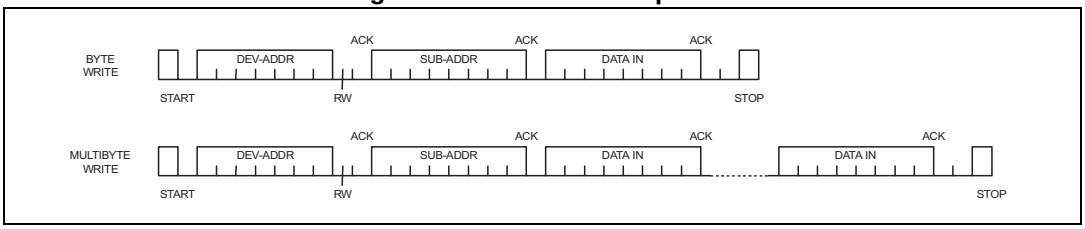
7.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the Omega FFX core. The master then terminates the transfer by generating a STOP condition.

7.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 7. Write mode sequence



7.4 Read operation

7.4.1 Current address byte read

Following the START condition, the master sends a device select code with the RW bit set to 1. The STA311B acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

7.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA311B. The master acknowledges each data byte read and then generates a STOP condition, terminating the transfer.

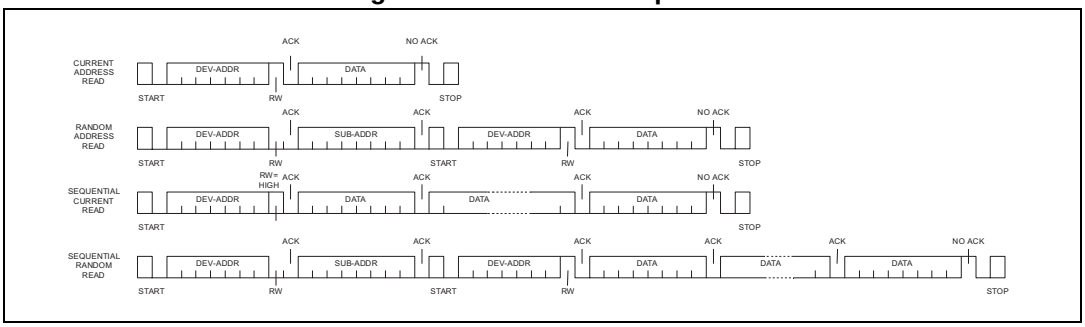
7.4.3 Random address byte read

Following the START condition, the master sends a device select code with the RW bit set to 0. The STA311B acknowledges this and then the master writes the internal address byte. After receiving the internal byte address, the STA311B again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA311B acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

7.4.4 Random address multi-byte read

The multi-byte read mode can start from any internal address. Sequential data bytes are read from sequential addresses within the STA311B. The master acknowledges each data byte read and then generates a STOP condition, terminating the transfer.

Figure 8. Read mode sequence



8 Registers

8.1 Register summary

Table 11. Register summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
Configuration									
0x00	CONFA	COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
0x01	ConfB				SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	ConfC			SAOD4	SAOFB	SAO3	SAO2	SAO1	SAO0
0x03	ConfD	MPC	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x04	ConfE	C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0x05	ConfF	PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0x06	ConfG	MPCV	DCCV	HPE	AM2E	AME	COD	SID	PWMD
0x07	ConfH	ECLE	LDTE	BCLE	IDE	ZDE	SVE	ZCE	NSBW
0x08	ConfI	EAPD							PSCE
Volume control									
0x09	MMUTE								MMUTE
0x0A	Mvol	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x0B	C1Vol	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x0C	C2Vol	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0D	C3Vol	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0E	C4Vol	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0x0F	C5Vol	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0x10	C6Vol	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0x11	C7Vol	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0x12	C8Vol	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0x13	C1VTMB	C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0x14	C2VTMB	C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0x15	C3VTMB	C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0x16	C4VTMB	C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0x17	C5VTMB	C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0x18	C6VTMB	C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0

Table 11. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x19	C7VTMB	C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0x1A	C8VTMB	C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0
Input mapping									
0x1B	C12im		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
0x1C	C34im		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
0x1D	C56im		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
0x1E	C78im		C8IM2	C8IM1	C8IM0		C7IM2	C7IM1	C7IM0
AutoMode									
0x1F	Auto1	AMDM	AMGC2	AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0x20	Auto2	SUB	RSS1	RSS0	CSS1	CSS0	FSS	AMBMXE	AMBMME
0x21	Auto3	AMAM2	AMAM1	AMAM0	AMAME			MSA	AMPS
0x22	PreEQ	XO2	XO1	XO0	PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
0x23	Ageq				AGEQ4	AGEQ3	AGEQ2	AGEQ1	AGEQ0
0x24	Bgeq				BGEQ4	BGEQ3	BGEQ2	BGEQ1	BGEQ0
0x25	Cgeq				CGEQ4	CGEQ3	CGEQ2	CGEQ1	CGEQ0
0x26	Dgeq				DGEQ4	DGEQ3	DGEQ2	DGEQ1	DGEQ0
0x27	Egeq				EGEQ4	EGEQ3	EGEQ2	EGEQ1	EGEQ0
Processing loop									
0x28	BQlp	C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP
0x29	MXlp	C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
Processing bypass									
0x2A	EQbp	C8EQBP	C7EQBP	C6EQBP	C5EQB	C4EQBP	C3EQBP	C2EQBP	C1EQBP
0x2B	ToneBP	C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
Tone control									
0x2C	Tone	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
Dynamics control									
0x2D	C1234ls	C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
0x2E	C5678ls	C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
0x2F	L1ar	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x30	L1atrt	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x31	L2ar	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0

Table 11. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x32	L2atrt	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
PWM output timing									
0x33	C12ot		C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
0x34	C34ot		C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
0x35	C56ot		C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
0x36	C78ot		C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
I²S output channel mapping									
0x37	C12om		C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0
0x38	C34om		C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
0x39	C56om		C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
0x3A	C78om		C8OM2	C8OM1	C8OM0		C7OM2	C7OM1	C7OM0
User-defined coefficient RAM									
0x3B	Cfaddr1							CFA9	CFA8
0x3C	Cfaddr2	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x3D	B1cf1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x3E	B1cf2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x3F	B1cf3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x40	B2cf1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x41	B2cf2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x42	B2cf3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x43	A1cf1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x44	A1cf2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x45	A1cf3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x46	A2cf1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x47	A2cf2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x48	A2cf3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x49	B0cf1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x4A	B0cf2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x4B	B0cf3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x4C	Cfud							WA	W1
0x4D	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x4E	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x4F	DCC1	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x50	DCC2	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0

Table 11. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x51	PSC1	RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4
0x52	PSC2	RCV3	RCV2	RCV1	RCV0	CNV11	CNV10	CNV9	CNV8
0x53	PSC3	CNV7	CNV6	CNV5	CNV4	CNV3	CNV2	CNV1	CNV0
I²S recombination interface									
0x5D	RCTR1	Boost6db			I²S_byp	I²S_en			
0x5E	PDMCT	AdvM6	AdvM5	AdvM4	AdvM3	AdvM2	AdvM1		
0x5F	RCTR2		bypRM1	CH1GG[5:0]					
0x60	RCTR3		bypRM2	CH2GG[5:0]					
0x61	RCTR4		bypRM3	CH3GG[5:0]					
0x62	RCTR5		LP1en	CH1NCA[5:0]					
0x63	RCTR6		LP2en	CH2NCA[5:0]					
0x64	RCTR7		LP3en	CH3NCA[5:0]					
0x65	RCTR8			CH1TH_N[5:0]					
0x66	RCTR9			CH2TH_N[5:0]					
0x67	RCTR10			CH3TH_N[5:0]					
0x68	RCTR11			CH1TH_H[5:0]					
0x69	RCTR12			CH2TH_H[5:0]					
0x6A	RCTR13			CH3TH_H[5:0]					
Extended DRC configuration registers									
0x6B	nL1at		L1AT6	L1AT5	L1AT4	L1AT3	L1AT2	L1AT1	L1AT0
0x6C	nL2at		L2AT6	L2AT5	L2AT4	L2AT3	L2AT2	L2AT1	L2AT0
0x6D	nL1rt			L1RT5	L1RT4	L1RT3	L1RT2	L1RT1	L1RT0
0x6E	nL2rt			L2RT5	L2RT4	L2RT3	L2RT2	L2RT1	L2RT0
0x6F	0Mute	RMSZS2	RMSZS1	RMSZS0	ZMTHS2	ZMTHS1	ZMTHS0	ZMHYS1	ZMHYS0
0x70		RMS2	RMS1	RMS0					FXLRC0
Clock manager configuration/status registers									
0x71	pllfrac1	PLFI15	PLFI14	PLFI13	PLFI12	PLFI11	PLFI10	PLFI9	PLFI8
0x72	pllfrac0	PLFI7	PLFI6	PLFI5	PLFI4	PLFI3	PLFI2	PLFI1	PLFI0
0x73	pll div	PLLDD1	PLLDD0	PLLND5	PLLND4	PLLND3	PLLND2	PLLND1	PLLND0
0x74	pll conf0	PDPDC	PLLFC	PLSTRB	PLSTBB	PLIFD3	PLIFD2	PLIFD1	PLIFD0

Table 11. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x75	pll conf1					PLLBYP	PLLDPR	LOWEN	BST32K
0x76	pll stat					PLLBYS	PLLPDS	OSCOK	LOWCKS
Biquad configuration									
0x77	CBQ1	EBQ3_1	EBQ3_0	EBQ2_1	EBQ2_0	EBQ1_1	EBQ1_0	EBQ0_0	EBQ0_0
0x78	CBQ2	EBQ7_1	EBQ7_0	EBQ6_1	EBQ6_0	EBQ5_1	EBQ5_0	EBQ4_0	EBQ4_0
0x79	CBQ3				nshen	EBQ9_1	EBQ9_0	EBQ8_0	EBQ8_0
RMS status registers									
0x7A	rmsZMH	RZM15	RZM14	RZM13	RZM12	RZM11	RZM10	RZM9	RZM8
0X7B	rmsZML	RZM7	RZM6	RZM5	RZM4	RZM3	RZM2	RZM1	RZM0
0X7C	rmsPOH	RPO15	RPO14	RPO13	RPO12	RPO11	RPO10	RPO9	RPO8
0X7D	rmsPOL	RPO7	RPO6	RPO5	RPO4	RPO3	RPO2	RPO1	RPO0
Tristate startup/shutdown pop removal signals									
0x80	DPT				DPT4	DPT3	DPT2	DPT1	DPT0
0x81	CFR129	RL3	RL2	RL1	RL0	RD	SID1	FBYP	RTP
0x82	TSDLY1	UDDT15	UDDT14	UDDT13	UDDT12	UDDT11	UDDT10	UDDT9	UDDT8
0x83	TSDLY2	UDDT7	UDDT6	UDDT5	UDDT4	UDDT3	UDDT2	UDDT1	UDDT0

8.2 Register description

8.2.1 Configuration register A (0x00)

D7	D6	D5	D4	D3	D2	D1	D0
COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
1	0	0	0	0	0	1	1

Bit	RW	RST	Name	Description
0	RW	1	MCS0	Master clock select: selects the ratio between the input I²S sampling frequency and the input clock.
1	RW	1	MCS1	
2	RW	0	MCS2	

The STA311B supports sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz, 2.8224 MHz DSD. Therefore the internal clocks are:

- 65.536 MHz for 32 kHz
- 90.3168 MHz for 44.1 kHz, 88.2 kHz, 176.4 kHz, and DSD
- 98.304 MHz for 48 kHz, 96 kHz, 192 kHz

The external clock frequency provided to the XTI or BICKI pin (depending on the MCS settings) must be a multiple of the input sampling frequency (fs). The relationship between the input clock (either XTI or BICKI) and the input sampling rate is determined by both the MCS[2:0] and the IR[1:0] (input rate) register bits in normal mode, if the Fs autodetect mode has been set, the IR[1:0] parameter and the BST32K bit will be set automatically (see *Fs autodetection on page 32*). The MCS[2:0] bits determine the PLL factor generating the internal clock and the IR[1:0] bits determine the oversampling ratio used internally.

If XTI input is not used, related pin must be tied to GND.

To get 98.304 MHz of system clock frequency when fs = 32 kHz, an extra oversampling factor is available by setting the BST32K bit in the 0x75 register (see *Clock manager configuration register (0x75) on page 93*).

Input sampling rate *fs* (kHz)	IR	MCS[2:0]						
		BICKI		XTI				
		111	110	10-	011	010	001	000
32, 44.1, 48	00	64*fs	na	128*fs	256*fs	384*fs	512*fs	768*fs
88.2, 96	01	64*fs	32*fs	64*fs	128*fs	192*fs	256*fs	384*fs
176.4, 192	10	64*fs	32*fs	64*fs	128*fs	192*fs	256*fs	na
DSD/PDM	11	2*fs	2*fs	2*fs	4*fs	6*fs	8*fs	12*fs

Fs autodetection

When FXLRC0 = '0' (see 0x70 register), the autodetection function is disabled, IR[1:0] and BST32K must be set via I²C. When FXLRC0 = '1' the autodetection function is enabled, then IR and BST32K will be set automatically based on Fs. Before and after enabling the function m, LRCKI must be stable for at least 3 cycles with a fixed Fs as reference. After 3 fixed Fs cycles when the function has been enabled, the real Fs can be fed to LRCKI.

Interpolation ratio select

Bit	RW	RST	Name	Description
3	RW	0	IR0	Interpolation ratio select: selects internal interpolation ratio based on input I²S sample frequency
4	RW	0	IR1	

The STA311B has variable interpolation (oversampling) settings such that internal processing and FFX output rates remain consistent. The first processing block interpolates by either 4 times, 2 times, or 1 time (pass-through).

The oversampling ratio of this interpolation is determined by the IR bits.

IR[1,0]	Input sample rate *Fs* (kHz)	1st stage interpolation ratio
00	32	4-times oversampling
00	44.1	4-times oversampling
00	48	4-times oversampling
01	88.2	2-times oversampling
01	96	2-times oversampling
10	176.4	Pass-through
10	192	Pass-through
11	DSD	DSD to 176.4 kHz conversion

Bit	RW	RST	Name	Description
0	RW	0	DSPB	DSP bypass bit: 0: normal operation 1: bypass of biquad and bass/treble functions

Setting the DSPB bit bypasses the biquad function of the processing core of the STA311B.

COS[1,0]	CKOUT frequency
00	PLL output
01	PLL output / 4
10	PLL output / 8
11	PLL output / 16

8.2.2 Configuration register B (0x01) - serial input formats

D7	D6	D5	D4	D3	D2	D1	D0
			SAIFB	SAI3	SAI2	SAI1	SAI0
			0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	SAI0	Serial audio input interface format: determines the interface format of the input serial digital audio interface
1	RW	0	SAI1	
2	RW	0	SAI2	
3	RW	0	SAI3	

Serial data interface

The STA311B audio serial input interfaces with standard digital audio components and accepts a number of serial data formats. The STA311B always acts a slave when receiving audio input from standard digital audio components. Serial data for eight channels is provided using 6 input pins: left/right clock LRCKI, serial clock BICKI, serial data 1 and 2 SDI_12, serial data 3 and 4 SDI_34, serial data 5 and 6 SDI_56, and serial data 7 and 8 SDI_78. The SAI/SAIFB register (configuration register B, address 0x01) is used to specify the serial data format. The default serial data format is I²S, MSB-first. Available formats are shown in the tables that follow.

Bit	RW	RST	Name	Description
4	RW	0	SAIFB	Determines MSB or LSB first for all SAO formats: 0: MSB first 1: LSB first

Note: Serial input and output formats are specified separately.

For example, SAI = 1110 and SAIFB = 1 would specify right-justified 16-bit data, LSB-first.

The table below lists the serial audio input formats supported by STA311B as related to BICKI = 32 * fs, 48 * fs, 64 * fs, where sampling rate, fs = 32, 44.1, 48, 88.2, 96, 176.4, 192 kHz.

Table 12. Serial audio input formats according to sampling rate

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	1100	X	I²S 15-bit data
	1110	X	Left/right-justified 16-bit data
48 * fs	0100	X	I²S 23-bit data
	0100	X	I²S 20-bit data
	1000	X	I²S 18-bit data
	0100	0	MSB-first I²S 16-bit data
	1100	1	LSB-first I²S 16-bit data
	0001	X	Left-justified 24-bit data
	0101	X	Left-justified 20-bit data
	1001	X	Left-justified 18-bit data
	1101	X	Left-justified 16-bit data
	0010	X	Right-justified 24-bit data
	0110	X	Right-justified 20-bit data
	1010	X	Right-justified 18-bit data
	1110	X	Right-justified 16-bit data
64 * fs	0000	X	I²S 24-bit data
	0100	X	I²S 20-bit data
	1000	X	I²S 18-bit data
	0000	0	MSB-first I²S 16-bit data
	1100	1	LSB-first I²S 16-bit data
	0001	X	Left-justified 24-bit data
	0101	X	Left-justified 20-bit data
	1001	X	Left-justified 18-bit data
	1101	X	Left-justified 16-bit data
	0010	X	Right-justified 24-bit data
	0110	X	Right-justified 20-bit data
	1010	X	Right-justified 18-bit data
	1110	X	Right-justified 16-bit data

8.2.3 Configuration register C (0x02) - serial output formats

D7	D6	D5	D4	D3	D2	D1	D0
		SAOD4	SAOFB	SAO3	SAO2	SAIO	SAO0
		0	0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	SAO0	Serial audio output interface format: determines the interface format of the output serial digital audio interface.
1	RW	0	SAO1	
2	RW	0	SAO2	
3	RW	0	SAO3	

The STA311B features a serial audio output interface that consists of 8 channels. The serial audio output always acts as a slave to the serial audio input interface and, therefore, all output clocks are synchronous with the input clocks. The output sampling frequency (fs) is also equivalent to the input sampling frequency. In the case of SACD/DSD input, the serial audio output acts as a master with an output sampling frequency of 8 xfs, 4 xfs or fs depending on SAOD4 bit. The output serial format can be selected independently from the input format and is done via the SAO and SAOFB bits.

Bit	RW	RST	Name	Description
4	RW	0	SAOFB	Determines MSB or LSB first for all SAO formats: 0: MSB first 1: LSB first

Bit	RW	RST	Name	Description
5	RW	0	SAOD4	Enables decimation by 4 on SAO interface for SACD/DSD input; no effect for others. 0: div by 1 1: div by 4 (1)

1. To avoid any aliasing on SAO streaming, a low-pass filter is needed to be implemented in one of the available user-programmable biquads.

Table 13. Serial audio output formats according to sampling rate

BICKI = BICKO	SAO[3:0]	Interface data format
32 * fs	0111	I²S data
	1111	Left/right-justified 16-bit data
48 * fs	1110	I²S data
	0001	Left-justified data
	1010	Right-justified 24-bit data
	1011	Right-justified 20-bit data
	1100	Right-justified 18-bit data
	1101	Right-justified 16-bit data
64 * fs	0000	I²S data
	0001	Left-justified data
	0010	Right-justified 24-bit data
	0011	Right-justified 20-bit data
	0100	Right-justified 18-bit data
	0101	Right-justified 16-bit data

8.2.4 Configuration register D (0x03)

D7	D6	D5	D4	D3	D2	D1	D0
MPC	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
1	1	1	1	1	1	1	0

Bit	RW	RST	Name	Description
0	RW	0	OM0	FFX power output mode: selects configuration of FFX output
1	RW	1	OM1	

The FFX power output mode selects how the FFX output timing is configured. Different power devices use different output modes. The STA50x recommended use is OM = 10.

OM[1,0]	Output stage - mode
00	STA50x/STA51xB - drop compensation
01	Discrete output stage - tapered compensation
10	STA50x/STA51xB - full-power mode
11	Variable drop compensation (CSZn bits)

Bit	RW	RST	Name	Description
2	RW	1	CSZ0	Contra size register: when OM[1,0] = 11, this register determines the size of the FFX compensating pulse from 0 clock ticks to 31 clock periods
3	RW	1	CSZ1	
4	RW	1	CSZ2	
5	RW	1	CSZ3	
6	RW	1	CSZ4	

CSZ[4:0]	Compensating pulse size
00000	0 clock period compensating pulse size
00001	1 clock period compensating pulse size
…	…
11111	31 clock period compensating pulse size

Bit	RW	RST	Name	Description
7	RW	1	MPC	Max power correction: setting of 1 enables STA50x correction for THD reduction near maximum power output.

Setting the MPC bit turns on special processing that corrects the STA50x power device at high power. This mode should lower the THD+N of a full STA50x FFX system at maximum power output and slightly below. This mode will only be operational in OM[1,0] = 01.

8.2.5 Configuration register E (0x04)

D7	D6	D5	D4	D3	D2	D1	D0
C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	C1BO	Channels 1, 2, 3, 4, 5, 6, 7, and 8 binary output mode enable bits. A setting of 0 indicates ordinary FFX tristate output. A setting of 1 indicates binary output mode.
1	RW	0	C2BO	
2	RW	0	C3BO	
3	RW	0	C4BO	
4	RW	0	C5BO	
5	RW	0	C6BO	
6	RW	0	C7BO	
7	RW	0	C8BO	

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel will be considered the positive output and output B is the negative inverse.

8.2.6 Configuration register F (0x05)

D7	D6	D5	D4	D3	D2	D1	D0
PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	HPB	High-pass filter bypass bit: setting of one bypasses internal AC coupling digital high-pass filter

The STA311B features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through an FFX amplifier. DC signals can cause speaker damage.

If HPB = 1, then the filter that the high-pass filter utilizes is made available as user-programmable biquad #1.

Bit	RW	RST	Name	Description
1	RW	0	DRC	Dynamic range compression/anti-clipping 0: limiters act in anti-clipping mode 1: limiters act in dynamic range compression mode

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode, the limiter threshold values are constant and dependent on the limiter settings.

In dynamic range compression mode, the limiter threshold values vary with the volume settings allowing a nighttime listening mode that provides a reduction in the dynamic range regardless of the volume level.

Bit	RW	RST	Name	Description
2	RW	0	DEMP	De-emphasis: 0: no de-emphasis 1: de-emphasis

By setting this bit to one de-emphasis will be implemented on all channels. When this is used it takes the place of biquad #7 in each channel and any coefficients using biquad #1 will be ignored. The DSPB (DSP bypass) bit must be set to 0 for de-emphasis to function.

Bit	RW	RST	Name	Description
3	RW	0	PSL	Post-scale link: 0: each channel uses individual post-scale value 1: each channel uses channel 1 post-scale value

Post-scale functionality can be used for power-supply error correction. For multi-channel applications running off the same power-supply, the post-scale values can be linked to the value of channel 1 for ease of use and in order to update the values faster.

Bit	RW	RST	Name	Description
4	RW	0	BQL	Biquad link: 0: each channel uses coefficient values 1: each channel uses channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the channel 1 coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

Bit	RW	RST	Name	Description
7:5	RW	00	PWMS[2:0]	PWM speed selection

PWMS[1:0]	PWM output speed
000	Normal speed (384 kHz) (all channels)
001	Half-speed (192 kHz) (all channels)
010	Double-speed (768 kHz) (all channels)
011	Normal speed (channels 1-6), double-speed (channels 7-8)
100	Odd speed (341.3 kHz) (all channels)

8.2.7 Configuration register G (0x06)

D7	D6	D5	D4	D3	D2	D1	D0
MPCV	DCCV	HPE	AM2E	AME	COD	SID	PWMD
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	PWMD	PWM output disable: 0: PWM output normal 1: no PWM output
1	RW	0	SID	Serial interface (I²S out) disable: 0: I²S output normal 1: no I²S output
2	RW	0	COD	Clock output disable: 0: clock output normal 1: no clock output

Bit	RW	RST	Name	Description
3	RW	0	AME	AM mode enable: 0: normal FFX operation 1: AM reduction mode FFX operation

The STA311B features an FFX processing mode that minimizes the amount of noise generated in the frequency range of AM radio. This mode is intended for use when FFX is operating in a device with an active AM tuner. The SNR of the FFX processing is reduced to ~83 dB in this mode, which is still greater than the SNR of AM radio.

Bit	RW	RST	Name	Description
4	RW	0	AM2E	AM2 mode enable: 0: normal FFX operation 1: AM2 reduction mode FFX operation

The STA311B features two FFX processing modes that minimize the amount of noise generated in the frequency range of AM radio. This second mode is intended for use when

FFX is operating in a device with an active AM tuner. This mode eliminates the noise-shaper.

Bit	RW	RST	Name	Description
5	RW	0	HPE	FFX headphone enable: 0: channels 7 and 8 normal FFX operation 1: channels 7 and 8 headphone operation

Channels 7 and 8 can be configured to be processed and output in such a manner that headphones can be driven using an appropriate output device. This signal is a differential 3-wire drive called FFX headphone.

Bit	RW	RST	Name	Description
6	RW	0	DCCV	Distortion compensation variable enable: 0: uses the preset DC coefficient 1: uses the DCC coefficient

Bit	RW	RST	Name	Description
7	RW	0	MPCV	Max power correction variable: 0: uses the standard MPC coefficient 1: uses the MPCC bits for the MPC coefficient

8.2.8 Configuration register H (0x07)

D7	D6	D5	D4	D3	D2	D1	D0
ECLE	LDTE	BCLE	IDE	ZDE	SVE	ZCE	NSBW
0	1	1	1	1	1	1	0

Bit	RW	RST	Name	Description
0	RW	0	NSBW	Noise-shaper bandwidth selection: 1: 3rd order NS 0: 4th order NS

Bit	RW	RST	Name	Description
1	RW	1	ZCE	Zero-crossing volume enable: 1: volume adjustments will only occur at digital zero-crossings 0: volume adjustments will occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings, no clicks will be audible.

Bit	RW	RST	Name	Description
2	RW	1	SVE	Soft volume enable: 1: volume adjustments use soft volume 0: volume adjustments occur immediately

Bit	RW	RST	Name	Description
3	RW	1	ZDE	Zero-detect mute enable: setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute. See *Section 9.5.7* for more details.

Bit	RW	RST	Name	Description
4	RW	1	IDE	Invalid input detect mute enable: 1: enable the automatic invalid input detect mute

Setting the IDE bit enables this function, which looks at the input I²S data and will automatically mute if the signals are perceived as invalid.

Bit	RW	RST	Name	Description
5	RW	1	BCLE	Binary output mode clock loss detection enable

The BCLE bit detects loss of input MCLK in binary mode and will output 50% duty cycle.

Bit	RW	RST	Name	Description
6	RW	1	LDTE	LRCLK double trigger protection enable

The LDTE bit actively prevents double triggering of LRCLK.

Bit	RW	RST	Name	Description
7	RW	0	ECLE	Auto EAPD on clock loss

When active, the ECLE bit will issue a device power-down signal (EAPD) on clock loss detection.

8.2.9 Configuration register I (0x08)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD							PSCE
0							0

This feature utilizes an ADC on SDI78 that provides power supply ripple information for correction. Registers PSC1, PSC2, PSC3 are utilized in this mode.

Bit	RW	RST	Name	Description
0	RW	0	PSCE	Power supply ripple correction enable: 0: normal operation 1: PSCorrect operation

Bit	RW	RST	Name	Description
7	RW	0	EAPD	External amplifier power-down: 0: external power stage power-down active 1: normal operation

8.2.10 Master mute register (0x09)

D7	D6	D5	D4	D3	D2	D1	D0
							MMUTE
							0

8.2.11 Master volume register (0x0A)

D7	D6	D5	D4	D3	D2	D1	D0
MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
1	1	1	1	1	1	1	1

Note: The value of the volume derived from MVOL is dependent on the AMV AutoMode volume settings.

8.2.12 Channel 1 volume (0x0B)

D7	D6	D5	D4	D3	D2	D1	D0
C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0	1	1	0	0	0	0	0

8.2.13 Channel 2 volume (0x0C)

D7	D6	D5	D4	D3	D2	D1	D0
C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0	1	1	0	0	0	0	0

8.2.14 Channel 3 volume (0x0D)

D7	D6	D5	D4	D3	D2	D1	D0
C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0	1	1	0	0	0	0	0

8.2.15 Channel 4 volume (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0
C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0	1	1	0	0	0	0	0

8.2.16 Channel 5 volume (0x0F)

D7	D6	D5	D4	D3	D2	D1	D0
C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0	1	1	0	0	0	0	0

8.2.17 Channel 6 volume (0x10)

D7	D6	D5	D4	D3	D2	D1	D0
C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0	1	1	0	0	0	0	0

8.2.18 Channel 7 volume (0x11)

D7	D6	D5	D4	D3	D2	D1	D0
C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0	1	1	0	0	0	0	0

8.2.19 Channel 8 volume (0x12)

D7	D6	D5	D4	D3	D2	D1	D0
C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0	1	1	0	0	0	0	0

8.2.20 Channel 1 volume trim, mute, bypass (0x13)

D7	D6	D5	D4	D3	D2	D1	D0
C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0	0	0	1	0	0	0	0

8.2.21 Channel 2 volume trim, mute, bypass (0x14)

D7	D6	D5	D4	D3	D2	D1	D0
C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0	0	0	1	0	0	0	0

8.2.22 Channel 3 volume trim, mute, bypass (0x15)

D7	D6	D5	D4	D3	D2	D1	D0
C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0	0	0	1	0	0	0	0

8.2.23 Channel 4 volume trim, mute, bypass (0x16)

D7	D6	D5	D4	D3	D2	D1	D0
C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0	0	0	1	0	0	0	0

8.2.24 Channel 5 volume trim, mute, bypass (0x17)

D7	D6	D5	D4	D3	D2	D1	D0
C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0	0	0	1	0	0	0	0

8.2.25 Channel 6 volume trim, mute, bypass (0x18)

D7	D6	D5	D4	D3	D2	D1	D0
C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0
0	0	0	1	0	0	0	0

8.2.26 Channel 7 volume trim, mute, bypass (0x19)

D7	D6	D5	D4	D3	D2	D1	D0
C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0	0	0	1	0	0	0	0

8.2.27 Channel 8 volume trim, mute, bypass (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0
C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0
0	0	0	1	0	0	0	0

The volume structure of the STA311B consists of individual volume registers for each channel and a master volume register that provides an offset to each channel's volume setting. There is also an additional offset for each channel called channel volume trim. The individual channel volumes are adjustable in 0.5 dB steps from +48 dB to -78 dB. As an example if C5V = 0xXX or +XXX dB and MV = 0xXX or -XX dB, then the total gain for channel 5 = XX dB. The channel volume trim is adjustable independently on each channel from -10 dB to +10 dB in 1 dB steps.

The master mute when set to 1 will mute all channels at once, whereas the individual channel mutes (CnM) will mute only that channel. Both the master mute and the channel mutes provide a "soft mute" with the volume ramping down to mute in 8192 samples from the maximum volume setting at the internal processing rate (~192 kHz). A "hard mute" can be obtained by commanding a value of 0xFF (255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel whose total volume is less than -91 dB will be muted. All changes in volume take place at zero-crossings when ZCE = 1 (configuration register H) on a per-channel basis as this creates the smoothest possible volume transitions. When ZCE = 0, volume updates occur immediately. Each channel also contains an individual channel volume bypass. If a particular channel has volume bypassed via the CnVBP = 1 register, then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel. Each channel also contains a channel mute. If CnM = 1 a soft mute is performed on that channel.

MV[7:0]	Volume offset from channel value
0x00	0 dB
0x01	-0.5 dB
0x02	-1 dB
…	…
0x4C	-38 dB
…	…
0xFE	-127 dB
0xFF	Hardware channel mute

CnV[7:0]	Volume
0x00	+48 dB
0x01	+47.5 dB
0x02	+47 dB
…	…
0x5F	+0.5 dB
0x60	0 dB
0x61	-0.5 dB
…	…
0xFE	-79.5 dB
0xFF	Hardware channel mute

CnVT[4:0]	Volume
0x00 to 0x06	+10 dB
0x07	+9 dB
…	…
0x0F	+1 dB
0x10	0 dB
0x11	-1 dB
…	…
0x19	-9 dB
0x1A to 0x1F	-10 dB

8.2.28 Channel input mapping channels 1 and 2 (0x1B)

D7	D6	D5	D4	D3	D2	D1	D0
	C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
	0	0	1		0	0	0

8.2.29 Channel input mapping channels 3 and 4 (0x1C)

D7	D6	D5	D4	D3	D2	D1	D0
	C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
	0	1	1		0	1	0

8.2.30 Channel input mapping channels 5 and 6 (0x1D)

D7	D6	D5	D4	D3	D2	D1	D0
	C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
	1	0	1		1	0	0

8.2.31 Channel input mapping channels 7 and 8 (0x1E)

D7	D6	D5	D4	D3	D2	D1	D0
	C8IM2	C8M1	C8IM0		C7IM2	C7IM1	C7IM0
	1	1	1		1	1	0

Each channel received via I²S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing, simplifies output stage designs, and enables the ability to perform crossovers. The default settings of these registers map each I²S input channel to its corresponding processing channel.

CnIM[2:0]	Serial input from
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6
110	Channel 7
111	Channel 8

8.2.32 AUTO1 - AutoModes EQ, volume, GC (0x1F)

D7	D6	D5	D4	D3	D2	D1	D0
AMDM	AMGC2	AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
1:0	RW	0	AMEQ[1:0]	Biquad 2-6 mode is: 00: user-programmable 01: preset EQ - PEQ bits 10: graphic EQ - xGEQ bits 11: auto volume-controlled loudness curve

Setting AMEQ to any setting other than 00 enables AutoMode EQ, biquads 1-5 are not user-programmable. Any coefficient settings for these biquads will be ignored. Also when AutoMode EQ is used, the pre-scale value for channels 1-6 becomes hard-set to -18 dB.

Bit	RW	RST	Name	Description
3:2	RW	0	AMV[1:0]	AutoMode volume mode (MVOL) is: 00: MVOL 0.5 dB 256 steps (standard) 01: MVOL auto curve 30 steps 10: MVOL auto curve 40 steps 11: MVOL auto curve 50 steps
6:4	RW	0	AMGC[2:0]	AutoMode gain compression/limiters mode is: 000: user programmable GC 001: AC no clipping 010: AC limited clipping (10%) 011: DRC nighttime listening mode 100: DRC TV commercial/channel AGC 101: AC 5.1 no clipping 110: AC 5.1 limited clipping (10%)

Bit	RW	RST	Name	Description
7	RW	0	AMDM	AutoMode 5.1 downmix: 0: normal operation 1: channels 7-8 are 2-channel downmix of channels 1-6

AutoMode downmix setting uses channels 7-8 of Mix#1 engine and therefore these channels of this function are fixed and not allowed to be set by the user when in this mode.

Channels 1-6 must be arranged via channel mapping (registers CnIM) if necessary in the following manner for this operation:

Channel 1: left
Channel 2: right
Channel 3: left surround
Channel 4: right surround
Channel 5: center
Channel 6: LFE

8.2.33 AUTO2 - AutoModes bass management2 (0x20)

D7	D6	D5	D4	D3	D2	D1	D0
SUB	RSS1	RSS0	CSS1	CSS0	FSS	AMBMXE	AMBMME
1	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	AMBMME	0: AutoMode bass management mix disabled 1: AutoMode bass management mix enabled

Bit	RW	RST	Name	Description
1	RW	0	AMBMXE	0: AutoMode bass management crossover disabled 1: AutoMode bass management crossover enabled

Setting the AMBMME bit enables the proper mixing to take place for various preset bass management configurations. Setting the AMBMXE bit enables the proper crossover filtering in biquad #7 to take place. The crossover for bass management is always 2^{nd} order (24 dB/oct) and the crossover frequency is determined by register bits PREEQ.XO[2:0].

All configurations of Dolby Bass Management can be performed in the IC. These different configurations are selected by the end user.

The AutoMode bass management settings utilize channels 1-6 on the mix #1 engine, channels 1-6 biquad #6, and channels 1-2 on the mix #2 engine in configuration #2. These functions cannot be user-programmed while the bass management automode is active.

Not all settings are valid as some configurations are unlikely and do not have to be supported by Dolby specifications.

Automatic crossover settings are provided or custom crossovers can be implemented using the available programmable biquads.

Input channels must be mapped using the channel-mapping feature in the following manner for bass management to be performed properly.

1: left front

2: right front

3: left rear

4: right rear

5: center

6: LFE

Bitfield	10	01	00
CSS - center speaker size	Off	Large	Small
RSS - rear speaker size	Off	Large	Small

Bitfield	1	0
FSS - front speaker size	Large	Small
SUB - subwoofer	On	Off

When AMBMXE = 1, biquad #7 on channels 1-6 are utilized for the bass-management crossover filter, this biquad is not user-programmable in this mode. The XO settings determine the crossover frequency used, the crossover is 2nd order for both high-pass and low-pass with a -3 dB cross point. Higher order filters can be obtained by programming coefficients in other biquads if desired.

It is recommended to use settings of 120-160 Hz when using small, single-driver satellite speakers as the frequency response of these speakers normally are limited to this region.

8.2.34 AUTO3 - AutoMode AM/pre-scale/bass management scale (0x21)

D7	D6	D5	D4	D3	D2	D1	D0
AMAM2	AMAM1	AMAM0	AMAME			MSA	AMPS
0	0	0	0			0	1

Bit	RW	RST	Name	Description
0	RW	0	AMPS	AutoMode pre-scale 1: -18 dB used for pre-scale when AMEQ /= 00 0: user-defined pre-scale when AMEQ /= 00

Bit	RW	RST	Name	Description
1	RW	0	MSA	Bass management mix scale adjustment 0: -12 dB scaling on satellite channels in config #1 1: no scaling on satellite channels in config #1

Bit	RW	RST	Name	Description
4	RW	0	AMAME	AutoMode AM enable 0: switching frequency determined by PWMS settings 1: switching frequency determined by AMAM settings

AMAM[2:0]	48 kHz/96 kHz input Fs	44.1 / 88.2 kHz input Fs
000	0.535 MHz - 0.720 MHz	0.535 MHz - 0.670 MHz
001	0.721 MHz - 0.900 MHz	0.671 MHz - 0.800 MHz
010	0.901 MHz - 1.100 MHz	0.801 MHz - 1.000 MHz
011	1.101 MHz - 1.300 MHz	1.001 MHz - 1.180 MHz
100	1.301 MHz - 1.480 MHz	1.181 MHz - 1.340 MHz
101	1.481 MHz - 1.600 MHz	1.341 MHz - 1.500 MHz
110	1.601 MHz - 1.700 MHz	1.501 MHz - 1.700 MHz

8.2.35 PREEQ - Preset EQ settings (0x22)

D7	D6	D5	D4	D3	D2	D1	D0
XO2	XO1	XO0	PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
1	0	1	0	0	0	0	0

XO[2:0]	Bass management crossover frequency
000	70 Hz
001	80 Hz
010	90 Hz
011	100 Hz
100	110 Hz
101	120 Hz
110	140 Hz
111	160 Hz

PEQ[4:0]	Mode / setting
00000	Flat
00001	Rock
00010	Soft Rock
00011	Jazz
00100	Classical
00101	Dance
00110	Pop
00111	Soft
01000	Hard
01001	Party
01010	Vocal
01011	Hip-Hop
01100	Dialog
01101	Bass-boost #1
01110	Bass-boost #2
01111	Bass-boost #3
10000	Loudness 1
10001	Loudness 2
10010	Loudness 3
10011	Loudness 4
10100	Loudness 5
10101	Loudness 6
10110	Loudness 7
10111	Loudness 8
11000	Loudness 9
11001	Loudness 10
11010	Loudness 11
11011	Loudness 12
11100	Loudness 13
11101	Loudness 14
11110	Loudness 15
11111	Loudness 16

8.2.36 AGEQ - graphic EQ 80-Hz band (0x23)

D7	D6	D5	D4	D3	D2	D1	D0
			AGEQ4	AGEQ3	AGEQ2	AGEQ1	AGEQ0
			0	1	1	1	1

8.2.37 BGEQ - graphic EQ 300-Hz band (0x24)

D7	D6	D5	D4	D3	D2	D1	D0
			BGEQ4	BGEQ3	BGEQ2	BGEQ1	BGEQ0
			0	1	1	1	1

8.2.38 CGEQ - graphic EQ 1-kHz band (0x25)

D7	D6	D5	D4	D3	D2	D1	D0
			CGEQ4	CGEQ3	CGEQ2	CGEQ1	CGEQ0
			0	1	1	1	1

8.2.39 DGEQ - graphic EQ 3-kHz band (0x26)

D7	D6	D5	D4	D3	D2	D1	D0
			DGEQ4	DGEQ3	DGEQ2	DGEQ1	DGEQ0
			0	1	1	1	1

8.2.40 EGEQ - graphic EQ 8-kHz band (0x27)

D7	D6	D5	D4	D3	D2	D1	D0
			EGEQ4	EGEQ3	EGEQ2	EGEQ1	EGEQ0
			0	1	1	1	1

xGEQ[4:0]	Boost / cut
11111	+16
11110	+15
11101	+14
…	…
10000	+1
01111	0
01110	-1
…	…
00001	-14
00000	-15

8.2.41 Biquad internal channel loop-through (0x28)

D7	D6	D5	D4	D3	D2	D1	D0
C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP
0	0	0	0	0	0	0	0

Each internal processing channel can receive two possible inputs at the input to the biquad block. The input can come either from the output of that channel's MIX#1 engine or from the output of the bass/treble (biquad #10) of the previous channel. In this scenario, channel 1 receives channel 8. This enables the use of more than 10 biquads on any given channel at the loss of the number of separate internal processing channels.

Bit	RW	RST	Name	Description
7:0	RW	0	CnBLP	For n = 1 to 8: 0: input from channel n MIX#1 engine output - normal operation 1: input from channel (n - 1) biquad #10 output - loop operation.

8.2.42 Mix internal channel loop-through (0x29)

D7	D6	D5	D4	D3	D2	D1	D0
C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
0	0	0	0	0	0	0	0

Each internal processing channel can receive two possible sets of inputs at the input to the Mix#1 block. The inputs can come from the outputs of the interpolation block as normally occurs (CnMXLP = 0) or they can come from the outputs of the Mix#2 block. This enables the use of additional filtering after the second mix block at the expense of losing this processing capability on the channel.

Bit	RW	RST	Name	Description
7:0	RW	0	CnMXLP	For n = 1 to 8: 0: inputs to channel n MIX#1 engine from interpolation outputs - normal operation 1: inputs to channel n MIX#1 engine from MIX#2 engine outputs - loop operation

8.2.43 EQ bypass (0x2A)

D7	D6	D5	D4	D3	D2	D1	D0
C8EQBP	C7EQBP	C6EQBP	C5EQBP	C4EQCBP	C3EQBP	C2EQBP	C1EQBP
0	0	0	0	0	0	0	0

EQ control can be bypassed on a per-channel basis. If EQ control is bypassed on a given channel, the prescale and all 10 filters (high-pass, biquads, de-emphasis, bass management cross-over, bass, treble in any combination) are bypassed for that channel.

Bit	RW	RST	Name	Description
7:0	RW	0	CnEQBP	For n = 1 to 8: 0: perform EQ on channel n - normal operation 1: bypass EQ on channel n

8.2.44 Tone control bypass (0x2B)

D7	D6	D5	D4	D3	D2	D1	D0
C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
0	0	0	0	0	0	0	0

Tone control (bass/treble) can be bypassed on a per-channel basis. If tone control is bypassed on a given channel, the two filters that tone control utilizes are made available as user-programmable biquads #9 and #10.

8.2.45 Tone control (0x2C)

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

This is the tone control boost / cut as a function of the BTC and TTC bits.

BTC[3:0] / TTC[3:0)	Boost / cut
0000	-12 dB
0001	-12 dB
…	…
0111	-4 dB
0110	-2 dB
0111	0 dB
1000	+2 dB
1001	+4 dB
…	…
1101	+12 dB
1110	+12 dB
1111	+12dB

8.2.46 Channel limiter select channels 1, 2, 3, 4 (0x2D)

D7	D6	D5	D4	D3	D2	D1	D0
C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
0	0	0	0	0	0	0	0

8.2.47 Channel limiter select channels 5, 6, 7, 8 (0x2E)

D7	D6	D5	D4	D3	D2	D1	D0
C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
0	0	0	0	0	0	0	0

8.2.48 Limiter 1 attack/release rate (0x2F)

D7	D6	D5	D4	D3	D2	D1	D0
L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0	1	1	0	1	0	1	0

8.2.49 Limiter 1 attack/release threshold (0x30)

D7	D6	D5	D4	D3	D2	D1	D0
L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0	1	1	0	1	0	0	1

8.2.50 Limiter 2 attack/release rate (0x31)

D7	D6	D5	D4	D3	D2	D1	D0
L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0	1	1	0	1	0	1	0

8.2.51 Limiter 2 attack/release threshold (0x32)

D7	D6	D5	D4	D3	D2	D1	D0
L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0	1	1	0	1	0	0	1

8.2.52 Bit description

The STA311B includes two independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anti-clipping mode or to actively reduce the dynamic range for a better listening environment such as a nighttime listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in configuration register B, bit 7 address 0x02. Each channel can be mapped to either limiter or not mapped, meaning that channel will clip when

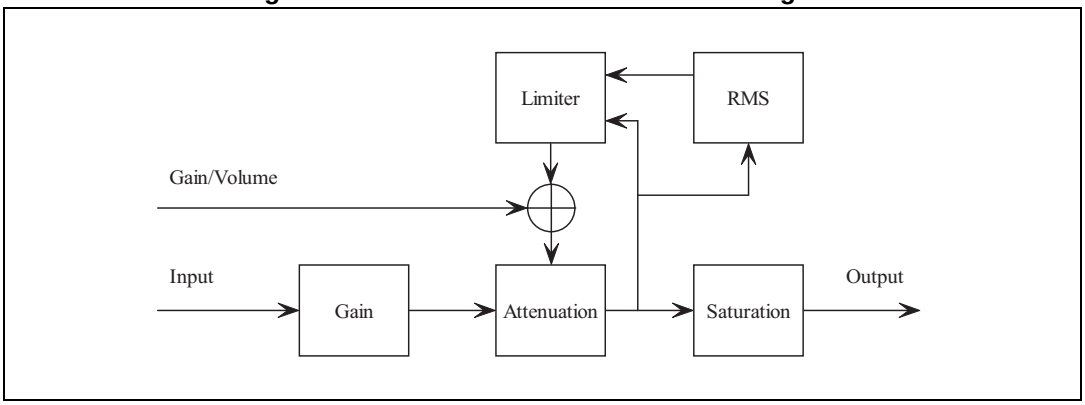
0 dBFS is exceeded. Each limiter will look at the present value of each channel that is mapped to it, select the maximum absolute value of all these channels, perform the limiting algorithm on that value, and then, if needed, adjust the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LnAT registers. It is recommended in anti-clipping mode to set this to 0 dBFS, which corresponds to the maximum unclipped output power of an FFX amplifier. Since gain can be added digitally within the STA311B it is possible to exceed 0 dBFS or any other LnAT setting. When this occurs, the limiter, when active, will automatically start reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. The gain reduction occurs on a peak-detect algorithm.

The release of the limiter, when the gain is again increased, is dependent on an RMS-detect algorithm. The output of the volume/limiter block is passed through an RMS filter. The output of this filter is compared to the release threshold, determined by the release threshold register. When the RMS filter output falls below the release threshold, the gain is again increased at a rate dependent upon the release rate register. The gain can never be increased past its set value and therefore the release will only occur if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as overlimiting can reduce the dynamic range to virtually zero and cause program material to sound lifeless.

In AC mode the attack and release thresholds are set relative to full-scale. In DRC mode the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

Figure 9. Basic limiter and volume flow diagram



CnLS[1,0]	Channel limiter mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

LnA[3:0]	Attack rate (dB/ms)
0000	3.1584 (fast)
0001	2.7072
0010	2.2560
0011	1.8048
0100	1.3536
0101	0.9024
0110	0.4512
0111	0.2256
1000	0.1504
1001	0.1123
1010	0.0902
1011	0.0752
1100	0.0645
1101	0.0564
1110	0.0501
1111	0.0451 (slow)

LnR[3:0]	Release rate (dB/ms)
0000	0.5116 (fast)
0001	0.1370
0010	0.0744
0011	0.0499
0100	0.0360
0101	0.0299
0110	0.0264
0111	0.0208
1000	0.0198
1001	0.0172
1010	0.0147
1011	0.0137
1100	0.0134
1101	0.0117
1110	0.0110
1111	0.0104 (slow)

LnAT[3:0]	Anti-clipping (AC) (dB relative to FS)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

LnRT[3:0]	Anti-clipping (AC) (dB relative to FS)
0000	-∞
0001	-29 dB
0010	-20 dB
0011	-16 dB
0100	-14 dB
0101	-12 dB
0110	-10 dB
0111	-8 dB
1000	-7 dB
1001	-6 dB
1010	-5 dB
1011	-4 dB
1100	-3 dB
1101	-2 dB
1110	-1 dB
1111	-0 dB

LnAT[3:0]	Dynamic range compression (DRC) (dB relative to volume)
0000	-31
0001	-29
0010	-27
0011	-25
0100	-23
0101	-21
0110	-19
0111	-17
1000	-16
1001	-15
1010	-14
1011	-13
1100	-12
1101	-10
1110	-7
1111	-4

LnRT[3:0]	Dynamic range compression (DRC) (db relative to volume + LnAT)
0000	-∞
0001	-38 dB
0010	-36 dB
0011	-33 dB
0100	-31 dB
0101	-30 dB
0110	-28 dB
0111	-26 dB
1000	-24 dB
1001	-22 dB
1010	-20 dB
1011	-18 dB
1100	-15 dB
1101	-12 dB
1110	-9 dB
1111	-6 dB

8.2.53 Channel 1 and 2 output timing (0x33)

D7	D6	D5	D4	D3	D2	D1	D0
	C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
	1	0	0		0	0	0

8.2.54 Channel 3 and 4 output timing (0x34)

D7	D6	D5	D4	D3	D2	D1	D0
	C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
	1	1	0		0	1	0

8.2.55 Channel 5 and 6 output timing (0x35)

D7	D6	D5	D4	D3	D2	D1	D0
	C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
	1	0	1		0	0	1

8.2.56 Channel 7 and 8 output timing (0x36)

D7	D6	D5	D4	D3	D2	D1	D0
	C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
	1	1	1		0	1	1

The centering of the individual channel PWM output periods can be adjusted by the output timing registers. The PWM slot settings can be chosen to ensure that pulse transitions do not occur at the same time on different channels using the same power device. There are 8 possible settings, the appropriate setting varies based on the application and connections to the FFX power devices.

CnOT[2:0]	PWM slot
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

8.2.57 Channel I²S output mapping channels 1 and 2 (0x37)

D7	D6	D5	D4	D3	D2	D1	D0
	C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0
	0	0	1		0	0	0

8.2.58 Channel I²S output mapping channels 3 and 4 (0x38)

D7	D6	D5	D4	D3	D2	D1	D0
	C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
	0	1	1		0	1	0

8.2.59 Channel I²S output mapping channels 5 and 6 (0x39)

D7	D6	D5	D4	D3	D2	D1	D0
	C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
	1	0	1		1	0	0

8.2.60 Channel I²S output mapping channels 7 and 8 (0x3A)

D7	D6	D5	D4	D3	D2	D1	D0
	C8OM2	C8M1	C8OM0		C7OM2	C7OM1	C7OM0
	1	1	1		1	1	0

Each I²S output channel can receive data from any channel output of the volume block. Which channel a particular I²S output receives is dependent upon that channel's CnOM register bits.

CnOM[2:0]	Serial output from
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6
110	Channel 7
111	Channel 8

8.2.61 Coefficient address register 1 (0x3B)

D7	D6	D5	D4	D3	D2	D1	D0
						CFA9	CFA8
						0	0

8.2.62 Coefficient address register 2 (0x3C)

D7	D6	D5	D4	D3	D2	D1	D0
CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0	0	0	0	0	0	0	0

8.2.63 Coefficient b1 data register, bits 23:16 (0x3D)

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

8.2.64 Coefficient b1 data register, bits 15:8 (0x3E)

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

8.2.65 Coefficient b1 data register, bits 7:0 (0x3F)

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

8.2.66 Coefficient b2 data register, bits 23:16 (0x40)

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

8.2.67 Coefficient b2 data register, bits 15:8 (0x41)

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

8.2.68 Coefficient b2 data register, bits 7:0 (0x42)

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

8.2.69 Coefficient a1 data register, bits 23:16 (0x43)

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

8.2.70 Coefficient a1 data register, bits 15:8 (0x44)

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

8.2.71 Coefficient a1 data register, bits 7:0 (0x45)

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

8.2.72 Coefficient a2 data register, bits 23:16 (0x46)

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

8.2.73 Coefficient a2 data register, bits 15:8 (0x47)

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

8.2.74 Coefficient a2 data register, bits 7:0 (0x48)

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

8.2.75 Coefficient b0 data register, bits 23:16 (0x49)

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

8.2.76 Coefficient b0 data register, bits 15:8 (0x4A)

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

8.2.77 Coefficient b0 data register, bits 7:0 (0x4B)

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

8.2.78 Coefficient write control register (0x4C)

D7	D6	D5	D4	D3	D2	D1	D0
						WA	W1
						0	0

Coefficients for EQ and Bass Management are handled internally in the STA311B via RAM. Access to this RAM is available to the user via an I²C register interface.

A collection of I²C registers are dedicated to this function. One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the write of the coefficient(s) to RAM. The following are instructions for reading and writing coefficients.

8.3 Reading a coefficient from RAM

1. Write the top 2 bits of address to I²C register 0x3B
2. Write the bottom 8 bits of address to I²C register 0x3C
3. Read the top 8 bits of coefficient in I²C address 0x3D
4. Read the middle 8 bits of coefficient in I²C address 0x3E
5. Read the bottom 8 bits of coefficient in I²C address 0x3F

8.4 Reading a set of coefficients from RAM

1. Write the top 2 bits of address to I²C register 0x3B
2. Write the bottom 8 bits of address to I²C register 0x3C
3. Read the top 8 bits of coefficient in I²C address 0x3D
4. Read the middle 8 bits of coefficient in I²C address 0x3E
5. Read the bottom 8 bits of coefficient in I²C address 0x3F
6. Read the top 8 bits of coefficient b2 in I²C address 0x40
7. Read the middle 8 bits of coefficient b2 in I²C address 0x41
8. Read the bottom 8 bits of coefficient b2 in I²C address 0x42
9. Read the top 8 bits of coefficient a1 in I²C address 0x43
10. Read the middle 8 bits of coefficient a1 in I²C address 0x44
11. Read the bottom 8 bits of coefficient a1 in I²C address 0x45
12. Read the top 8 bits of coefficient a2 in I²C address 0x46
13. Read the middle 8 bits of coefficient a2 in I²C address 0x47
14. Read the bottom 8 bits of coefficient a2 in I²CI²C address 0x48
15. Read the top 8 bits of coefficient b0 in I²C address 0x49
16. Read the middle 8 bits of coefficient b0 in I²C address 0x4A
17. Read the bottom 8 bits of coefficient b0 in I²C address 0x4B

8.5 Writing a single coefficient to RAM

1. Write the top 2 bits of address to I²C register 0x3B
2. Write the bottom 8 bits of address to I²C register 0x3C
3. Write the top 8 bits of coefficient in I²C address 0x3D
4. Write the middle 8 bits of coefficient in I²C address 0x3E
5. Write the bottom 8 bits of coefficient in I²C address 0x3F
6. Write 1 to the W1 bit in I²C address 0x4C

8.6 Writing a set of coefficients to RAM

1. Write the top 2 bits of starting address to I²C register 0x3B
2. Write the bottom 8 bits of starting address to I²C register 0x3C
3. Write the top 8 bits of coefficient b1 in I²C address 0x3D
4. Write the middle 8 bits of coefficient b1 in I²C address 0x3E
5. Write the bottom 8 bits of coefficient b1 in I²C address 0x3F
6. Write the top 8 bits of coefficient b2 in I²C address 0x40
7. Write the middle 8-bits of coefficient b2 in I²C address 0x41
8. Write the bottom 8 bits of coefficient b2 in I²C address 0x42
9. Write the top 8 bits of coefficient a1 in I²C address 0x43
10. Write the middle 8 bits of coefficient a1 in I²C address 0x44
11. Write the bottom 8 bits of coefficient a1 in I²C address 0x45
12. Write the top 8 bits of coefficient a2 in I²C address 0x46
13. Write the middle 8 bits of coefficient a2 in I²C address 0x47
14. Write the bottom 8 bits of coefficient a2 in I²C address 0x48
15. Write the top 8-bits of coefficient b0 in I²C address 0x49
16. Write the middle 8 bits of coefficient b0 in I²C address 0x4A
17. Write the bottom 8 bits of coefficient b0 in I²C address 0x4B
18. Write 1 to the WA bit in I²C address 0x4C

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side-effects.

When using this technique, the 10-bit address would specify the address of the biquad b1 coefficient (for example, decimals 0, 5, 10, 15, …, 100, … 395), and the STA311B will generate the RAM addresses as offsets from this base value to write the complete set of coefficient data.

9 Configuration registers (0x77; 0x78; 0x79)

CBQ1 (reg 0x77)

D7	D6	D5	D4	D3	D2	D1	D0
EBQ3_1	EBQ3_0	EBQ2_1	EBQ2_0	EBQ1_1	EBQ1_0	EBQ0_0	EBQ0_0
0	0	0	0	0	0	0	0

CBQ2 (reg 0x78)

D7	D6	D5	D4	D3	D2	D1	D0
EBQ7_1	EBQ7_0	EBQ6_1	EBQ6_0	EBQ5_1	EBQ5_0	EBQ4_1	EBQ4_0
0	0	0	0	0	0	0	0

CBQ3 (reg 0x79)

D7	D6	D5	D4	D3	D2	D1	D0
			nshen	EBQ9_1	EBQ9_0	EBQ8_1	EBQ8_0
0	0	0	1	0	0	0	0

The STA311B EQ biquads use the following equation:

$Y[n] = 2 * (b_0 / 2) * X[n] + 2 * (b_1 / 2) * X[n-1] + b_2 * X[n-2] - 2 * (a_1 / 2) * Y[n-1] - a_2 * Y[n-2]$

$= b_0 * X[n] + b_1 * X[n-1] + b_2 * X[n-2] - a_1 * Y[n-1] - a_2 * Y[n-2]$

where Y[n] represents the output and X[n] represents the input. Multipliers are 24-bit signed fractional multipliers, with coefficient values in the range of 0x800000 (-1) to 0x7FFFFF (0.9999995231628). The default coefficient range (+/-1) can be reconfigured to ±2 or ±4 with the 0x77, 0x78 and 0x79 I²C registers. The coefficients range setting is common for all the channels.

- (EBQx_1;EBQx_0)=”00”: Biquad x use +/-1 range
- (EBQx_1;EBQx_0)=”01”: Biquad x use +/-2 range
- (EBQx_1;EBQx_0)=”10”: Biquad x use +/-4 range
- (EBQx_1;EBQx_0)=”11”: reserved

Coefficients stored in the user-defined coefficient RAM are referenced in the following manner:

$CxHy0 = b_1 / 2$

$CxHy1 = b_2$

$CxHy2 = -a_1 / 2$

$CxHy3 = -a_2$

$CxHy4 = b_0 / 2$

where x represents the channel and the y the biquad number. For example, C0H41 is the b_2 coefficient in the fourth biquad for channel 2.

By default, all user-defined filters are pass-through where all coefficients are set to 0, except the $b_0/2$ coefficient which is set to 0x400000 (representing 0.5). Mix coefficients use only ±1 range.

A special feature inside the digital processing block is available (active when the ashen bit is set to '1'). In case of poles positioned at very low frequencies, biquads filters can generate some audible quantization noise or unwanted DC level. In order to avoid this kind of effect a quantization noise-shaping capability can be used. The filter structure including this special feature, relative to each biquad is shown in *Figure 10*.

The new feature can be enabled independently for each biquad using the I²C registers. The D7 bit, when set, is responsible for activating this function on the crossover filter while the other bits address any specific biquads according to the previous table. Channels 1 and 2 share the same settings. Bit D7 is effective also for channel 3 if the related OCFG is used.

Figure 10. Biquad filter structure with quantization error noise shaping

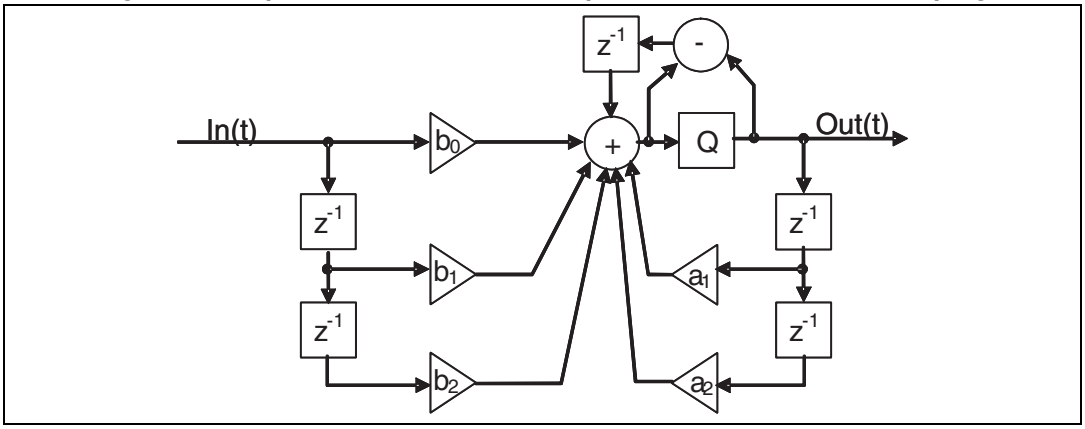
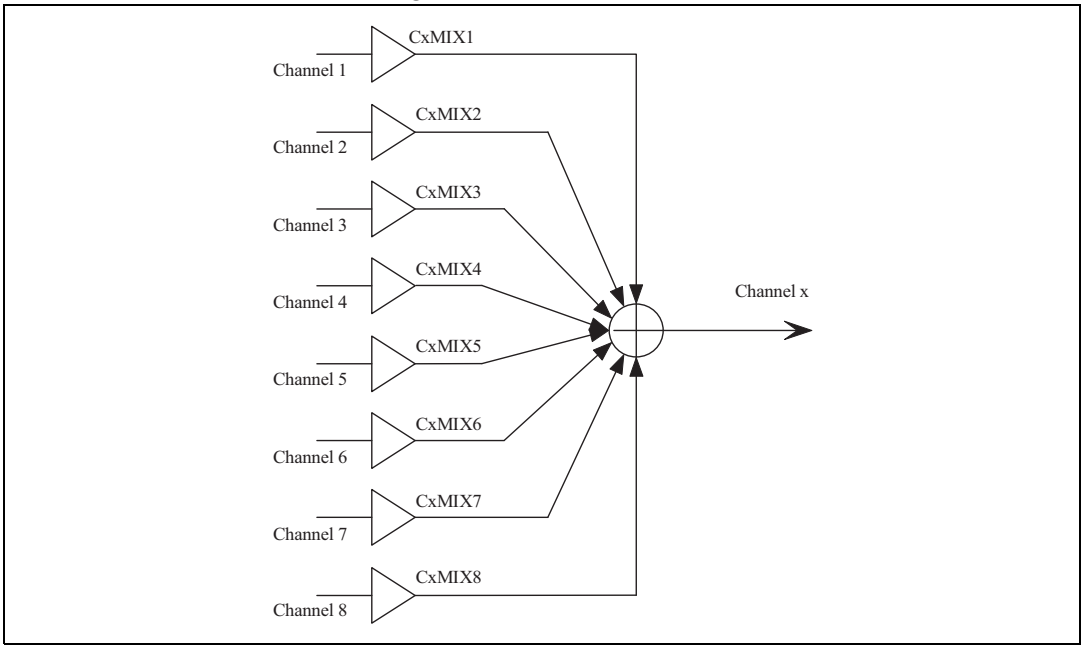


Figure 11. Channel mixer



9.1 Post-scale

The STA311B provides one additional multiplication after the last interpolation stage and before the distortion compensation on each channel. This is a 24-bit signed fractional multiply.

The scale factor for this multiply is loaded into RAM using the same I²C registers as the biquad coefficients and the bass-management.

This post-scale factor can be used in conjunction with an ADC-equipped microcontroller to perform power-supply error correction. All channels can use the channel 1 by setting the post-scale link bit.

Table 14. RAM block for biquads, mixing, and bass management

Index (decimal)	Index (hex)		Coefficient	Default
0	0x00	Channel 1 - Biquad 1	C1H10 (b1/2)	0x000000
1	0x01		C1H11 (b2)	0x000000
2	0x02		C1H12 (a1/2)	0x000000
3	0x03		C1H13 (a2)	0x000000
4	0x04		C1H14 (b0/2)	0x400000
5	0x05	Channel 1 - Biquad 2	C1H20	0x000000
…	…	…	…	…
49	0x31	Channel 1 - Biquad 10	C1HA4	0x400000
50	0x32	Channel 2 - Biquad 1	C2H10	0x000000
51	0x33		C2H11	0x000000
…	…	…	…	…
99	0x63	Channel 2 - Biquad 10	C2HA4	0x4000000
100	0x64	Channel 3 - Biquad 1	C3H10	0x000000
…	…	…	…	…
399	0x18F	Channel 8 - Biquad 10	C8HA4	0x400000
400	0x190	Channel 1 - Pre-scale	C1PreS	0x7FFFFF
401	0x191	Channel 2 - Pre-scale	C2PreS	0x7FFFFF
402	0x192	Channel 3 - Pre-scale	C3PreS	0x7FFFFF
…	…	…	…	…
407	0x197	Channel 8 - Pre-scale	C8PreS	0x7FFFFF
408	0x198	Channel 1 - Post-scale	C1PstS	0x7FFFFF
409	0x199	Channel 2 - Post-scale	C2PstS	0x7FFFFF
…	…	…	…	…
415	0x19F	Channel 8 - Post-scale	C8PstS	0x7FFFFF
416	0x1A0	Channel 1 - Mix# 1 1	C1MX11	0x7FFFFF
417	0x1A1	Channel 1 - Mix#1 2	C1MX12	0x000000

Table 14. RAM block for biquads, mixing, and bass management (continued)

Index (decimal)	Index (hex)		Coefficient	Default
…	…	…	…	…
423	0x1A7	Channel 1 - Mix#1 8	C1MX18	0x000000
424	0x1A8	Channel 2 - Mix#1 1	C2MX11	0x000000
425	0x1A9	Channel 2 - Mix#1 2	C2MX12	0x7FFFFF
…	…	…	…	…
479	0x1DF	Channel 8 - Mix#1 8	C8MX18	0x7FFFFF
480	0x1E0	Channel 1 - Mix#2 1	C1MX21	0x7FFFFF
481	0x1E1	Channel 1 - Mix#2 2	C1MX22	0x000000
…	…	…	…	…
487	0x1E7	Channel 1 - Mix#2 8	C1MX28	0x000000
488	0x1E8	Channel 2 - Mix#2 1	C2MX21	0x000000
489	0x1E9	Channel 2 - Mix#2 2	C2MX22	0x7FFFFF
…	…	…	…	…
543	0x21F	Channel 8 - Mix#2 8	C8MX28	0x7FFFFF

9.2 Variable max power correction

9.2.1 MPCC1-2 (0x4D, 0x4E)

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

D7	D6	D5	D4	D3	D2	D1	D0
MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0	0	1	0	1	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
1	1	0	0	0	0	0	0

9.3 Variable distortion compensation

9.3.1 DCC1-2 (0x4F, 0x50)

The DCC bits determine the 16 MSBs of the distortion compensation coefficient. This coefficient is used in place of the default coefficient when DCCV = 1.

D7	D6	D5	D4	D3	D2	D1	D0
DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
1	1	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0	0	1	1	0	0	1	1

9.4 PSCorrect registers

An ADC is used to input ripple data to SDI78. The left channel (7) is used internally. No audio data can therefore be used on these channels, although all channel mapping and mixing from other inputs to channels 7 and 8 internally are still valid.

9.4.1 PSC1-2: ripple correction value (RCV) (0x51, 0x52)

This value is equivalent to the negative maximum ripple peak as a percentage of Vcc (MPR), scaled by the inverse of the maximum ripple p-p as a percentage of the full-scale analog input to the ADC. It is represented as a 1.11 signed fractional number.

D7	D6	D5	D4	D3	D2	D1	D0
RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
RCV3	RCV2	RCV1	RCV0	CNV11	CNV10	CNV9	CNV8
0	0	0	0	1	1	1	1

9.4.2 PSC3: correction normalization value (CNV) (0x53)

This value is equivalent to 1 / (1+MPR) expressed as a 0.12 unsigned fractional number.

D7	D6	D5	D4	D3	D2	D1	D0
CNV7	CNV6	CNV5	CNV4	CNV3	CNV2	CNV1	CNV0
1	1	1	1	1	1	1	1

9.5 Extended DRC configuration registers

9.5.1 Extended limiter/dynamic range control LUT (NLENAR)(0x5A)

An extended limiter/DRC LUT has been implemented to provide incremental steps of 0.25/0.50 dB. To enable this feature the NLENAR bit has to be set, refer to the following tables.

D7	D6	D5	D4	D3	D2	D1	D0
							NLENAR
							0

Bit	RW	RST	Name	Description
0	RW	0	NLENAR	Enables a new limiter/DRC LUT 0: Extended LUT disabled 1: Extended LUT enabled

9.5.2 Extended limiter/dynamic range LUT registers (nLxAT/RT) (0x6B, 0x6C, 0x6D, 0x6E)

nL1at (0x6B)

D7	D6	D5	D4	D3	D2	D1	D0
	L1AT6	L1AT5	L1AT4	L1AT3	L1AT2	L1AT1	L1AT0
0	0	1	1	0	0	0	0

nL2at (0x6C)

D7	D6	D5	D4	D3	D2	D1	D0
	L2AT6	L2AT5	L2AT4	L2AT3	L2AT2	L2AT1	L2AT0
0	0	1	1	0	0	0	0

nL1rt (0x6D)

D7	D6	D5	D4	D3	D2	D1	D0
		L1RT5	L1RT4	L1RT3	L1RT2	L1RT1	L1RT0
0	0	1	0	1	1	1	1

nL2rt (0x6E)

D7	D6	D5	D4	D3	D2	D1	D0
		L2RT5	L2RT4	L2RT3	L2RT2	L2RT1	L2RT0
0	0	1	0	1	1	1	1

Table 15. Extended release thresholds (AC mode)

LnRT[5:0]	Anti-clipping(AC) (dB relative to full scale)
000000	-∞
000001	-29.00
000010	-28.50
000011	-28.00
000100	-27.50
000101	-27.00
000110	-26.50
000111	-26.00
001000	-25.50
001001	-25.00
001010	-24.50

Table 15. Extended release thresholds (AC mode) (continued)

LnRT[5:0]	Anti-clipping(AC) (dB relative to full scale)
001011	-24.00
001100	-23.50
001101	-23.00
001110	-22.50
001111	-22.00
010000	-21.50
010001	-21.00
010010	-20.50
010011	-20.00
010100	-19.50
010101	-19.00
010110	-18.50
010111	-18.00
011000	-17.50
011001	-17.00
011010	-16.50
011011	-16.00
011100	-15.50
011101	-15.00
011110	-14.50
011111	-14.00
100000	-13.50
100001	-13.00
100010	-12.50
100011	-12.00
100100	-11.50
100101	-11.00
100110	-10.50
100111	-10.00
101000	-9.50
101001	-9.00
101010	-8.50
101011	-8.00
101100	-7.50

Table 15. Extended release thresholds (AC mode) (continued)

LnRT[5:0]	Anti-clipping(AC) (dB relative to full scale)
101101	-7.00
101110	-6.50
101111	-6.00
110000	-5.50
110001	-5.00
110010	-4.50
110011	-4.00
110100	-3.50
110101	-3.00
110110	-2.50
110111	-2.00
111000	-1.50
111001	-1.00
111010	-0.50
OTHERS	0.00

Table 16. Extended attack thresholds (AC mode)

LnAT[6:0]	Anti-clipping (AC) (dB relative to volume)
0000000	-12.00
0000001	-11.75
0000010	-11.50
0000011	-11.25
0000100	-11.00
0000101	-10.75
0000110	-10.50
0000111	-10.25
0001000	-10.00
0001001	-9.75
0001010	-9.50
0001011	-9.25
0001100	-9.00
0001101	-8.75
0001110	-8.50

Table 16. Extended attack thresholds (AC mode) (continued)

LnAT[6:0]	Anti-clipping (AC) (dB relative to volume)
0001111	-8.25
0010000	-8.00
0010001	-7.75
0010010	-7.50
0010011	-7.25
0010100	-7.00
0010101	-6.75
0010110	-6.50
0010111	-6.25
0011000	-6.00
0011001	-5.75
0011010	-5.50
0011011	-5.25
0011100	-5.00
0011101	-4.75
0011110	-4.50
0011111	-4.25
0100000	-4.00
0100001	-3.75
0100010	-3.50
0100011	-3.25
0100100	-3.00
0100101	-2.75
0100110	-2.50
0100111	-2,25
0101000	-2.00
0101001	-1.75
0101010	-1.50
0101011	-1.25
0101100	-1.00
0101101	-0.75
0101110	-0.50
0101111	-0.25
0110000	0.00

Table 16. Extended attack thresholds (AC mode) (continued)

LnAT[6:0]	Anti-clipping (AC) (dB relative to volume)
0110001	+0.25
0110010	+0.50
0110011	+0.75
0110100	+1.00
0110101	+1.25
0110110	+1.50
0110111	+1.75
0111000	+2.00
0111001	+2.25
0111010	+2.50
0111011	+2.75
0111100	+3.00
0111101	+3.25
0111110	+3.50
0111111	+3.75
1000000	+4.00
1000001	+4.25
1000010	+4.50
1000011	+4.75
1000100	+5.00
1000101	+5.25
1000110	+5.50
1000111	+5.75
1001000	+6.00
1001001	+6.25
1001010	+6.50
1001011	+6.75
1001100	+7.00
1001101	+7.25
1001110	+7.50
1001111	+7.75
1010000	+8.00
1010001	+8.25
1010010	+8.50

Table 16. Extended attack thresholds (AC mode) (continued)

LnAT[6:0]	Anti-clipping (AC) (dB relative to volume)
1010011	+8.75
1010100	+9.00
1010101	+9.25
1010110	+9.50
1010111	+9.75
OTHERS	+10.00

Table 17. Extended attack thresholds (DRC mode)

LnAT[6:0]	Dynamic range compression (DRC) (dB relative to volume)
0000000	-31.00
0000001	-30.50
0000010	-30.00
0000011	-29.50
0000100	-29.00
0000101	-28.50
0000110	-28.00
0000111	-27.50
0001000	-27.00
0001001	-26.50
0001010	-26.00
0001011	-25.50
0001100	-25.00
0001101	-24.50
0001110	-24.00
0001111	-23.50
0010000	-23.00
0010001	-22.50
0010010	-22.00
0010011	-21.50
0010100	-21.00
0010101	-20.50
0010110	-20.00
0010111	-19.50

Table 17. Extended attack thresholds (DRC mode) (continued)

LnAT[6:0]	Dynamic range compression (DRC) (dB relative to volume)
0011000	-19.00
0011001	-18.50
0011010	-18.00
0011011	-17.50
0011100	-17.00
0011101	-16.50
0011110	-16.00
0011111	-15.50
0100000	-15.00
0100001	-14.50
0100010	-14.00
0100011	-13.50
0100100	-13.00
0100101	-12.50
0100110	-12.00
0100111	-11.50
0101000	-11.00
0101001	-10.50
0101010	-10.00
0101011	-9.50
0101100	-9.00
0101101	-8.50
0101110	-8.00
0101111	-7.50
0110000	-7.00
0110001	-6.50
0110010	-6.00
0110011	-5.50
0110100	-5.00
0110101	-4.50
OTHERS	-4.00

Table 18. Extended release thresholds (DRC mode)

LnRT[5:0]	Dynamic range compression (DRC) (dB relative to volume)
000000	-inf
000001	-38.00
000010	-37.50
000011	-37.00
000100	-36.50
000101	-36.00
000110	-35.50
000111	-35.00
001000	-34.50
001001	-34.00
001010	-33.50
001011	-33.00
001100	-32.50
001101	-32.00
001110	-31.50
001111	-31.00
010000	-30.50
010001	-30.00
010010	-29.50
010011	-29.00
010100	-28.50
010101	-28.00
010110	-27.50
010111	-27.00
011000	-26.50
011001	-26.00
011010	-25.50
011011	-25.00
011100	-24.50
011101	-24.00
011110	-23.50
011111	-23.00
100000	-22.50
100001	-22.00

Table 18. Extended release thresholds (DRC mode) (continued)

LnRT[5:0]	Dynamic range compression (DRC) (dB relative to volume)
100010	-21.50
100011	-21.00
100100	-20.50
100101	-20.00
100110	-19.50
100111	-19.00
101000	-18.50
101001	-18.00
101010	-17.50
101011	-17.00
101100	-16.50
101101	-16.00
101110	-15.50
101111	-15.00
110000	-14.50
110001	-14.00
110010	-13.50
110011	-13.00
110100	-12.50
110101	-12.00
110110	-11.50
110111	-11.00
111000	-10.50
111001	-10.00
111010	-9.50
111011	-9.00
111100	-8.50
111101	-8.00
111110	-7.50
111111	-7.00
OTHERS	-6.00

9.5.3 Recombination control register 1 (0x5D)

D7	D6	D5	D4	D3	D2	D1	D0
Boost6db			I²S_byp	I²S_en	mike_en	mike_byp	m_mode
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
7	RW	0	Boost6dB(1)	'1': Output (after recombination) multiplied x2 '0': Output (after recombination) as it is
6	RW	0		
5	RW	0		
4	RW	0	I²S_byp	'1': I²S recombination is bypassed '0': I²S recombination is used
3	RW	0	I²S_en	'1': I²S recombination IP is active '0': I²S recombination IP is not active (acts like a HW bypass)
0	RW	0	m_mode	'1': Auto-configuration of the CKOUT generator to Fout = sys_clk/32 '0': CKOUT is configured only through COS bits

1. Mike recomb only

Table 19. Gain adjustment (sensitivity)

Index	dB	Index	dB	Index	dB
0x00	-4	0x16	-1.25	0x2C	1.5
0x01	-3.875	0x17	-1.125	0x2D	1.625
0x02	-3.75	0x18	-1	0x2E	1.75
0x03	-3.625	0x19	-0.875	0x2F	1.875
0x04	-3.5	0x1A	-0.75	0x30	2
0x05	-3.375	0x1B	-0.625	0x31	2.125
0x06	-3.25	0x1C	-0.5	0x32	2.25
0x07	-3.125	0x1D	-0.375	0x33	2.375
0x08	-3	0x1E	-0.25	0x34	2.5
0x09	-2.875	0x1F	-0.125	0x35	2.625
0x0A	-2.75	0x20	0	0x36	2.75
0x0B	-2.625	0x21	0.125	0x37	2.875
0x0C	-2.5	0x22	0.25	0x38	3
0x0D	-2.375	0x23	0.375	0x39	3.125
0x0E	-2.25	0x24	0.5	0x3A	3.25
0x0F	-2.125	0x25	0.625	0x3B	3.375
0x10	-2	0x26	0.75	0x3C	3.5
0x11	-1.875	0x27	0.875	0x3D	3.625
0x12	-1.75	0x28	1	0x3E	3.75
0x13	-1.625	0x29	1.125	0x3F	3.875
0x14	-1.5	0x2A	1.25		
0x15	-1.375	0x2B	1.375		

9.5.4 Recombination control register 5, 6 and 7 (0x62; 0x63; 0x64)

D7	D6	D5	D4	D3	D2	D1	D0
	LP1en	CH1NCA[5:0]					
0	1	1	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
	LP2en	CH2NCA[5:0]					
0	1	1	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
	LP3en	CH3NCA[5:0]					
0	1	1	0	0	0	0	0

Bit	RW	RST	Name	Description
7	RW			
6	RW		LPxen	'1': Low-pass filter of mike x is enabled '0': Low-pass filter of mike x is not enabled
5	RW		CHxNCA[5:0]	see *Table 20*
4	RW			
3	RW			
2	RW			
1	RW			
0	RW			

Table 20. Normal channel attenuation

Index	dB	Index	dB	Index	dB
0x00	0	0x16	18.75	0x2C	21.5
0x01	10.5	0x17	18.875	0x2D	21.625
0x02	11	0x18	19	0x2E	21.75
0x03	11.5	0x19	19.125	0x2F	21.875
0x04	12	0x1A	19.25	0x30	22
0x05	12.5	0x1B	19.375	0x31	22.5
0x06	13	0x1C	19.5	0x32	23
0x07	13.5	0x1D	19.625	0x33	23.5
0x08	14	0x1E	19.75	0x34	24
0x09	14.5	0x1F	19.875	0x35	24.5
0x0A	15	0x20	20	0x36	25
0x0B	15.5	0x21	20.125	0x37	25.5
0x0C	16	0x22	20.25	0x38	26
0x0D	16.5	0x23	20.375	0x39	26.5
0x0E	17	0x24	20.5	0x3A	27
0x0F	17.5	0x25	20.625	0x3B	27.5
0x10	18	0x26	20.75	0x3C	28
0x11	18.125	0x27	20.875	0x3D	28.5
0x12	18.25	0x28	21	0x3E	29
0x13	18.375	0x29	21.125	0x3F	29.5
0x14	18.5	0x2A	21.25		
0x15	18.625	0x2B	21.375		

9.5.5 Recombination control register 8, 9 and 10 (0x65; 0x66; 0x67)

D7	D6	D5	D4	D3	D2	D1	D0
		CH1TH_N[5:0]					
0	0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
		CH2TH_N[5:0]					
0	0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
		CH3TH_N[5:0]					
0	0	1	1	0	0	1	1

Bit	RW	RST	Name	Description
7	RW			Reserved
6	RW			
5	RW		CHxTH_N[5:0]	see *Table 21*
4	RW			
3	RW			
2	RW			
1	RW			
0	RW			

Table 21. Threshold configuration

Index	dB	Index	dB	Index	dB	Index	dB	Index	dB	Index	dB
0x00	0	0x0B	-11	0x16	-22	0x21	-33	0x2C	-44	0x37	-55
0x01	-1	0x0C	-12	0x17	-23	0x22	-34	0x2D	-45	0x38	-56
0x02	-2	0x0D	-13	0x18	-24	0x23	-35	0x2E	-46	0x39	-57
0x03	-3	0x0E	-14	0x19	-25	0x24	-36	0x2F	-47	0x3A	-58
0x04	-4	0x0F	-15	0x1A	-26	0x25	-37	0x30	-48	0x3B	-59
0x05	-5	0x10	-16	0x1B	-27	0x26	-38	0x31	-49	0x3C	-60
0x06	-6	0x11	-17	0x1C	-28	0x27	-39	0x32	-50	0x3D	-61
0x07	-7	0x12	-18	0x1D	-29	0x28	-40	0x33	-51	0x3E	-62
0x08	-8	0x13	-19	0x1E	-30	0x29	-41	0x34	-52	0x3F	-63
0x09	-9	0x14	-20	0x1F	-31	0x2A	-42	0x35	-53		
0x0A	-10	0x15	-21	0x20	-32	0x2B	-43	0x36	-54		

9.5.6 Recombination control register 11, 12 and 13 (0x68; 0x69; 0x6A)

D7	D6	D5	D4	D3	D2	D1	D0
		CH1TH_H[5:0]					
0	0	0	1	1	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
		CH2TH_H[5:0]					
0	0	0	1	1	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
		CH3TH_H[5:0]					
0	0	0	1	1	0	1	1

Bit	RW	RST	Name	Description
7	RW	0		Reserved
6	RW	0		
5	RW	0	CHxHCT[5:0]	see *Table 21*
4	RW	1		
3	RW	1		
2	RW	0		
1	RW	1		
0	RW	1		

9.5.7 Zero-mute threshold/hysteresis and RMS zero-mute selectors (0x6F)

Zero-mute (0x6F)

D7	D6	D5	D4	D3	D2	D1	D0
RMSZS2	RMSZS1	RMSZS0	ZMTHS2	ZMTHS1	ZMTHS0	ZMHYS1	ZMHYS0
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
7	RW	0	RMSZS2	Select channel for reading the zero-mute RMS level on registers rmsZMH (0x7A) & rmsZML (0x7B).
6	RW	0	RMSZS1	
5	RW	0	RMSZS0	
4	RW	0	ZMTHS2	Select the zero-mute threshold level. If signal is below this level, output will be in switch off mode.
3	RW	0	ZMTHS1	
2	RW	0	ZMTHS1	
1	RW	0	ZMHYS1	Select the hysteresis window width.
0	RW	0	ZMHYS0	

The STA311B implements an RMS-based zero-detect function (on serial input interface data) able to detect in a very reliable way the presence of an input signal, so that the power bridge outputs can be automatically connected to ground. When active, the function will mute the output PWM when the input level become less than threshold - hysteresis.

Once muted, the PWM will be unmuted when the input level is detected greater than threshold + hysteresis.

The measured level is then reported (each input channel is selected by RMSZS[2:0] value) on registers 0x7A, 0x7B.

Table 22. RMS channel select

RMSZS[2:0]	Channel
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

Table 23. Zero-detect threshold

ZMTHS[2:0]	Equivalent input level (dB)
000	-78
001	-84
010	-90
011	-96
100	-102
101	-108
110	-114
111	-114

Table 24. Zero-detect hysteresis

ZMHYS[1:0]	Equivalent input level hysteresis(dB)
00	3
01	4
10	5
11	6

9.5.8 RMS post-processing selectors and Fs autodetection (0x70)

D7	D6	D5	D4	D3	D2	D1	D0
RMSOS2	RMSOS1	RMSOS0					FXLRC0
0	0	0	0	0	0	0	0

RMS out selector

Bit	RW	RST	Name	Description
7	RW	0	RMSOS2	RMS post-processing selectors. For each channel the current RMS value after the processing step is available on registers rmsPOH (0x7C) and rmsPOL (0x7D).
6	RW	0	RMSOS1	
5	RW	0	RMSOS0	

Table 25. RMS post-processing channel select

RMSOS[2:0]	Channel
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

Fs autodetection

Bit	RW	RST	Name	Description
0	RW	0	FXLRC0	If set to 1, the IR and BST32K parameters are auto-selected by the Fs autodetection internal block; otherwise, the I²C register values are used.

9.5.9 Clock manager configuration

PLL configuration registers (0x71, 0x72, 0x73, 0x74)

PLL multiplication factor (fractional part, H) (0x71)

D7	D6	D5	D4	D3	D2	D1	D0
PLLFI[15:8]							
0	0	0	0	0	0	0	0

PLL multiplication factor (fractional part, L) (0x72)

D7	D6	D5	D4	D3	D2	D1	D0
PLLFI[7:0]							
0	0	0	0	0	0	0	0

PLL multiplication factor (integral part) named as N Division Factor (NDIV) and dithering (0x73)

D7	D6	D5	D4	D3	D2	D1	D0
PLLDD[1:0]		PLLND[5:0]					
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
7	RW	0	PLLDD1	PLL dithering: 00 : PLL clock dithering disabled 01 : PLL clock dithering enabled (triangular) 10 : PLLclock dithering enabled (rectangular) 11 : reserved
6	RW	0	PLLDD0	
5	RW	0	PLLND5	N (loop) Division Factor This factor should be: $5 \leq NDIV \leq 55$
4	RW	0	PLLND4	
3	RW	0	PLLND3	
2	RW	1	PLLND2	
1	RW	0	PLLND1	
0	RW	1	PLLND0	

PLL input division factor and others (0x74)

D7	D6	D5	D4	D3	D2	D1	D0
PDPDC	PLLFC	PLSTRB	PLSTBB	PLIDF3	PLIDF2	PLIDF1	PLIDF0
0	0	0	0	0	0	0	0

By default the STA311B is able to configure the embedded PLL automatically depending on the MCS bits (reg 0x00). For certain applications and to provide flexibility to the user, a manual PLL configuration can be used (setting PLLFC to 1). The output PLL frequency formula is:

$$Fout = \frac{Fin}{IDF} \times \left(ND + \frac{FI}{2^{16}}\right) \quad \text{when PLLFC = 1}$$

$$Fout = \frac{Fin}{IDF} \times (ND) \quad \text{when PLLFC = 0}$$

Clock manager configuration register (0x75)

D7	D6	D5	D4	D3	D2	D1	D0
				PLLBYP	PLLDPR	LOWEN	BST32K
				0	0	0	0

Bit	RW	RST	Name	Description
3	RW	0	PLLBYP	PLL bypass enable ‘0’: disabled ‘1’: bypassed
2	RW	0	PLLDPR	PLL direct programming ‘0’: PLL configuration depends on MCS ‘1’: PLL configuration depends on I²C regs (0x72, 0x73 and 0x74)
1	RW	0	LOWEN	Low clock enable ‘0’: if input clock is too slow, master clock will become the internal oscillator clock (20 MHz), PLL bypassed ‘1’: disabled
0	RW	0	BST32K	Boost oversampling for fs = 32 kHz ‘0’: disabled ‘1’: input oversampling is selected x 3

Clock manager status register (0x76)

D7	D6	D5	D4	D3	D2	D1	D0
				PLLBYS	PLLPDS	OSCOK	LOWCKS
				0	0	0	0

Bit	RW	RST	Name	Description
3	R	0	PLLBYS	PLL bypass status ‘0’: normal ‘1’: bypassed
2	R	0	PLLPDS	PLL power-down status ‘0’: normal ‘1’: standby
1	R	0	OSCOK	Oscillator clock OK ‘0’: not ready ‘1’: ready
0	R	0	LOWCKS	Low clock status ‘0’: normal ‘1’: input clock too slow

9.5.10 RMS level registers (0x7A, 0x7B, 0x7C, 0x7D)

Two set of registers are available to monitor the RMS level detected by the zero-mute block and after the signal processing.

The measured level for a selected channel is given in 0x7A & 0x7B (zero-mute level) and 0x7C & 0x7D (PWM out level) according to the following expression:

$$Value(dB) = 20Log(rms[15:0]/(2^{16} \times 0.635))$$

where rms[15:0] is an unsigned integer formed by:

rms[15:0] = rmsZMH[7:0], rmsZML[7:0] for zero-mute level

or

rms[15:0] = rmsPOH[7:0], rmsPOL[7:0] for PWM output level

rmsZMx

D7	D6	D5	D4	D3	D2	D1	D0
RZM15	RZM14	RZM13	RZM12	RZM11	RZM10	RZM9	RZM8
0	0	0	0	0	0	0	0
RZM7	RZM6	RZM5	RZM4	RZM3	RZM2	RZM1	RZM0
0	0	0	0	0	0	0	0

rmsZMH

Bit	RW	RST	Name	Description
7	R		RZM15	RMS zero-detect level register, H
6	R		RZM14	
5	R		RZM13	
4	R		RZM12	
3	R		RZM11	
2	R		RZM10	
1	R		RZM9	
0	R		RZM8	

rmsZML

Bit	RW	RST	Name	Description
7	R		RZM7	RMS zero detect level register, L
6	R		RZM6	
5	R		RZM5	
4	R		RZM4	
3	R		RZM3	
2	R		RZM2	
1	R		RZM1	
0	R		RZM0	

rmsPOx

D7	D6	D5	D4	D3	D2	D1	D0
RPO15	RPO14	RPO13	RPO12	RPO11	RPO10	RPO9	RPO8
0	0	0	0	0	0	0	0
RPO7	RPO6	RPO5	RPO4	RPO3	RPO2	RPO1	RPO0
0	0	0	0	0	0	0	0

rmsPOH

Bit	RW	RST	Name	Description
7	R		RPO15	RMS PWM out (post-processing) register, H
6	R		RPO14	
5	R		RPO13	
4	R		RPO12	
3	R		RPO11	
2	R		RPO10	
1	R		RPO9	
0	R		RPO8	

rmsPOL

Bit	RW	RST	Name	Description
7	R		RPO7	RMS PWM out (post-processing) register, L
6	R		RPO6	
5	R		RPO5	
4	R		RPO4	
3	R		RPO3	
2	R		RPO2	
1	R		RPO1	
0	R		RPO0	

10 Startup/shutdown pop noise removal

10.1 DPT: PWM and tristate delay (0x80)

D7	D6	D5	D4	D3	D2	D1	D0
			DPT4	DPT3	DPT2	DPT1	DPT0
			1	1	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	DPT0	Set a delay between the PWM and the tristate signal to compensate the external amplifier delay.
1	RW	0	DPT1	
2	RW	0	DPT2	
3	RW	1	DPT3	
4	RW	1	DPT4	

10.2 Configuration register (0x81)

D7	D6	D5	D4	D3	D2	D1	D0
RL3	RL2	RL1	RL0	RD	SID1	FBYP	RTP
0	0	0	0	0	1	0	1

Bit	RW	RST	Name	Description
0	RW	1	RTP	Remove tristate initial pulses 1: remove the tristate initial pulses with frequency less than 16 kHz 0: the tristate initial pulses are not removed

Bit	RW	RST	Name	Description
1	RW	0	FBYP	Fault user-defined bypass mode 1: the fault internal management is disabled 0: the fault internal management is enabled

Bit	RW	RST	Name	Description
2	RW	1	SID1	Serial interface (I²S out) 1: SDO_56 is connected to the fault signal and SDO_78 outputs the tristate signal 0: I²S out normal

Bit	RW	RST	Name	Description
3	RW	0	RD	Startup/shutdown pop noise disable 1: the startup/shutdown tristate sequence used to remove the pop noise is disabled 0: the startup/shutdown tristate signal sequence used to remove the pop noise is enabled. This feature is not activated by default, and can be activated only if at least one channel is in binary mode and the PWMs out speed is equal to 384KHz.

Bit	RW	RST	Name	Description
4	RW	0	RL0	Set a tristate duration (same value for startup/shutdown pop noise removal)
5	RW	0	RL1	
6	RW	0	RL2	
7	RW	0	RL3	

RL[3:0]	Tristate duration
0000	default duration equal to 116 ms
0001	default value x2
0010	default value x3
0011	default value x4
0100	default value x5
0101	default value x6
0110	default value x7

10.3 User-defined delay time (0x82) and (0x83)

D7	D6	D5	D4	D3	D2	D1	D0
UDDT15	UDDT14	UDDT13	UDDT12	UDDT11	UDDT10	UDDT9	UDDT8
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
UDDT7	UDDT6	UDDT5	UDDT4	UDDT3	UDDT2	UDDT1	UDDT0
1	1	1	1	1	1	1	1

11 Package information

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Table 26. VFQFPN-56 (8 x 8 mm) package dimensions

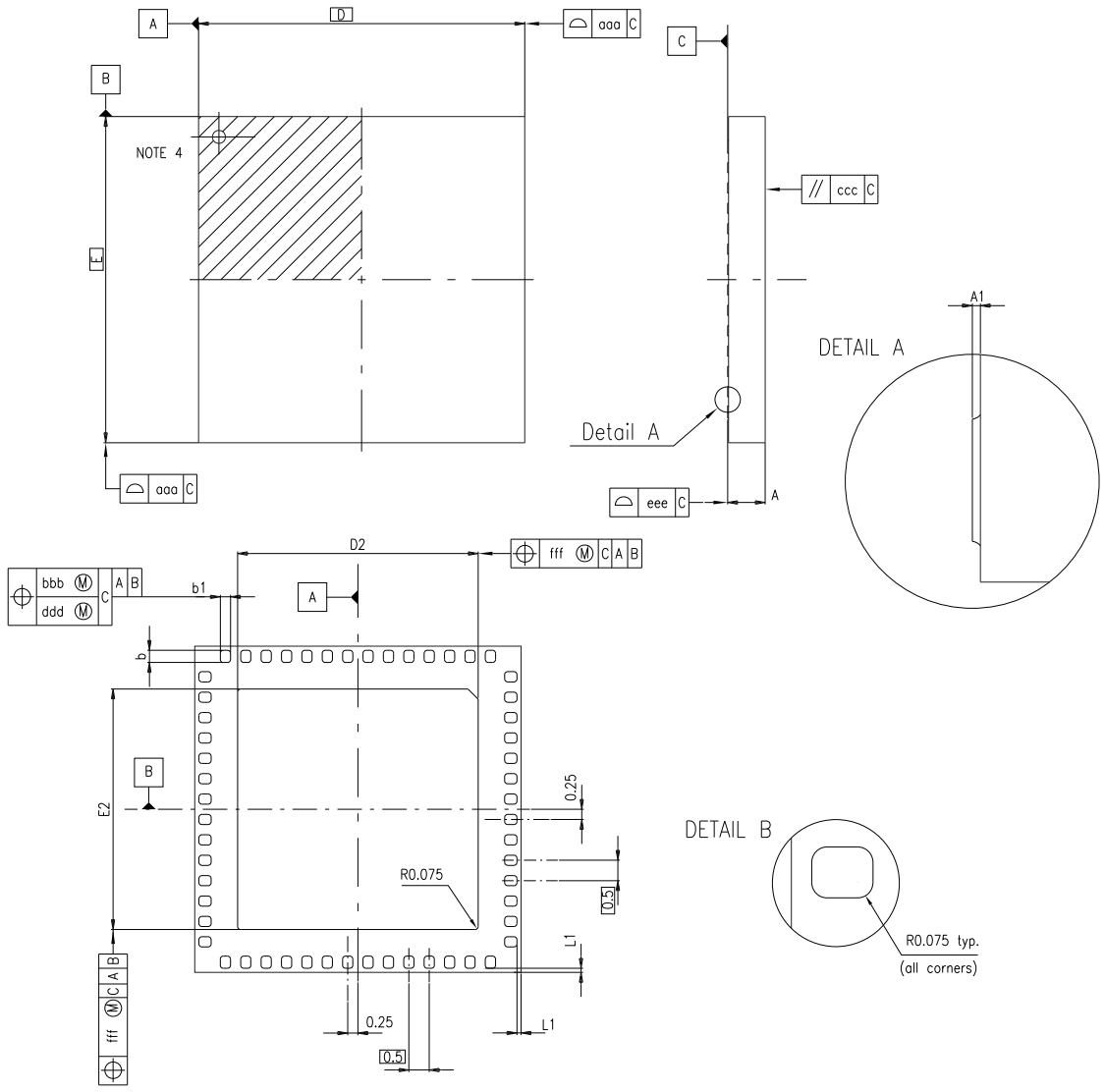
Reference	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0		0.05
D		8.00	
D2	See exposed pad variations		
E		8.00	
E2	See exposed pad variations		
b	0.25	0.30	0.35
b1	0.20	0.25	0.30
e (pad pitch)(1)			
L1	0.05		0.15
aaa		0.15	
bbb		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
ccc		0.10	

1. Refer to *Figure 12*.

Table 27. Exposed pad variations

Variation	D2			E2		
	Min.	Typ.	Max	Min.	Typ.	Max.
A	5.85	5.90	5.95	5.85	5.90	5.95
B	4.25	4.30	4.35	4.25	4.30	4.35

Figure 12. VFQFPN-56 (8 x 8 mm) package outline



NOTES
1 – All dimensions are in mm.
2 – Conform to JEDEC MO-220
3 – Au finishing
4 – Pin one indicator to be fully inside the hatched area

The axis of each pad must lie simultaneously in both tolerance zones.

(4) - The terminal A1 corner must be identified on the top surface through inked or lasered mark dot.
A distinguishing feature is allowable on the bottom surface of the package, chamfer at die paddle corner to identify the terminal A1. Exact shape of each corner is optional.

(5) – All dimensions are in mm.

826820

12 Revision history

Table 28. Document revision history

Date	Revision	Changes
21-Oct-2013	1	Initial release.

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