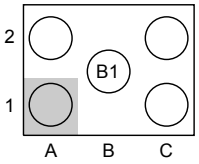
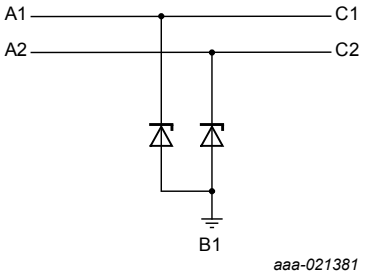
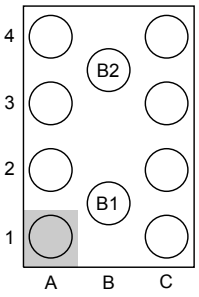
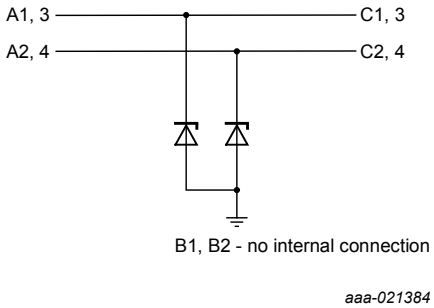
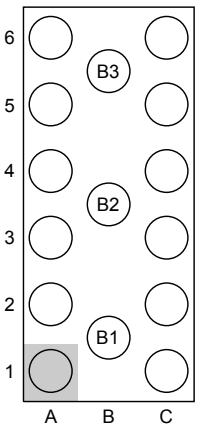
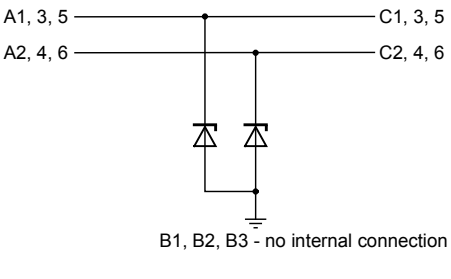
## 2. Pinning information

**Table 2. Pinning**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| **PESD1USB3S (WLCSP5_2-1-2)** | | | | |
| A1 | CH1_IN+ | channel 1+, external |  Transparent top view **WLCSP5_2-1-2** |  |
| A2 | CH1_IN- | channel 1-, external | | |
| B1 | GND_CH1 | ground channel 1 | | |
| C1 | CH1_OUT+ | channel 1+, internal | | |
| C2 | CH1_OUT- | channel 1-, internal | | |
| **PESD2USB3S (WLCSP10_4-2-4)** | | | | |
| A1 | CH1_IN+ | channel 1+, external |  Transparent top view **WLCSP10_4-2-4** |  |
| A2 | CH1_IN- | channel 1-, external | | |
| A3 | CH2_IN+ | channel 2+, external | | |
| A4 | CH2_IN- | channel 2-, external | | |
| B1 | GND_CH1 | ground channel 1 | | |
| B2 | GND_CH2 | ground channel 2 | | |
| C1 | CH1_OUT+ | channel 1+, internal | | |
| C2 | CH1_OUT- | channel 1-, internal | | |
| C3 | CH2_OUT+ | channel 2+, internal | | |
| C4 | CH2_OUT- | channel 2-, internal | | |
| **PESD3USB3S (WLCSP15_6-3-6)** | | | | |
| A1 | CH1_IN+ | channel 1+, external |  Transparent top view **WLCSP15_6-3-6** |  |
| A2 | CH1_IN- | channel 1-, external | | |
| A3 | CH2_IN+ | channel 2+, external | | |
| A4 | CH2_IN- | channel 2-, external | | |
| A5 | CH3_IN+ | channel 3+, external | | |
| A6 | CH3_IN- | channel 3-, external | | |
| B1 | GND_CH1 | ground channel 1 | | |
| B2 | GND_CH2 | ground channel 2 | | |
| B3 | GND_CH3 | ground channel 3 | | |
| C1 | CH1_OUT+ | channel 1+, internal | | |
| C2 | CH1_OUT- | channel 1-, internal | | |
| C3 | CH2_OUT+ | channel 2+, internal | | |
| C4 | CH2_OUT- | channel 2-, internal | | |
| C5 | CH3_OUT+ | channel 3+, internal | | |
| C6 | CH3_OUT- | channel 3-, internal | | |

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | |
|---|---|---|
| | Name | Description |
| PESD1USB3S | WLCSP5 | wafer level chip-size package; 5 bumps (2-1-2) |
| PESD2USB3S | WLCSP10 | wafer level chip-size package; 10 bumps (4-2-4) |
| PESD3USB3S | WLCSP15 | wafer level chip-size package; 15 bumps (6-3-6) |

## 4. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PESD1USB3S | PD1S |
| PESD2USB3S | PD2S |
| PESD3USB3S | PD3S |

## 5. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_I$ | input voltage | | -0.5 | 5 | V |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2, level 4; all input pins to ground | | | |
| | | • contact discharge | -15 | 15 | kV |
| | | • air discharge | -15 | 15 | kV |
| | | IEC 61000-4-2, level 4; all output pins to ground | | | |
| | | • contact discharge | -2 | 2 | kV |
| | | • air discharge | -2 | 2 | kV |
| $I_{PPM}$ | rated peak-pulse current | $t_p$ = 8/20 µs | -8 | 8 | A |
| $T_{stg}$ | storage temperature | | -40 | +125 | °C |
| $T_{amb}$ | ambient temperature | | -40 | +125 | °C |

# 6. Characteristics

## 6.1. Channel characteristics

**Table 6. Channel characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $C_d$ | diode capacitance | f = 1 MHz; $V_I$ = 2.5 V | [1] | - | 0.45 | - | pF |
| $I_{RM}$ | reverse leakage current | per line; $V_I$ = 5 V | | - | 1 | 100 | nA |
| $V_{BR}$ | breakdown voltage | $I_R$ = 1 mA | | 6 | 9 | - | V |
| $V_F$ | forward voltage | $I_F$ = 10 mA | | - | 0.8 | - | V |
| $R_{dyn}$ | dynamic resistance | TLP | [2] | | | | |
| | | • positive transient | | - | 0.16 | - | Ω |
| | | • negative transient | | - | 0.16 | - | Ω |
| | | surge | [3] | | | | |
| | | • positive transient | | - | 0.25 | - | Ω |
| | | • negative transient | | - | 0.25 | - | Ω |

[1] This parameter is guaranteed by design.
[2] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 70 to 90 ns.
[3] According to IEC 61000-4-5 (8/20 µs).

## 6.2. Frequency characteristics

**Table 7. Frequency characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Differential mode: $S_{dd21}$** | | | | | | | |
| $f_{-3dB}$ | cut-off frequency | | [1] | - | 17 | - | GHz |

[1] Normalized to attenuation at 1 MHz.

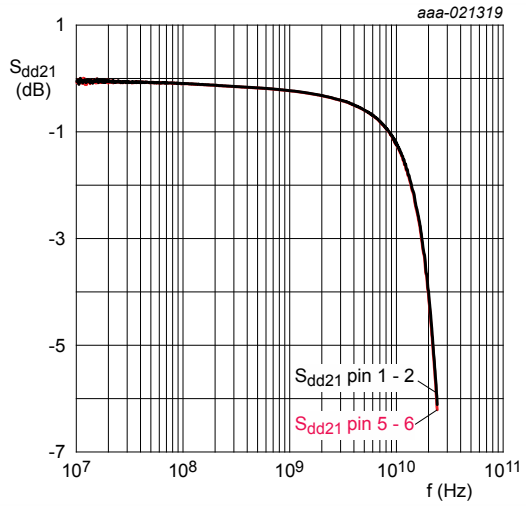



**Fig. 1. Differential mode insertion loss; typical values**

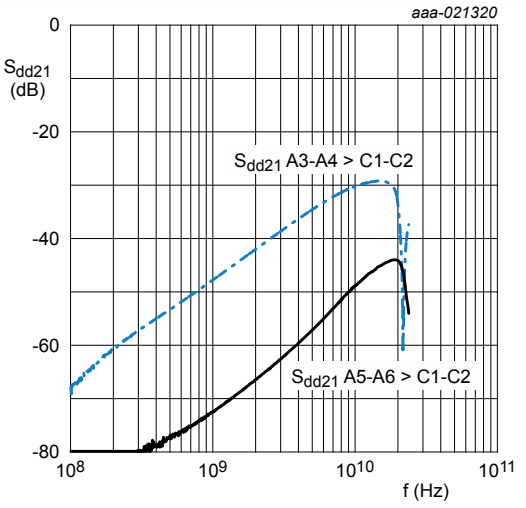
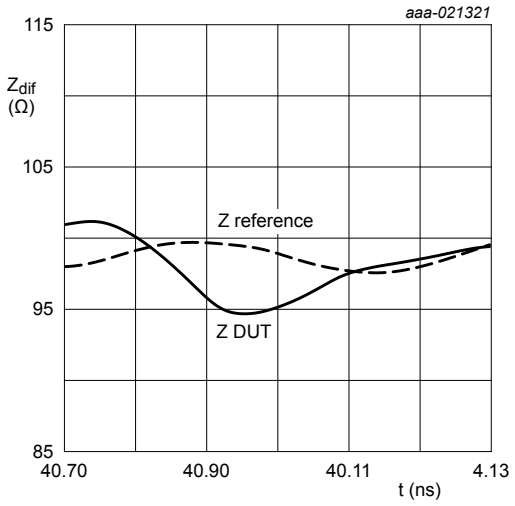
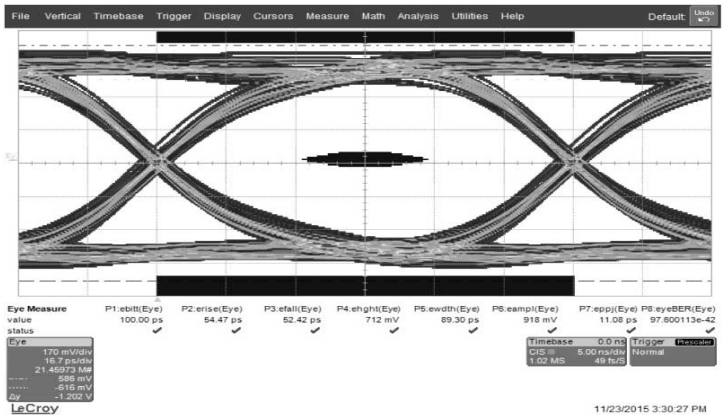



**Fig. 2. Differential cross-talk; typical values**



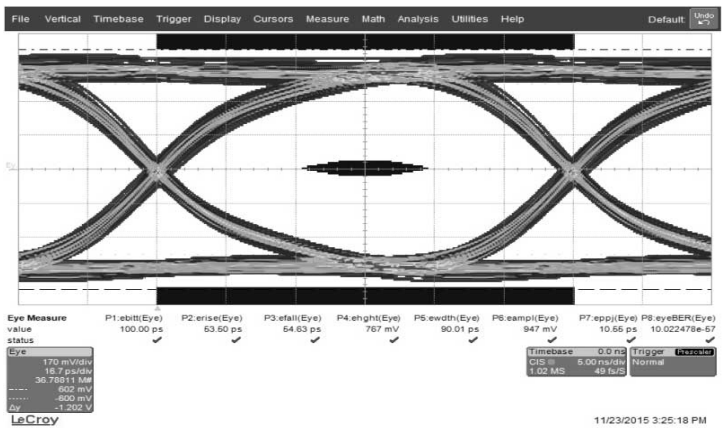

$t_r$ = 200 ps

**Fig. 3. Differential Time Domain Reflectometer (TDR) plot; typical values**




aaa-021322

**Fig. 4. USB3.1 eye diagram 10 Gbps, test board with PESD3USB3S; typical values**




aaa-021323

**Fig. 5. USB3.1 eye diagram 10 Gbps, test board without device; typical values**

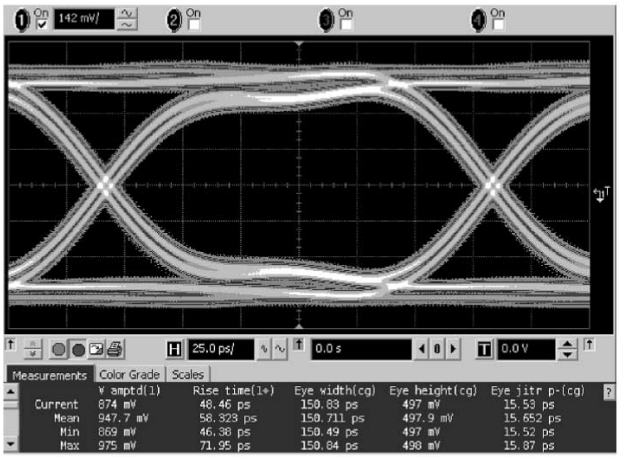



**Fig. 6. HDMI 2.0 eye diagram TP1, test board with PESD3USB3S; typical values**

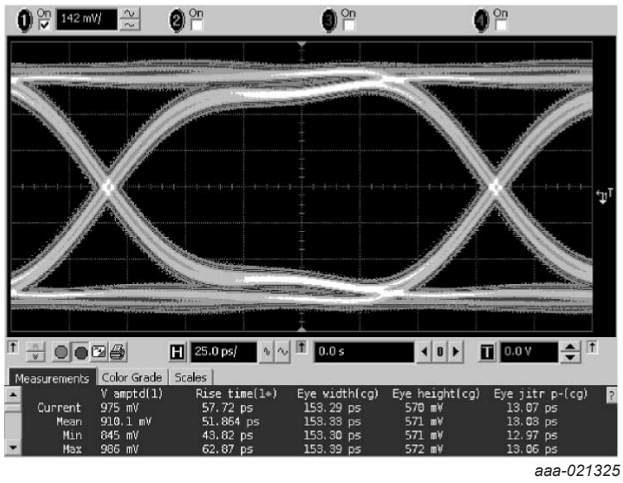
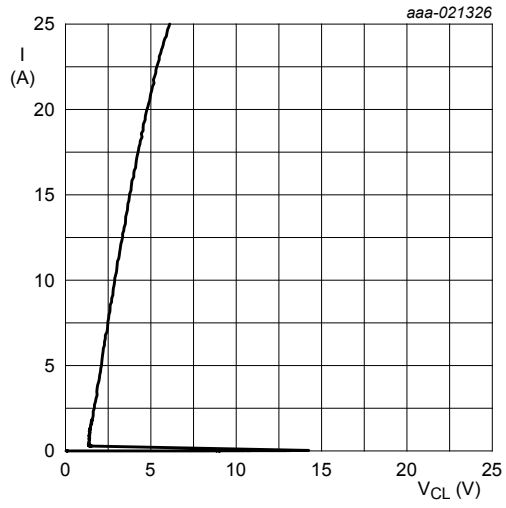
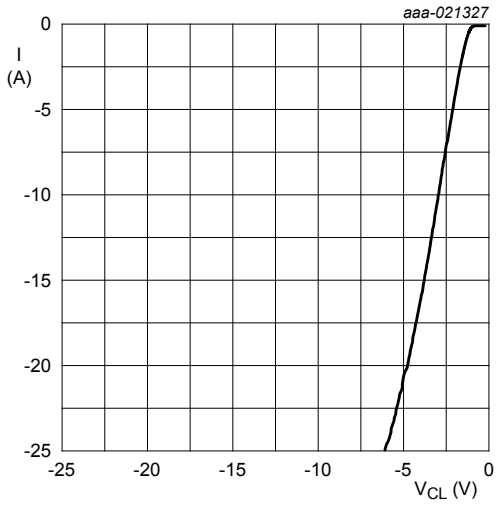



**Fig. 7. HDMI 2.0 eye diagram TP1, test board without device; typical values**



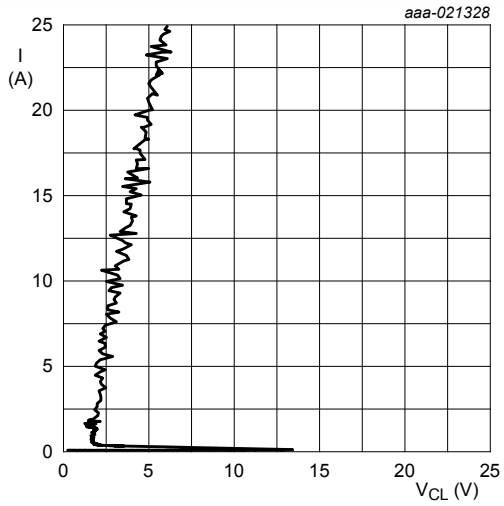

Transmission Line Pulse (TLP) = 100 ns

**Fig. 8. Dynamic resistance with positive clamping; typical values**



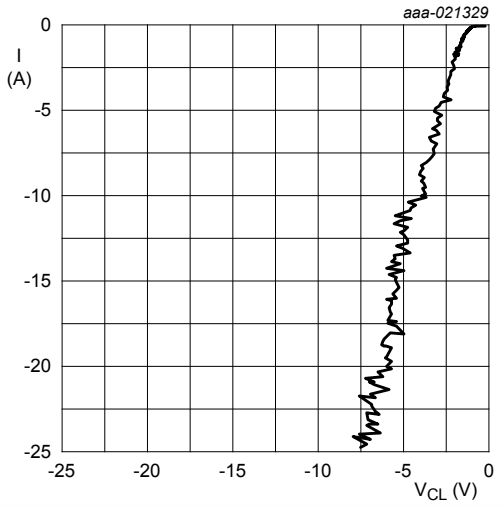

Transmission Line Pulse (TLP) = 100 ns

**Fig. 9. Dynamic resistance with negative; typical values**




Transmission Line Pulse (TLP) = 5 ns

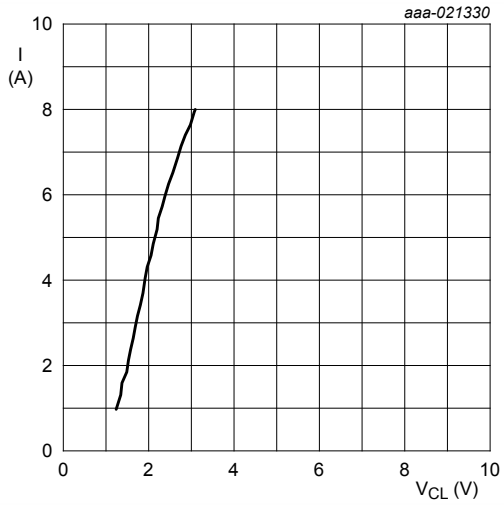
**Fig. 10. Dynamic resistance with positive clamping; typical values**




Transmission Line Pulse (TLP) = 5 ns

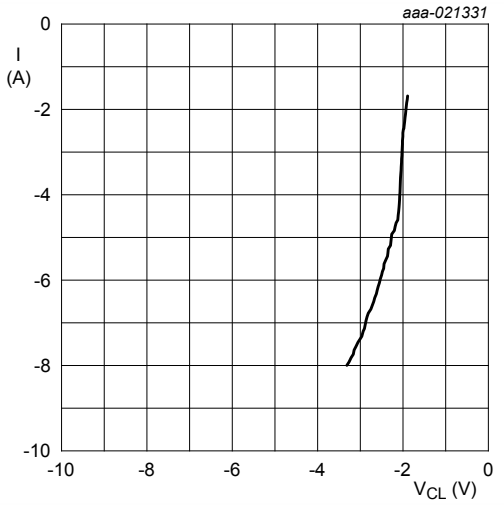
**Fig. 11. Dynamic resistance with negative clamping; typical values**

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).




IEC61000-4-5; $t_p$ = 8/20 µs; positive pulse

**Fig. 12. Dynamic resistance with positive clamping; typical values**




IEC61000-4-5; $t_p$ = 8/20 µs; negative pulse

**Fig. 13. Dynamic resistance with negative clamping; typical values**

# 7. Application information

The device is designed to provide high-level ESD protection for differential high-speed data line pairs such as:

- USB 3.2
- HDMI 2.0
- Transition-Minimized Differential Signaling (TMDS)
- DisplayPort
- external Serial Advanced Technology Attachment (eSATA)
- Low Voltage Differential Signaling (LVDS)

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the protected signal lines to unlimited current sources like, for example, a battery.

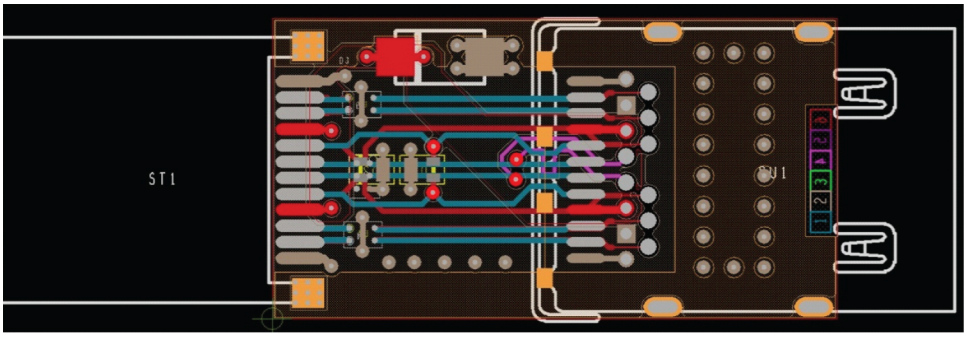
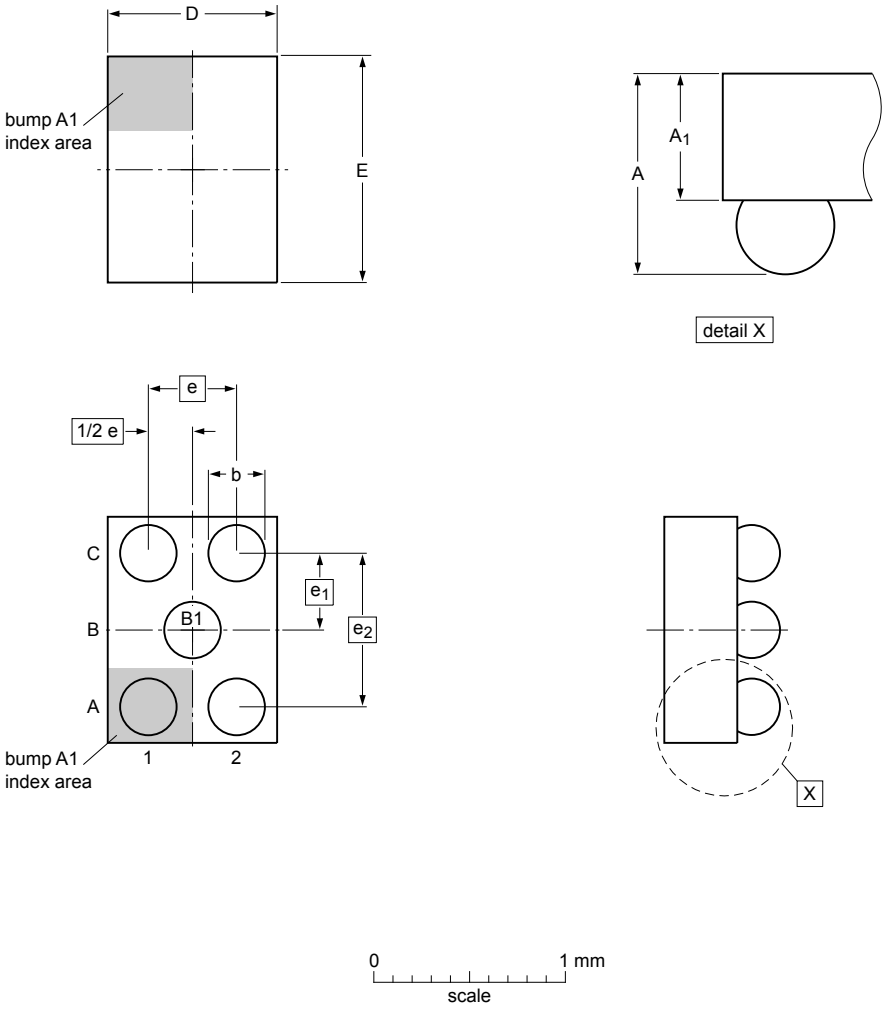



**Fig. 14. Application diagram: protecting the differential data lines of a USB Type-C connector evaluation dongle with PESD1USB3S**

Since the SuperSpeed TX/RX lines are separated by GND or VBUS from the Hi-Speed lines, PESD1USB3S makes it easy to achieve same signal lengths, straight routing, and optimal positioning for ESD protection directly at the connector.

# 8. Package outline

**WLCSP5: wafer level chip-size package; 5 bumps (2-1-2)** **PESD1USB3S**




Dimensions (mm are the original dimensions)

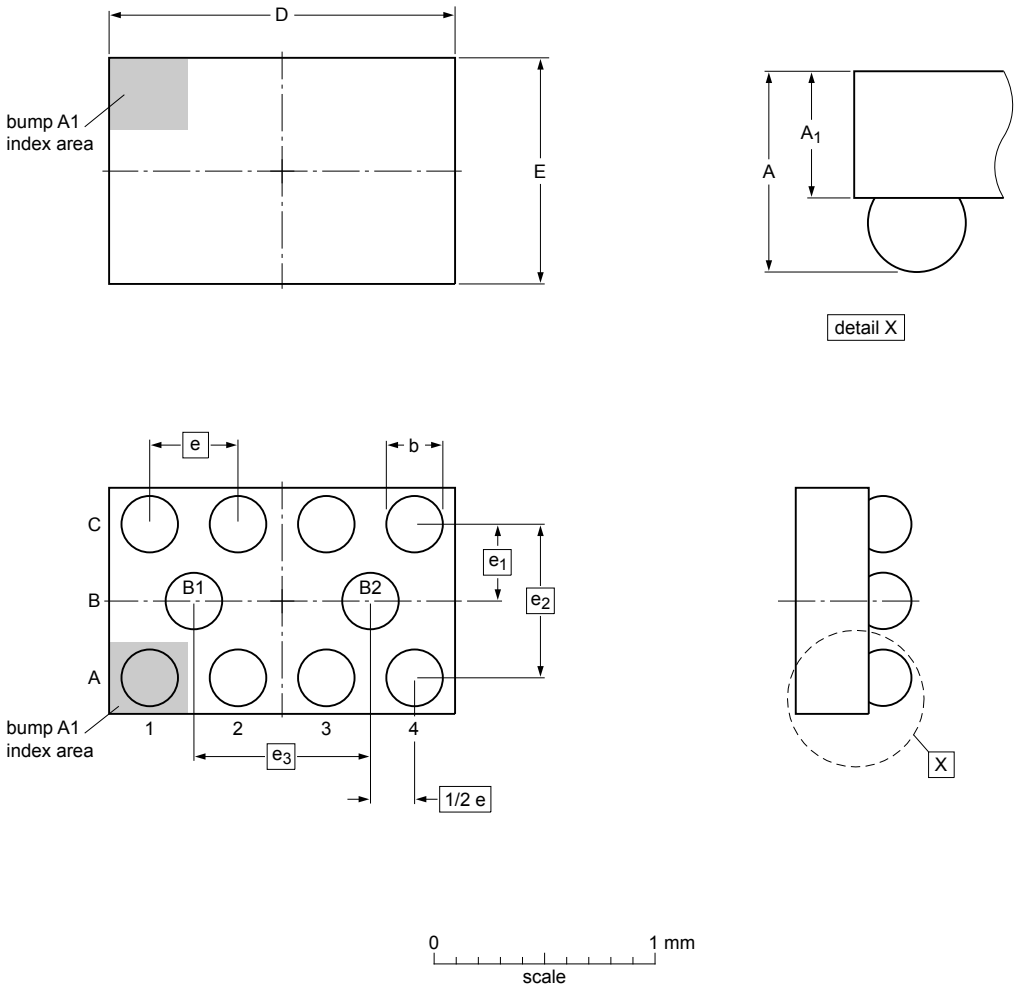
| Unit | | A | $A_1$ | b | D | E | e | $e_1$ | $e_2$ |
|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.60 | 0.38 | 0.31 | 0.82 | 1.22 | | | |
| | nom | 0.57 | 0.37 | 0.26 | 0.77 | 1.17 | 0.40 | 0.40 | 0.80 |
| | min | 0.54 | 0.36 | 0.21 | 0.72 | 1.12 | | | |

*pesd1usb3s_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| PESD1USB3S | | | | | | 15-12-11 |

**Fig. 15. Package outline WLCSP5**

**WLCSP10: wafer level chip-size package; 10 bumps (4-2-4)** **PESD2USB3S**




Dimensions (mm are the original dimensions)

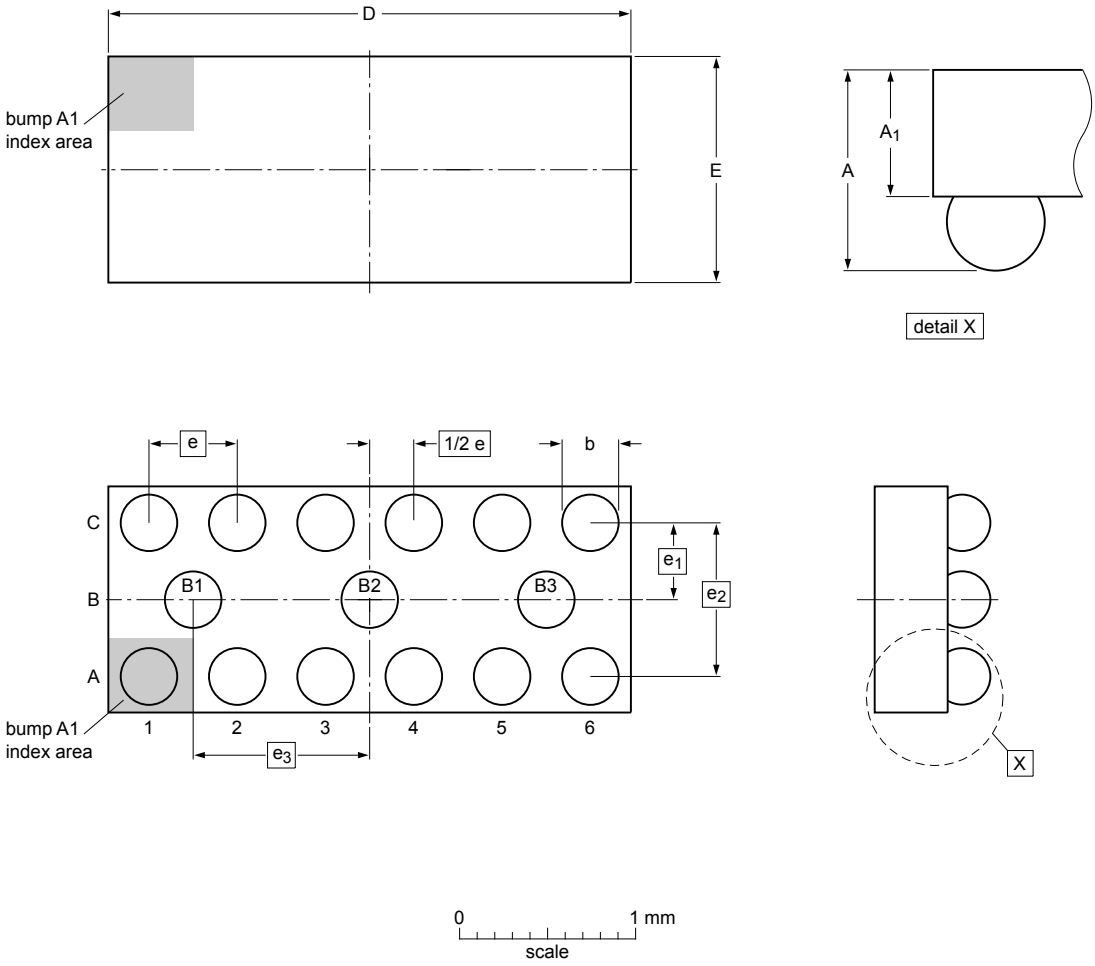
| Unit | | A | $A_1$ | b | D | E | e | $e_1$ | $e_2$ | $e_3$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.60 | 0.38 | 0.31 | 1.62 | 1.22 | | | | |
| | nom | 0.57 | 0.37 | 0.26 | 1.57 | 1.17 | 0.40 | 0.40 | 0.80 | 0.80 |
| | min | 0.54 | 0.36 | 0.21 | 1.52 | 1.12 | | | | |

*pesd2usb3s_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| PESD2USB3S | | | | | | 15-12-11 |

**Fig. 16. Package outline WLCSP10**

**WLCSP15: wafer level chip-size package; 15 bumps (6-3-6)** **PESD3USB3S**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | b | D | E | e | $e_1$ | $e_2$ | $e_3$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.60 | 0.38 | 0.31 | 2.42 | 1.22 | | | | |
| | nom | 0.57 | 0.37 | 0.26 | 2.37 | 1.17 | 0.40 | 0.40 | 0.80 | 0.80 |
| | min | 0.54 | 0.36 | 0.21 | 2.32 | 1.12 | | | | |

*pesd3usb3s_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| PESD3USB3S | | | | | | 15-12-11 |

**Fig. 17. Package outline WLCSP15**

# 9. Soldering

**WLCSP5: Solder footprint and stencil aperture** **PESD1USB3S**

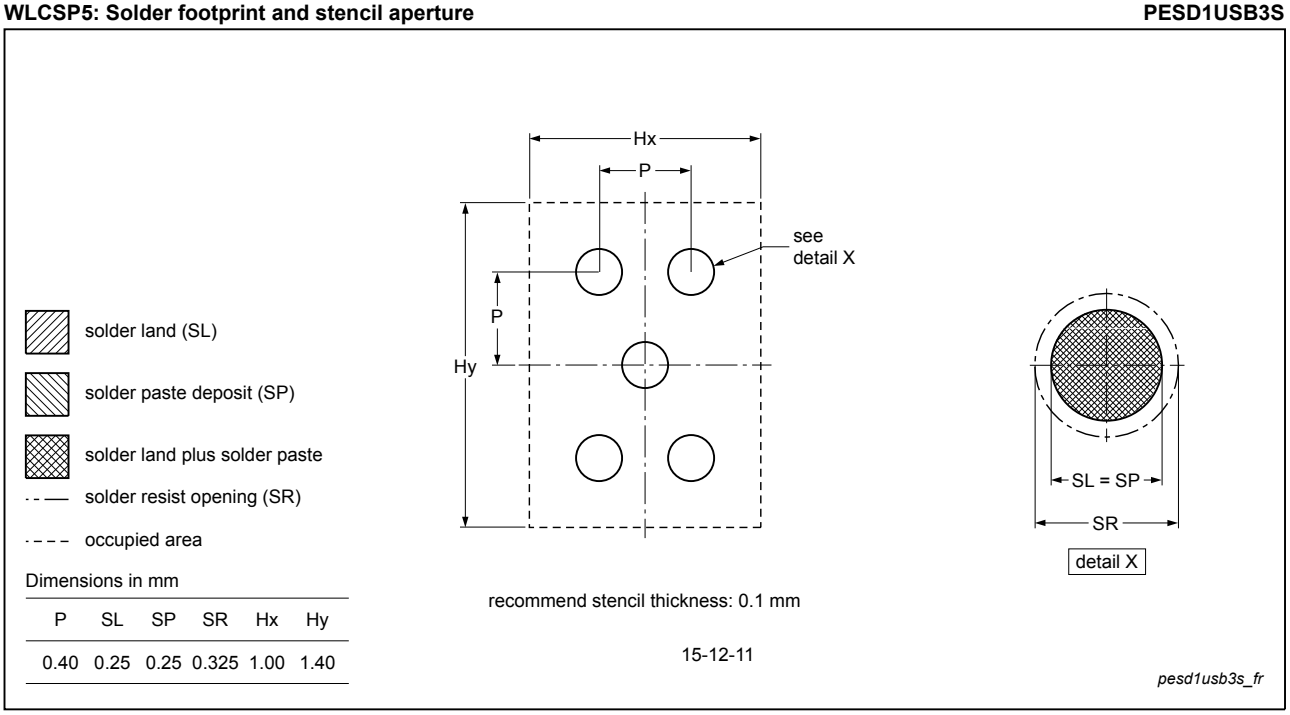



**Fig. 18. Soldering footprint WLCSP5 (PESD1USB3S)**

**WLCSP10: Solder footprint and stencil aperture** **PESD2USB3S**

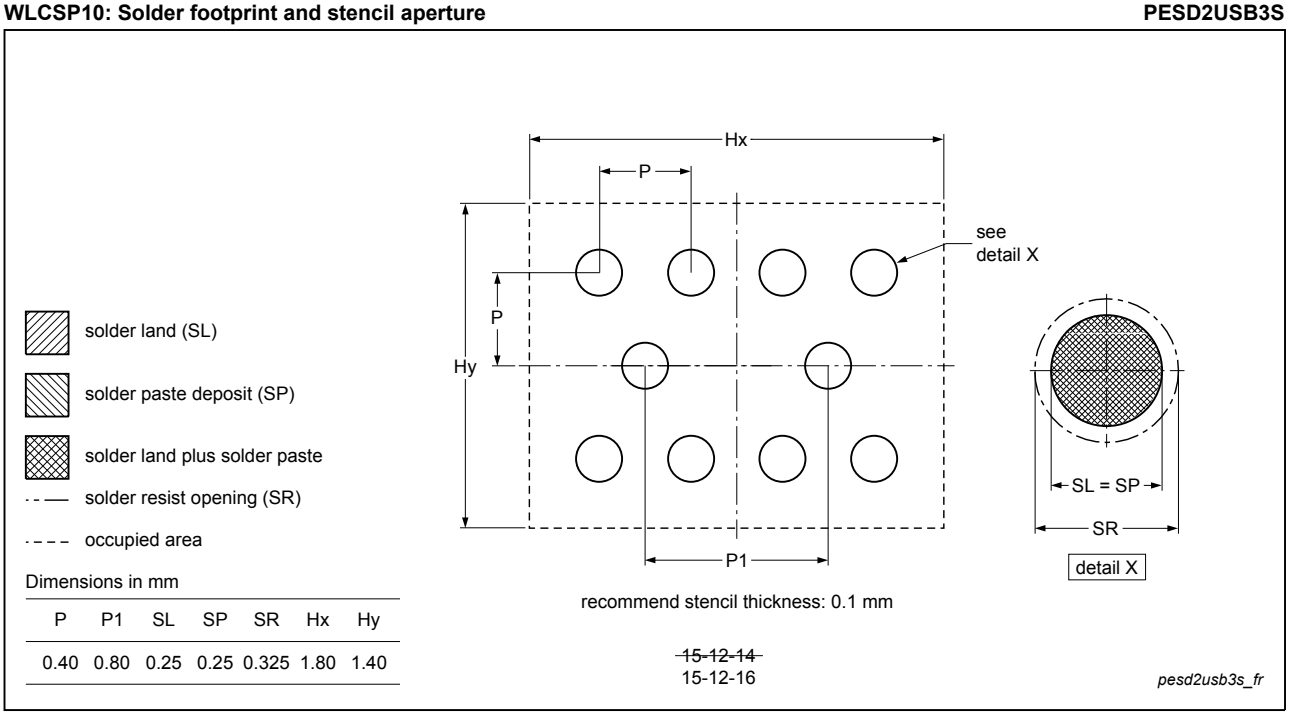



**Fig. 19. Soldering footprint WLCSP10 (PESD2USB3S)**

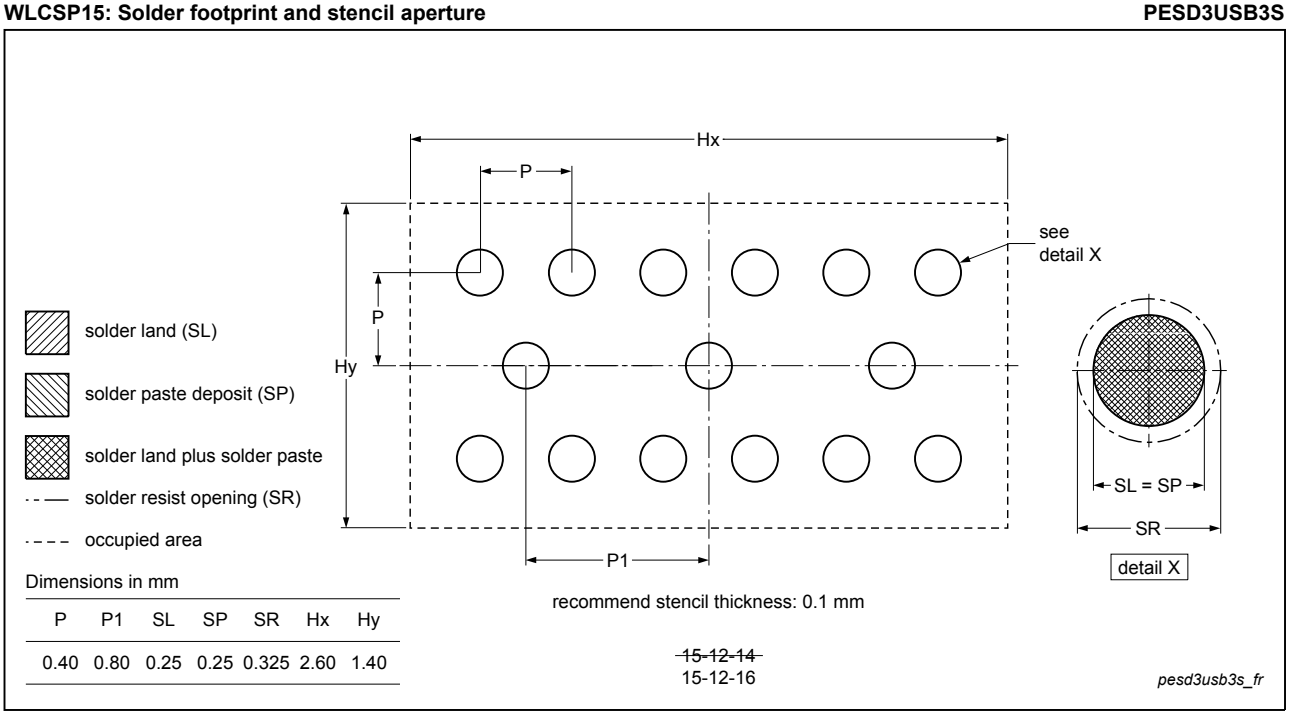



**Fig. 20. Soldering footprint WLCSP15 (PESD3USB3S)**

## 10. Revision history

**Table 8. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PESDXUSB3S_SER v.4 | 20190130 | Product data sheet | - | PESDXUSB3S_SER v.3 |
| Modifications: | • Limiting values: maximum value for $T_{amb}$ updated<br>• Frequency characteristics: table and Fig 2 + 3: $S_{21dd}$ changed to $S_{dd21}$ | | | |
| PESDXUSB3S_SER v.3 | 20160426 | Product data sheet | - | PESDXUSB3S_SER v.2 |
| PESDXUSB3S_SER v.2 | 20160127 | Product data sheet | - | PESDXUSB3S_SER v.1 |
| PESDXUSB3S_SER v.1 | 20151216 | | | |

# 11. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com
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