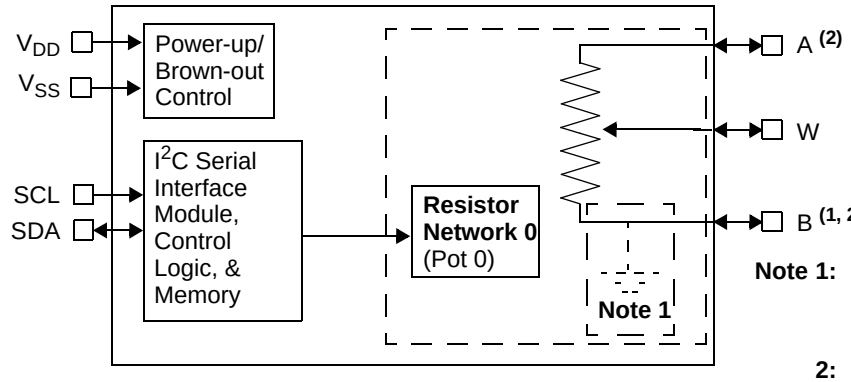
Device Block Diagram



Note 1: Some configurations will have this signal internally connected to ground.

2: In some configurations, this signal may not be connected externally (internally floating or grounded).

Comparison of Similar Microchip Devices (1)

Device	Control Interface	# of Steps	Wiper Configuration	Memory Type	Resistance (typical) Options (kΩ)	V_{DD} Operating Range	HV Interface	WiperLock Technology	Package
MCP40D17 (2)	I²C	128	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	No	No	SC70-6
MCP4017 (2, 4)	I²C	128	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	No	No	SC70-6
MCP4012 (2)	U/D	64	Rheostat	RAM	2.1, 5.0, 10.0, 50.0	1.8V to 5.5V	Yes	No	SOT-23-6
MCP4022 (2)	U/D	64	Rheostat	EE	2.1, 5.0, 10.0, 50.0	2.7V to 5.5V	Yes	Yes	SOT-23-6
MCP4132 (3)	SPI	129	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	Yes	No	PDIP-8, SOIC-8, MSOP-8, DFN-8
MCP4142 (3)	SPI	129	Rheostat	EE	5.0, 10.0, 50.0, 100.0	2.7V to 5.5V	Yes	Yes	
MCP4152 (3)	SPI	257	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	Yes	No	
MCP4162 (3)	SPI	257	Rheostat	EE	5.0, 10.0, 50.0, 100.0	2.7V to 5.5V	Yes	Yes	
MCP4532 (3)	I²C	129	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	Yes	No	MSOP-8, DFN-8
MCP4542 (3)	I²C	129	Rheostat	EE	5.0, 10.0, 50.0, 100.0	2.7V to 5.5V	Yes	Yes	
MCP4552 (3)	I²C	257	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	Yes	No	
MCP4562 (3)	I²C	257	Rheostat	EE	5.0, 10.0, 50.0, 100.0	2.7V to 5.5V	Yes	Yes	
MCP40D18 (2)	I²C	128	Potentiometer	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	No	No	SC70-6
MCP4018 (2, 4)	I²C	128	Potentiometer	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	No	No	SC70-6
MCP4013 (2)	U/D	64	Potentiometer	RAM	2.1, 5.0, 10.0, 50.0	1.8V to 5.5V	Yes	No	SOT-23-6
MCP4023 (2)	U/D	64	Potentiometer	EE	2.1, 5.0, 10.0, 50.0	2.7V to 5.5V	Yes	Yes	SOT-23-6
MCP40D19 (2)	I²C	128	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	No	No	SC70-5
MCP4019 (2, 4)	I²C	128	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	No	No	SC70-5
MCP4014 (2)	U/D	64	Rheostat	RAM	2.1, 5.0, 10.0, 50.0	1.8V to 5.5V	Yes	No	SOT-23-5
MCP4024 (2)	U/D	64	Rheostat	EE	2.1, 5.0, 10.0, 50.0	2.7V to 5.5V	Yes	Yes	SOT-23-5

Note 1: This table is broken into three groups by a thick line (and color coding). The unshaded devices in this table are the devices described in this data sheet, while the shaded devices offer a comparable resistor network configuration.

2: Analog characteristics only tested from 2.7V to 5.5V.

3: Analog characteristics only tested from 3.0V to 5.5V.

4: These devices have a simplified I²C command format, which allows higher data throughput.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS} ..... -0.6V to +7.0V
Voltage on SCL, and SDA with respect to V_{SS} ..... -0.6V to 12.5V
Voltage on all other pins (A, W, and B) with respect to V_{SS} ..... -0.3V to V_{DD} + 0.3V
Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ ON HV pins) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA
Maximum output current sunk by any Output pin ..... 25 mA
Maximum output current sourced by any Output pin ..... 25 mA
Maximum current out of V_{SS} pin ..... 100 mA
Maximum current into V_{DD} pin ..... 100 mA
Maximum current into A, W and B pins ..... ±2.5 mA
Package power dissipation (T_A = +50°C, T_J = +150°C)
SC70-5 ..... 302 mW
SC70-6 ..... 483 mW
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C
ESD protection on all pins ..... ≥ 4 kV (HBM)
..... ≥ 400V (MM)
Maximum Junction Temperature (T_J) ..... +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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AC/DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Supply Voltage	V_{DD}	2.7	—	5.5	V	Analog Characteristics specified
		1.8	—	5.5	V	Digital Characteristics specified
V_{DD} Start Voltage to ensure Wiper Reset	V_{BOR}	—	—	1.65	V	RAM retention voltage (V_{RAM}) < V_{BOR}
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	(**Note 7**)			V/ms	
Delay after device exits the reset state (V_{DD} > V_{BOR})	T_{BORD}	—	10	20	µS	
Supply Current **(Note 8)**	I_{DD}	—	45	80	µA	Serial Interface Active, Write all 0's to Volatile Wiper V_{DD} = 5.5V, F_{SCL} = 400 kHz
		—	2.5	5	µA	Serial Interface Inactive, (Stop condition, SCL = SDA = V_{IH}), Wiper = 0, V_{DD} = 5.5V

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP40D18** device only, includes V_{WZSE} and V_{WFSE}.

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This specification by design.

6: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

7: POR/BOR is not rate dependent.

8: Supply current is independent of current through the resistor network

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Resistance (± 20%)	R_{AB}	4.0	5	6.0	kΩ	-502 devices **(Note 1)**	
		8.0	10	12.0	kΩ	-103 devices **(Note 1)**	
		40.0	50	60.0	kΩ	-503 devices **(Note 1)**	
		80.0	100	120.0	kΩ	-104 devices **(Note 1)**	
Resolution	N		128		Taps	No Missing Codes	
Step Resistance	R_S	—	R_{AB} / (127)	—	Ω	**Note 5**	
Wiper Resistance	R_W	—	100	170	Ω	V_{DD} = 5.5 V, I_W = 2.0 mA, code = 00h	
		—	155	325	Ω	V_{DD} = 2.7 V, I_W = 2.0 mA, code = 00h	
Nominal Resistance Tempco	$\Delta R_{AB}/\Delta T$	—	50	—	ppm/°C	T_A = -20°C to +70°C	
		—	100	—	ppm/°C	T_A = -40°C to +85°C	
		—	150	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco	$\Delta V_{WB}/\Delta T$	—	15	—	ppm/°C	Code = Midscale (3Fh)	
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	Vss	—	V_{DD}	V	**Note 4, Note 5**	
Maximum current through Terminal (A, W or B) **Note 5**	I_T	—	—	2.5	mA	Terminal A	I_{AW}, W = Full Scale (FS)
		—	—	2.5	mA	Terminal B	I_{BW}, W = Zero Scale (ZS)
		—	—	2.5	mA	Terminal W	I_{AW} or I_{BW}, W = FS or ZS
		—	—	1.38	mA	Terminal A and Terminal B	I_{AB}, V_B = 0V, V_A = 5.5V, $R_{AB(MIN)}$ = 4000
		—	—	0.688	mA		I_{AB}, V_B = 0V, V_A = 5.5V, $R_{AB(MIN)}$ = 8000
		—	—	0.138	mA		I_{AB}, V_B = 0V, V_A = 5.5V, $R_{AB(MIN)}$ = 40000
		—	—	0.069	mA		I_{AB}, V_B = 0V, V_A = 5.5V, $R_{AB(MIN)}$ = 80000

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP40D18** device only, includes V_{WZSE} and V_{WFSE}.

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This specification by design.

6: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

7: POR/BOR is not rate dependent.

8: Supply current is independent of current through the resistor network

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Full Scale Error (**MCP40D18** only) (code = 7Fh)	V_{WFSE}	-3.0	-0.1	—	LSb	5 kΩ	2.7V ≤ V_{DD} ≤ 5.5V
		-2.0	-0.1	—	LSb	10 kΩ	2.7V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb	50 kΩ	2.7V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb	100 kΩ	2.7V ≤ V_{DD} ≤ 5.5V
Zero Scale Error (**MCP40D18** only) (code = 00h)	V_{WZSE}	—	+0.1	+3.0	LSb	5 kΩ	2.7V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+2.0	LSb	10 kΩ	2.7V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb	50 kΩ	2.7V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb	100 kΩ	2.7V ≤ V_{DD} ≤ 5.5V
Potentiometer Integral Non-linearity	INL	-0.5	±0.25	+0.5	LSb	2.7V ≤ V_{DD} ≤ 5.5V **MCP40D18** device only **(Note 2)**	
Potentiometer Differential Non-linearity	DNL	-0.25	±0.125	+0.25	LSb	2.7V ≤ V_{DD} ≤ 5.5V **MCP40D18** device only **(Note 2)**	
Bandwidth -3 dB (See Figure 2-83, load = 30 pF)	BW	—	2	—	MHz	5 kΩ	Code = 3Fh
		—	1	—	MHz	10 kΩ	Code = 3Fh
		—	260	—	kHz	50 kΩ	Code = 3Fh
		—	100	—	kHz	100 kΩ	Code = 3Fh

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP40D18** device only, includes V_{WZSE} and V_{WFSE}.

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This specification by design.

6: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

7: POR/BOR is not rate dependent.

8: Supply current is independent of current through the resistor network

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Rheostat Integral Non-linearity **MCP40D18** (**Note 3**) **MCP40D17** and **MCP40D19** devices only **(Note 3)**	R-INL	-2.0	±0.5	+2.0	LSb	5 kΩ	5.5V, I_W = 900 µA
		-5.0	+3.5	+5.0	LSb		2.7V, I_W = 430 µA (**Note 6**)
		See **Section 2.0**			LSb		1.8V (**Note 6**)
		-2.0	±0.5	+2.0	LSb	10 kΩ	5.5V, I_W = 450 µA
		-4.0	+2.5	+4.0	LSb		2.7V, I_W = 215 µA (**Note 6**)
		See **Section 2.0**			LSb		1.8V (**Note 6**)
		-1.125	±0.5	+1.125	LSb	50 kΩ	5.5V, I_W = 90 µA
		-1.5	+1	+1.5	LSb		2.7V, I_W = 43 µA (**Note 6**)
		See **Section 2.0**			LSb		1.8V (**Note 6**)
		-0.8	±0.5	+0.8	LSb	100 kΩ	5.5V, I_W = 45 µA
		-1.125	+0.25	+1.125	LSb		2.7V, I_W = 21.5 µA (**Note 6**)
		See **Section 2.0**			LSb		1.8V (**Note 6**)
Rheostat Differential Non-linearity **MCP40D18** (**Note 3**) **MCP40D17** and **MCP40D19** devices only **(Note 3)**	R-DNL	-0.5	±0.25	+0.5	LSb	5 kΩ	5.5V, I_W = 900 mA
		-0.75	+0.5	+0.75	LSb		2.7V, I_W = 430 µA (**Note 6**)
		See **Section 2.0**			LSb		1.8V (**Note 6**)
		-0.5	±0.25	+0.5	LSb	10 kΩ	5.5V, I_W = 450 µA
		-0.75	+0.5	+0.75	LSb		2.7V, I_W = 215 µA (**Note 6**)
		See **Section 2.0**			LSb		1.8V (**Note 6**)
		-0.375	±0.25	+0.375	LSb	50 kΩ	5.5V, I_W = 90 µA
		-0.375	±0.25	+0.375	LSb		2.7V, I_W = 43 µA (**Note 6**)
		See **Section 2.0**			LSb		1.8V (**Note 6**)
		-0.375	±0.25	+0.375	LSb	100 kΩ	5.5V, I_W = 45 µA
		-0.375	±0.25	+0.375	LSb		2.7V, I_W = 21.5 µA (**Note 6**)
		See **Section 2.0**			LSb		1.8V (**Note 6**)
Capacitance (P_A)	C_{AW}	—	75	—	pF	f =1 MHz, Code = Full Scale	
Capacitance (P_W)	C_W	—	120	—	pF	f =1 MHz, Code = Full Scale	
Capacitance (P_B)	C_{BW}	—	75	—	pF	f =1 MHz, Code = Full Scale	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP40D18** device only, includes V_{WZSE} and V_{WFSE}.

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This specification by design.

6: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

7: POR/BOR is not rate dependent.

8: Supply current is independent of current through the resistor network

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Digital Inputs/Outputs (SDA, SCK)							
Schmitt Trigger High Input Threshold	V_{IH}	0.7 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 5.5V	
Schmitt Trigger Low Input Threshold	V_{IL}	-0.5	—	0.3V_{DD}	V		
Hysteresis of Schmitt Trigger Inputs **(Note 5)**	V_{HYS}	—	0.1V_{DD}	—	V	All inputs except SDA and SCL	
		N.A.	—	—	V	SDA and SCL, 100 kHz	V_{DD} < 2.0V
		N.A.	—	—	V	SDA and SCL, 100 kHz	V_{DD} ≥ 2.0V
		0.1 V_{DD}	—	—	V	SDA and SCL, 400 kHz	V_{DD} < 2.0V
		0.05 V_{DD}	—	—	V	SDA and SCL, 400 kHz	V_{DD} ≥ 2.0V
Output Low Voltage (SDA)	V_{OL}	V_{SS}	—	0.2V_{DD}	V	V_{DD} < 2.0V, I_{OL} = 1 mA	
		V_{SS}	—	0.4	V	V_{DD} ≥ 2.0V, I_{OL} = 3 mA	
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}	
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 400 kHz	
RAM (Wiper) Value							
Value Range	N	0h	—	7Fh	hex		
Wiper POR/BOR Value	$N_{POR/BOR}$	3Fh			hex		
Power Requirements							
Power Supply Sensitivity (**MCP40D18** only)	PSS	—	0.0005	0.0035	%/%	V_{DD} = 2.7V to 5.5V, V_A = 2.7V, Code = 3Fh	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP40D18** device only, includes V_{WZSE} and V_{WFSE}.

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This specification by design.

6: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

7: POR/BOR is not rate dependent.

8: Supply current is independent of current through the resistor network

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1.1 I²C Mode Timing Waveforms and Requirements

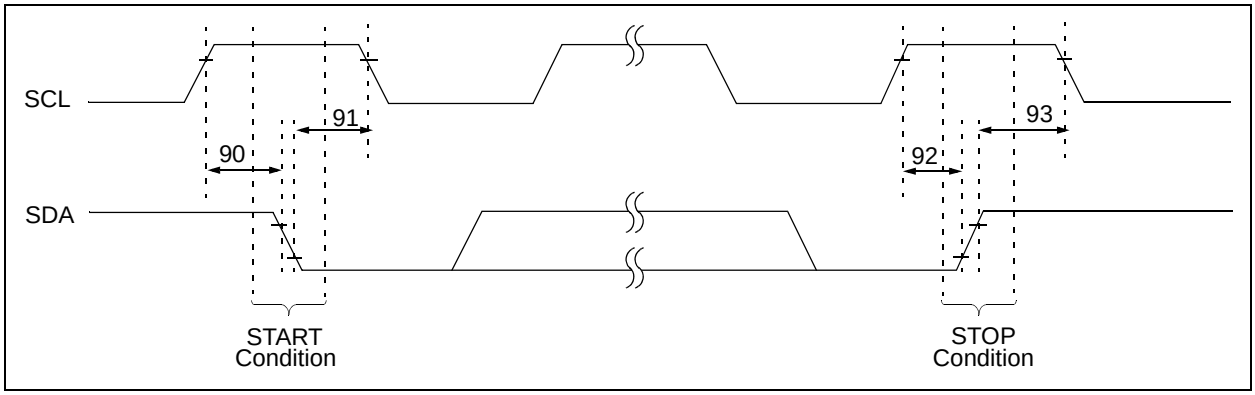
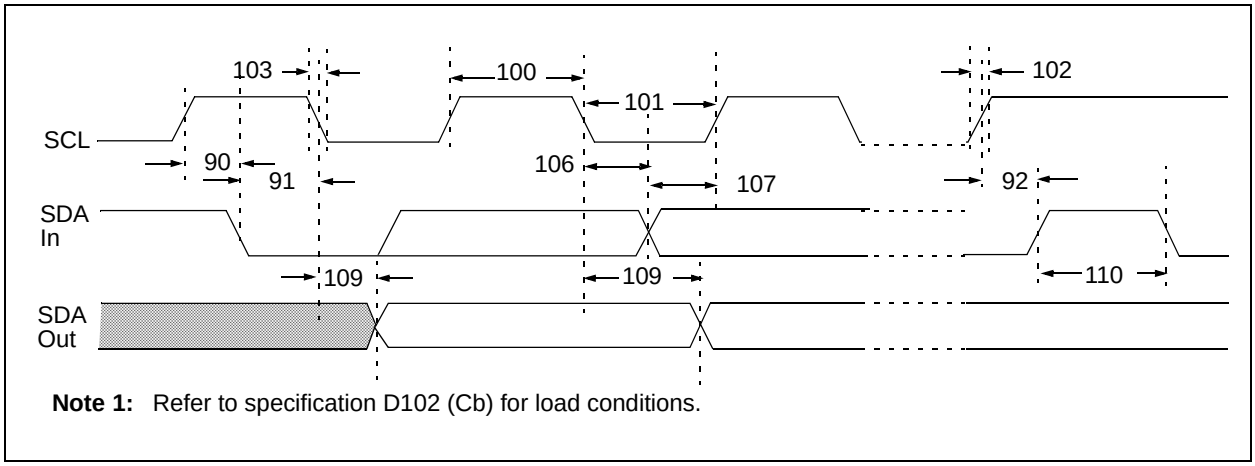


FIGURE 1-1: *I²C Bus Start/Stop Bits Timing Waveforms.*

TABLE 1-1: I²C BUS START/STOP BITS REQUIREMENTS

I²C AC Characteristics			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Section 2.0 "Typical Performance Curves"**				
Param. No.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
	F_{SCL}		Standard Mode	0	100	kHz	C_b = 400 pF, 1.8V - 5.5V
			Fast Mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
D102	Cb	Bus capacitive loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	ns	
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	ns	
92	TSU:STO	STOP condition Setup time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	



Note 1: Refer to specification D102 (Cb) for load conditions.

FIGURE 1-2: *I²C Bus Data Timing.*

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TABLE 1-2: I²C BUS DATA REQUIREMENTS (SLAVE MODE)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) Operating Voltage VDD range is described in **AC/DC characteristics**			
Parameter No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
100	T_{HIGH}	Clock high time	100 kHz mode	4000	—	ns	1.8V-5.5V
			400 kHz mode	600	—	ns	2.7V-5.5V
101	T_{LOW}	Clock low time	100 kHz mode	4700	—	ns	1.8V-5.5V
			400 kHz mode	1300	—	ns	2.7V-5.5V
102A (5)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
102B (5)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
103A (5)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	40	ns	
103B (5)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb (4)	300	ns	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	1.8V-5.5V, Note 6
			400 kHz mode	0	—	ns	2.7V-5.5V, Note 6
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	(2)
			400 kHz mode	100	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3450	ns	(1)
			400 kHz mode	—	900	ns	
110	T_{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start
			400 kHz mode	1300	—	ns	
	T_{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	Philips Spec states N.A.
			400 kHz mode	—	50	ns	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu; DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

3: The MCP40D18/MCP40D19 device must provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to guarantee that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not Tested.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

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TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	**Note 1**
Thermal Resistance, 6L-SC70	θ_{JA}	—	207	—	°C/W	

Note 1: Package Power Dissipation (P_{DIS}) is calculated as follows:
$P_{DIS} = (T_J - T_A) / \theta_{JA}$,
where: T_J = Junction Temperature, T_A = Ambient Temperature.

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NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

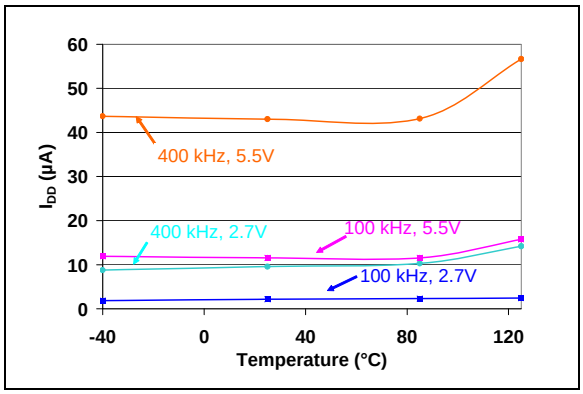

FIGURE 2-1: *Interface Active Current (I_{DD}) vs. SCL Frequency (f_{SCL}) and Temperature (V_{DD} = 1.8V, 2.7V and 5.5V).*

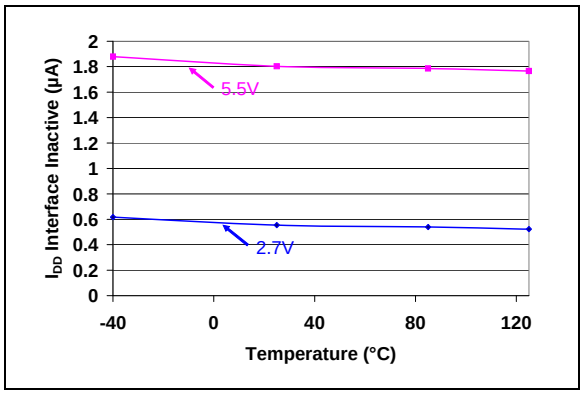

FIGURE 2-2: *Interface Inactive Current (I_{SHDN}) vs. Temperature and V_{DD}. (V_{DD} = 1.8V, 2.7V and 5.5V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

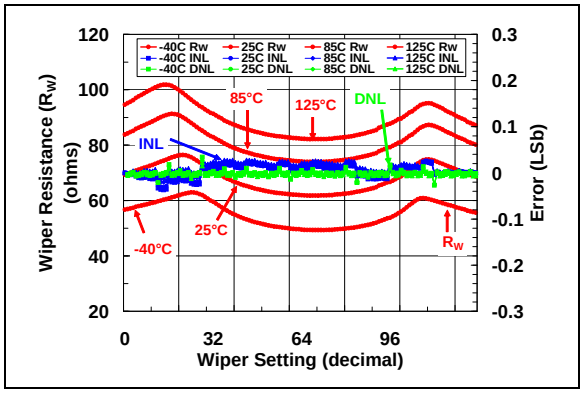


FIGURE 2-3: *5.0 kΩ: Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 5.5V). (A = V_{DD}, B = V_{SS}).*

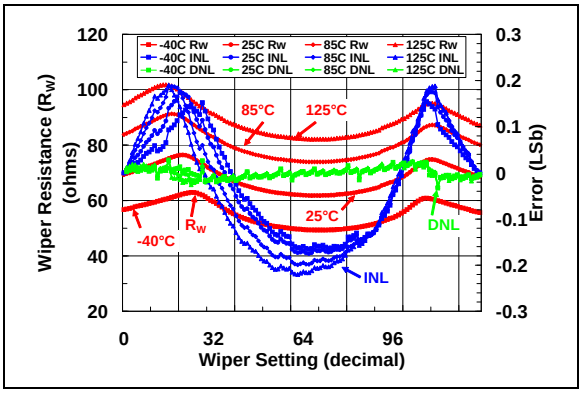


FIGURE 2-6: *5.0 kΩ: Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 5.5V).(I_W = 1.4 mA, B = V_{SS})*

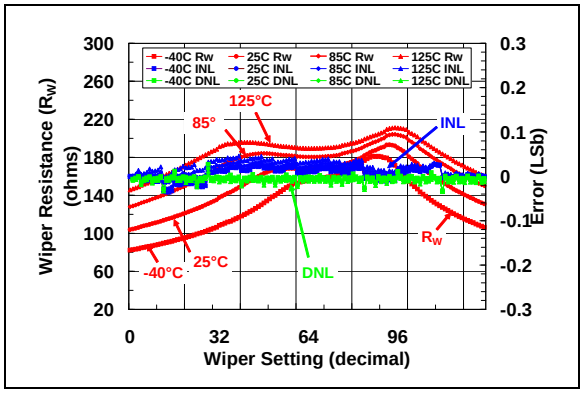


FIGURE 2-4: *5.0 kΩ: Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 2.7V). (A = V_{DD}, B = V_{SS})*

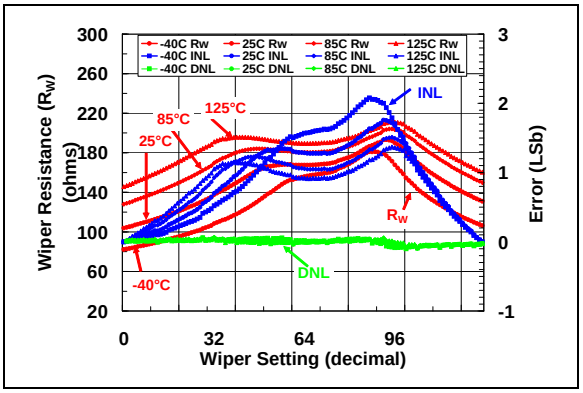
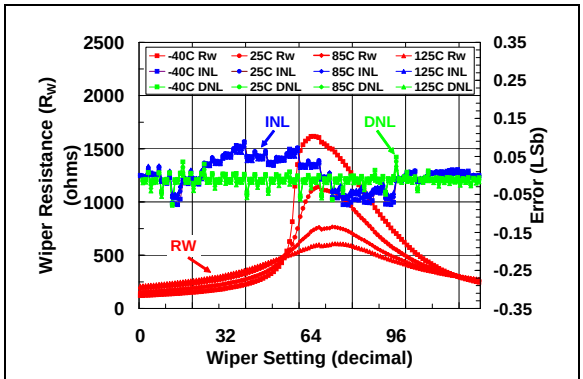
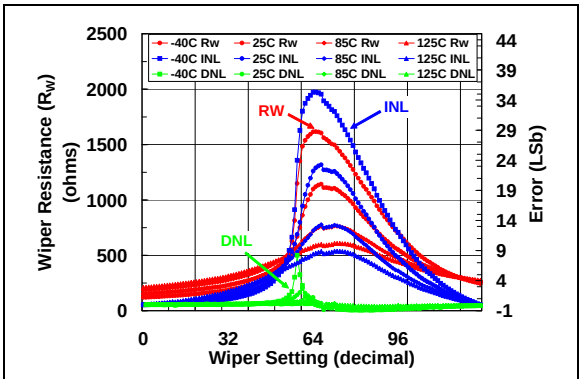


FIGURE 2-7: *5.0 kΩ: Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 2.7V).(I_W = 450 µA, B = V_{SS})*



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-5: *5.0 kΩ: Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 1.8V). (A = V_{DD}, B = V_{SS})*



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-8: *5.0 kΩ: Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 1.8V). (I_W =260 µA, B = V_{SS})*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

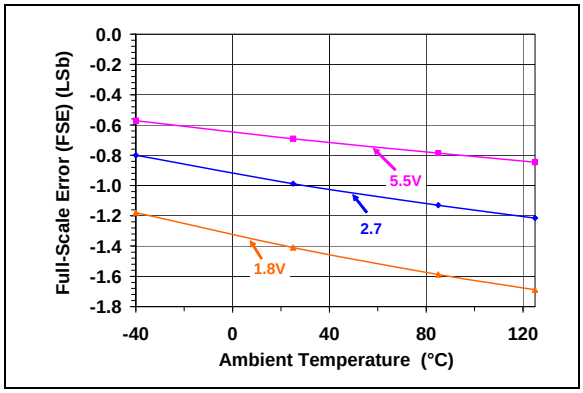

FIGURE 2-9: *5.0 kΩ: Full Scale Error (FSE) vs. Temperature (V_{DD} = 5.5V, 2.7V, 1.8V).*

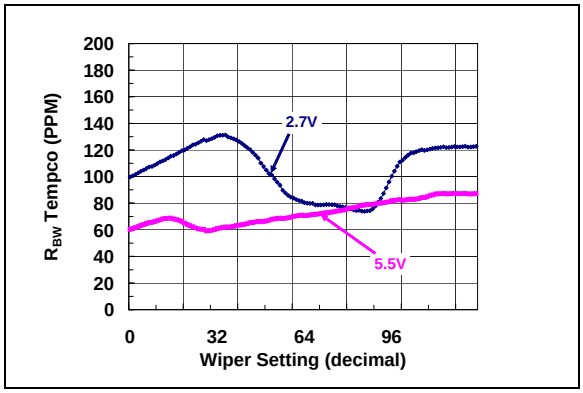

FIGURE 2-12: *5.0 kΩ: R_{BW} Tempco ΔR_{WB} / ΔT vs. Code.*

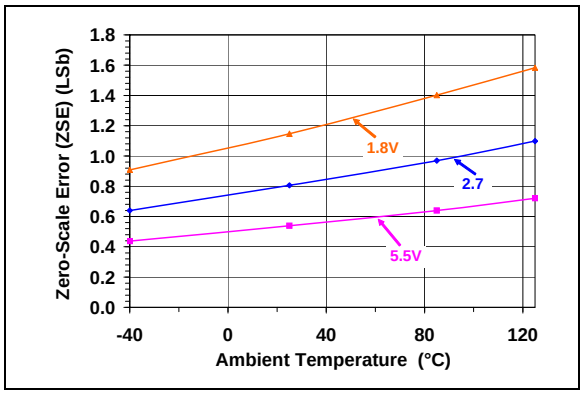

FIGURE 2-10: *5.0 kΩ: Zero Scale Error (ZSE) vs. Temperature (V_{DD} = 5.5V, 2.7V, 1.8V).*

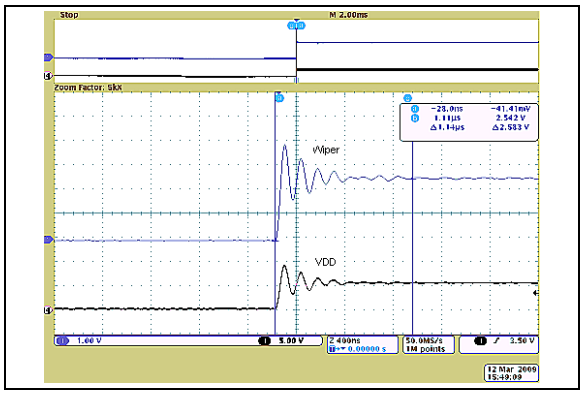

FIGURE 2-13: *5.0 kΩ: Power-Up Wiper Response Time.*

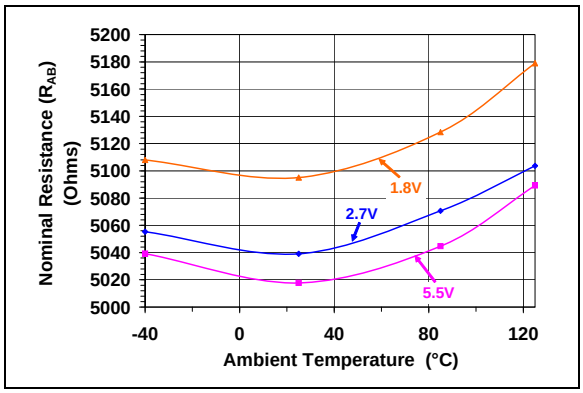

FIGURE 2-11: *5.0 kΩ: Nominal Resistance (Ω) vs. Temperature and V_{DD}.*

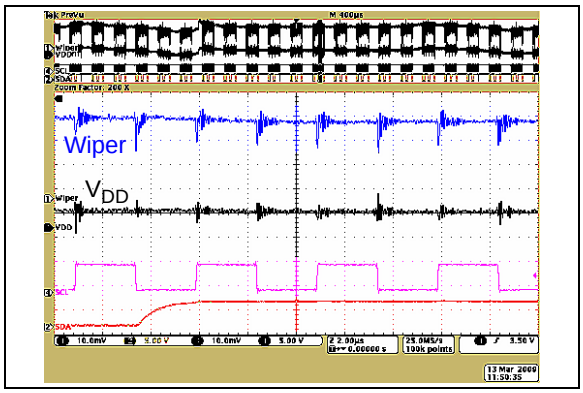

FIGURE 2-14: *5.0 kΩ: Digital Feedthrough (SCL signal coupling to Wiper pin).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

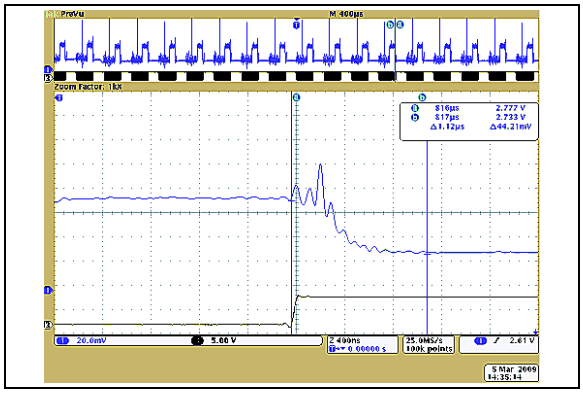

FIGURE 2-15: *5.0 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD}=5.5V).*

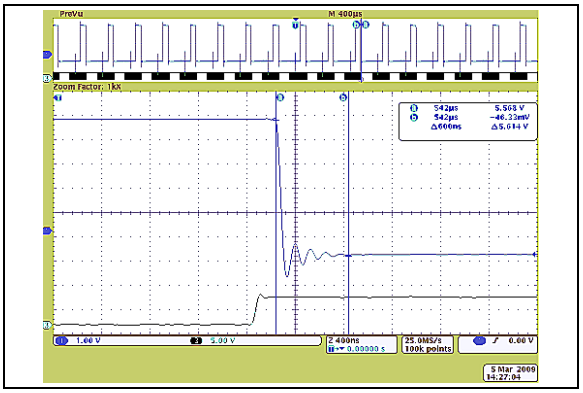

FIGURE 2-18: *5.0 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD}=5.5V).*

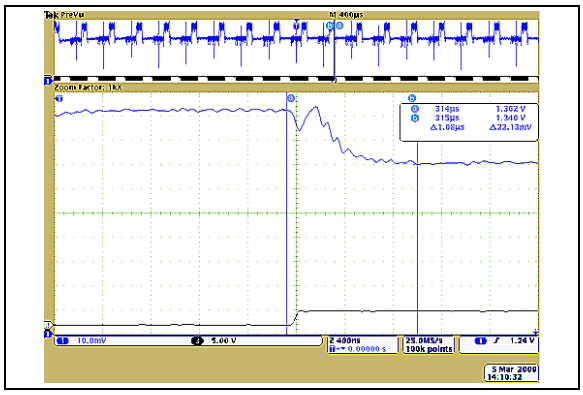

FIGURE 2-16: *5.0 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD}=2.7V).*

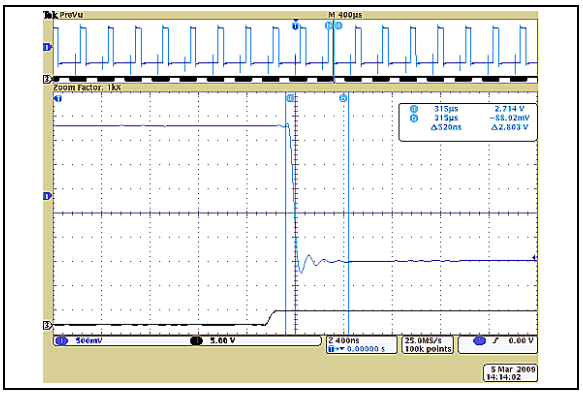

FIGURE 2-19: *5.0 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD}=2.7V).*

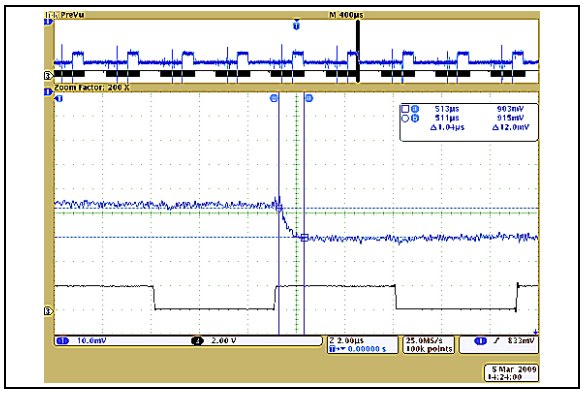

FIGURE 2-17: *5.0 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD}=1.8V).*

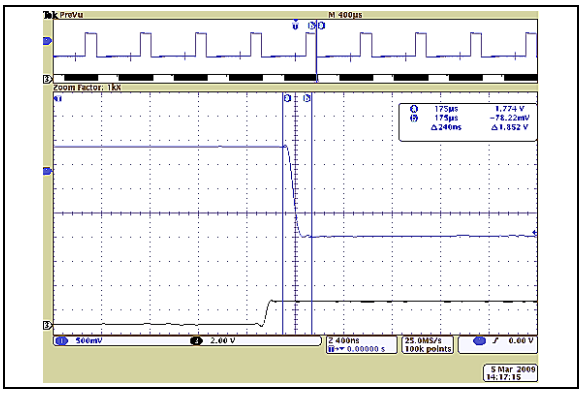

FIGURE 2-20: *5.0 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD}=1.8V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

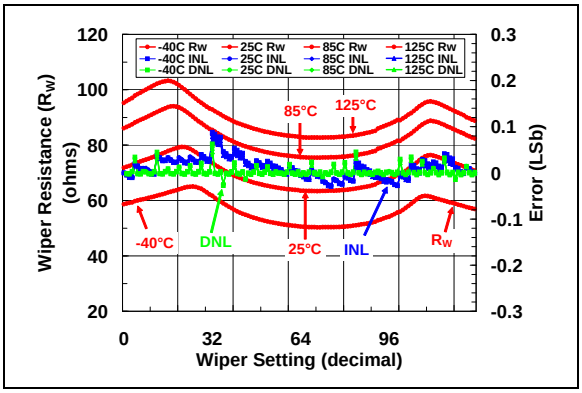


FIGURE 2-21: *10 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 5.5V). (A = V_{DD}, B = V_{SS}).*

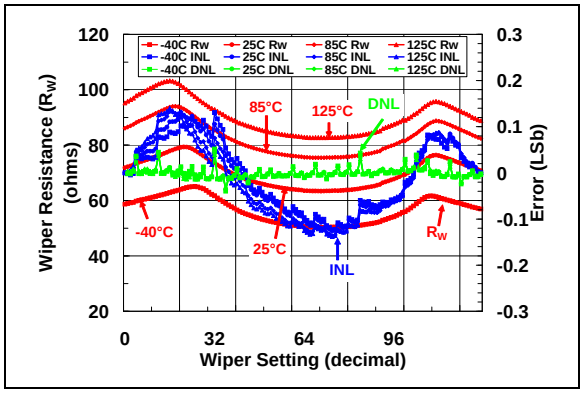


FIGURE 2-24: *10 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 5.5V).(I_W = 450 µA, B = V_{SS}).*

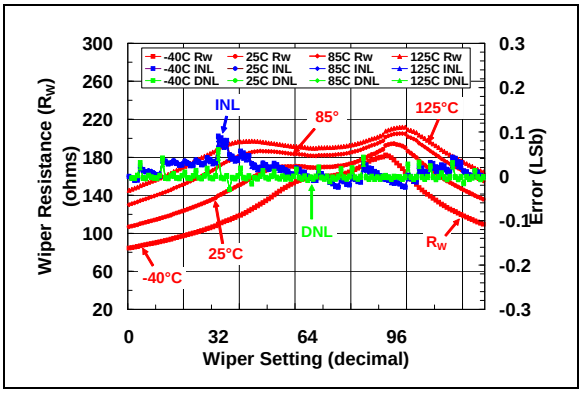


FIGURE 2-22: *10 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 2.7V). (A = V_{DD}, B = V_{SS}).*

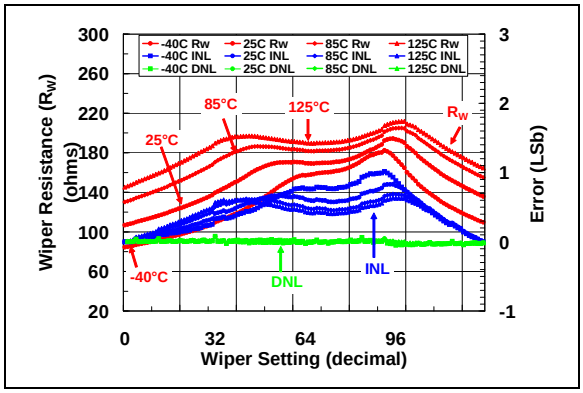
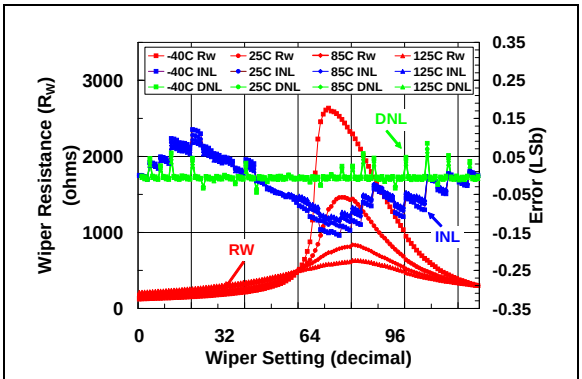
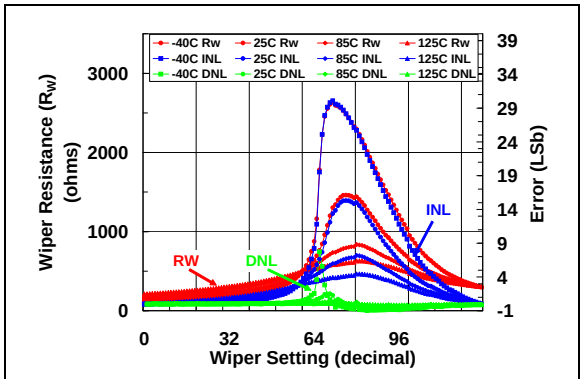


FIGURE 2-25: *10 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 2.7V).(I_W = 210 µA, B = V_{SS}).*



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-23: *10 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 1.8V). (A = V_{DD}, B = V_{SS}).*



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-26: *10 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 1.8V). (I_W =260 µA, B = V_{SS}).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

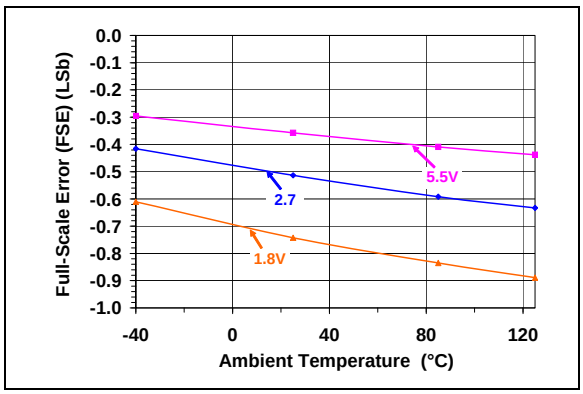

FIGURE 2-27: *10 kΩ: Full Scale Error (FSE) vs. Temperature (V_{DD} = 5.5V, 2.7V, 1.8V).*

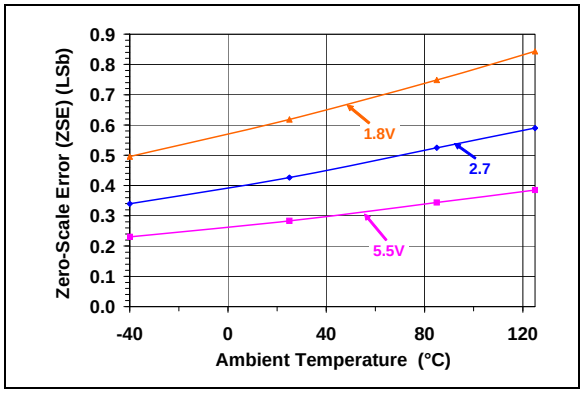

FIGURE 2-28: *10 kΩ: Zero Scale Error (ZSE) vs. Temperature (V_{DD} = 5.5V, 2.7V, 1.8V).*

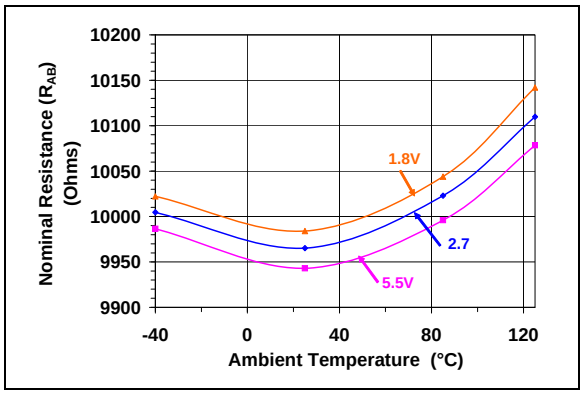

FIGURE 2-29: *10 kΩ: Nominal Resistance (Ω) vs. Temperature and V_{DD}.*

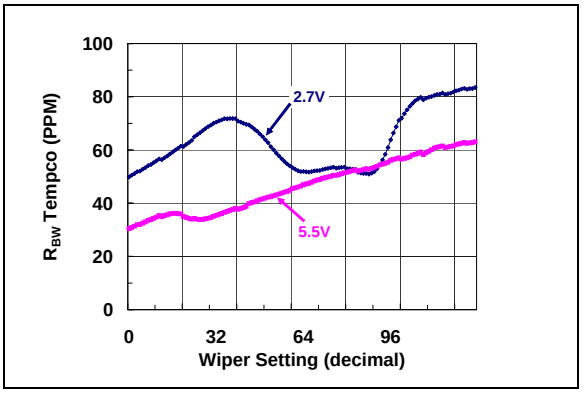

FIGURE 2-30: *10 kΩ: R_{BW} Tempco $\Delta R_{WB} / \Delta T$ vs. Code.*

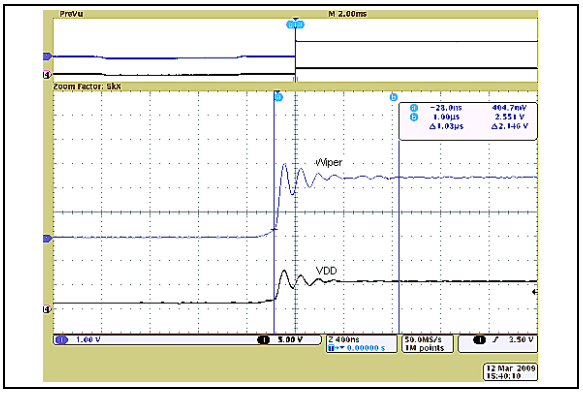

FIGURE 2-31: *10 kΩ: Power-Up Wiper Response Time.*

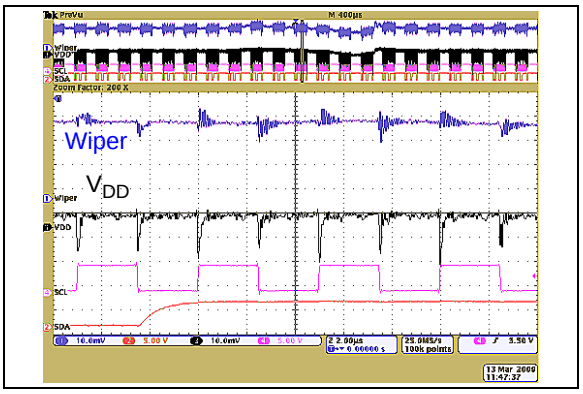

FIGURE 2-32: *10 kΩ: Digital Feedthrough (SCL signal coupling to Wiper pin).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

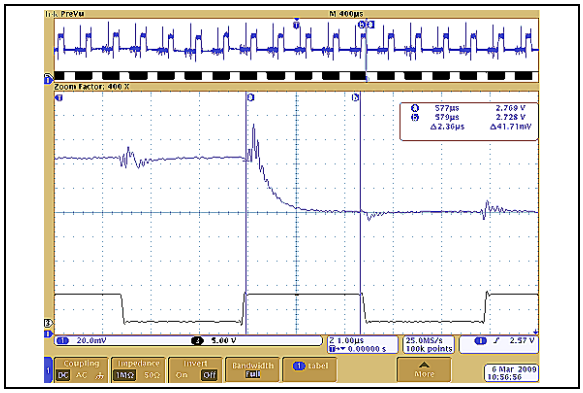

FIGURE 2-33: *10 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD}=5.5V).*

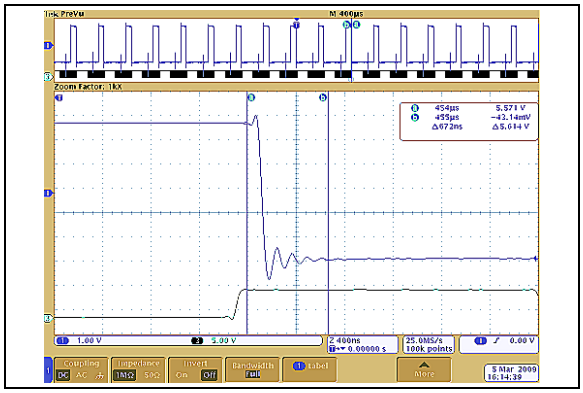

FIGURE 2-36: *10 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD}=5.5V).*

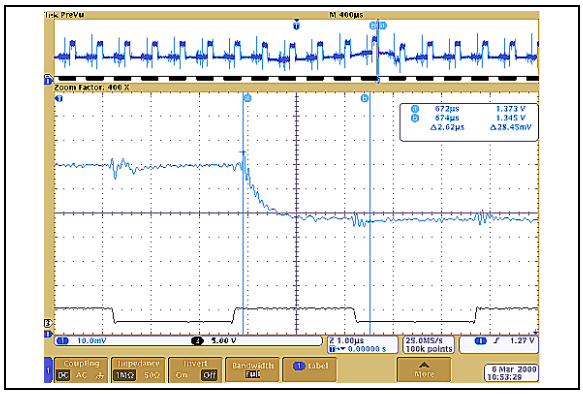

FIGURE 2-34: *10 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD}=2.7V).*

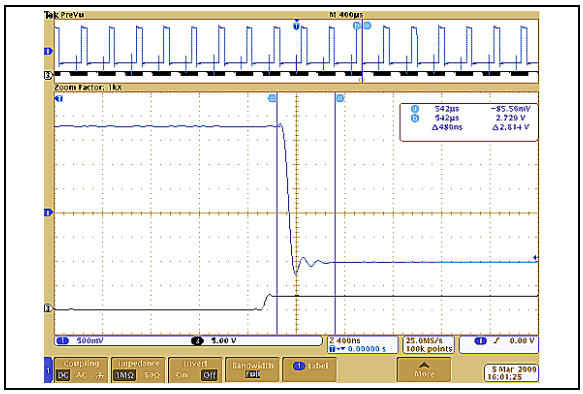

FIGURE 2-37: *10 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD}=2.7V).*

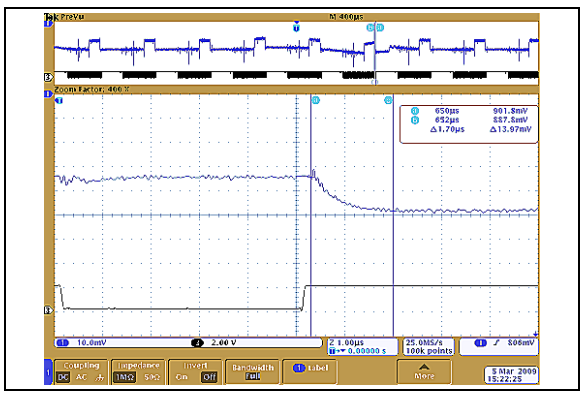

FIGURE 2-35: *10 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD}=1.8V).*

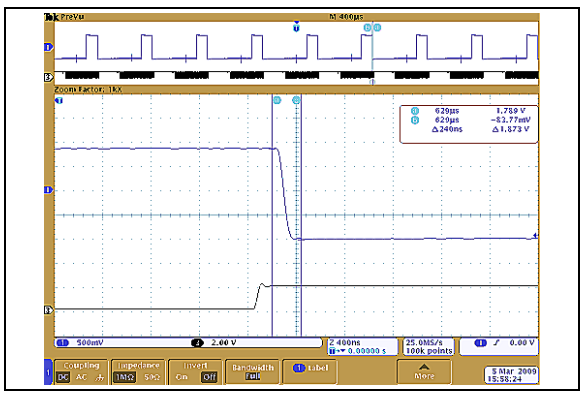

FIGURE 2-38: *10 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD}=1.8V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

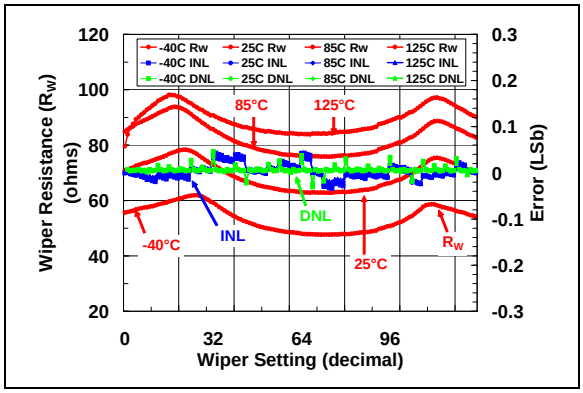


FIGURE 2-39: *50 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 5.5V).*

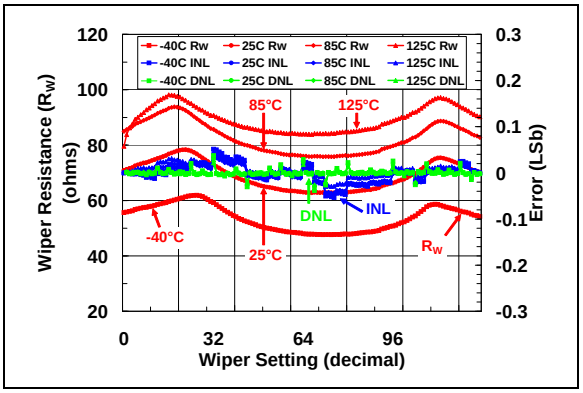


FIGURE 2-42: *50 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 5.5V).(I_W = 90 µA, B = V_{SS})*

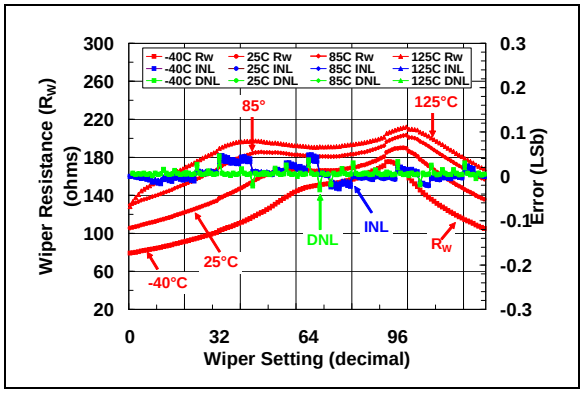


FIGURE 2-40: *50 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 2.7V).*

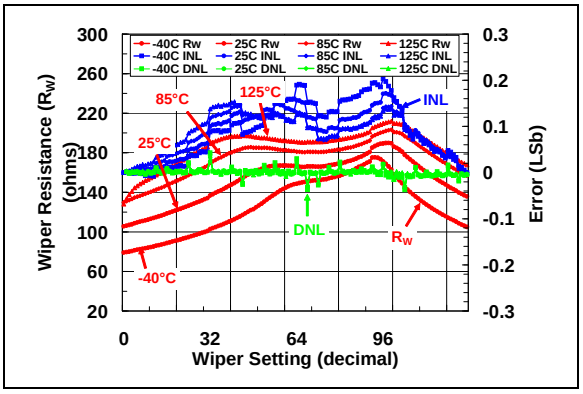
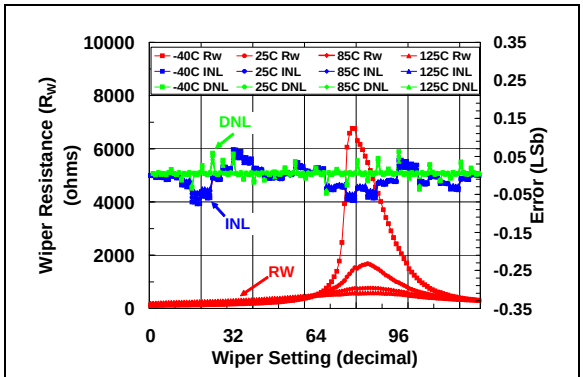
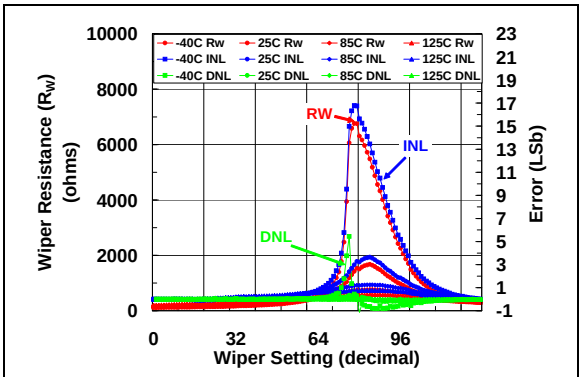


FIGURE 2-43: *50 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 2.7V).(I_W = 45 µA, B = V_{SS}).*



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-41: *50 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 1.8V).*



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-44: *50 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 1.8V). (I_W =260 µA, B = V_{SS}).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

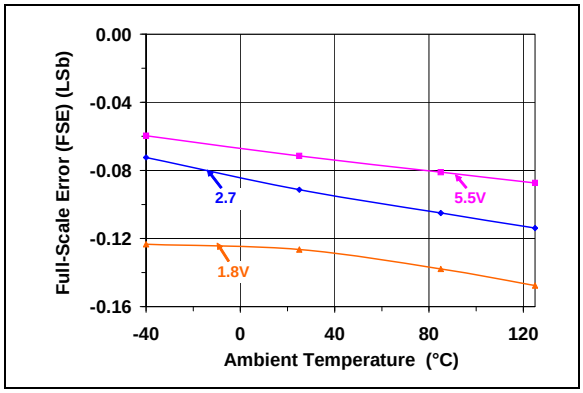

FIGURE 2-45: *50 kΩ: Full Scale Error (FSE) vs. Temperature (V_{DD} = 5.5V, 2.7V, 1.8V).*

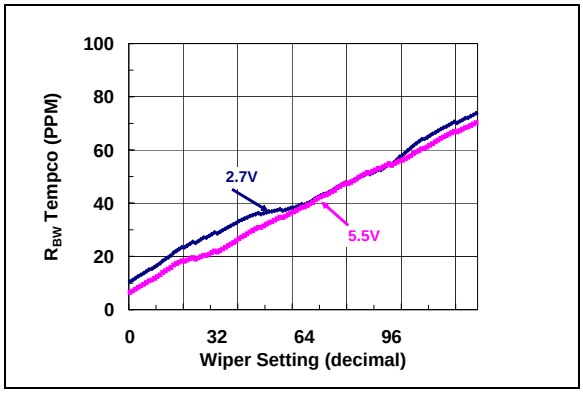

FIGURE 2-48: *50 kΩ: R_{BW} Tempco ΔR_{WB} / ΔT vs. Code.*

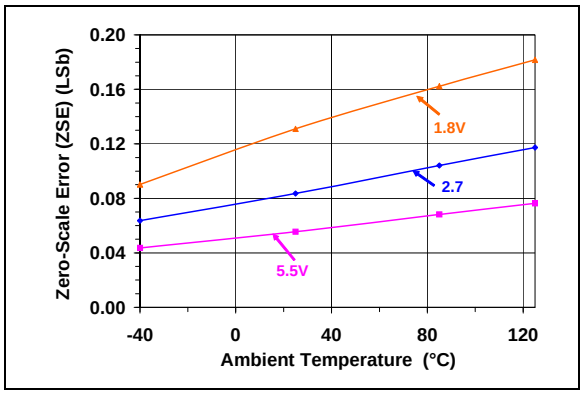

FIGURE 2-46: *50 kΩ: Zero Scale Error (ZSE) vs. Temperature (V_{DD} = 5.5V, 2.7V, 1.8V).*

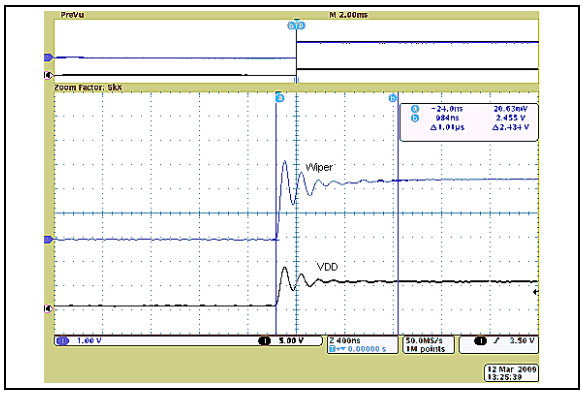

FIGURE 2-49: *50 kΩ: Power-Up Wiper Response Time.*

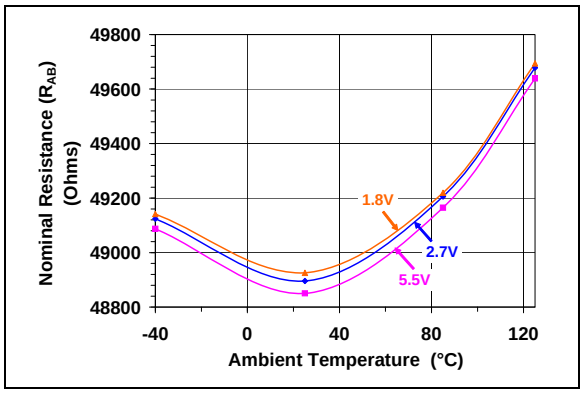

FIGURE 2-47: *50 kΩ: Nominal Resistance (Ω) vs. Temperature and V_{DD}.*

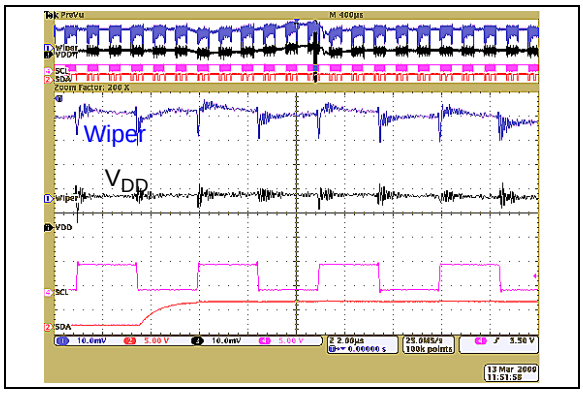

FIGURE 2-50: *50 kΩ: Digital Feedthrough (SCL signal coupling to Wiper pin).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

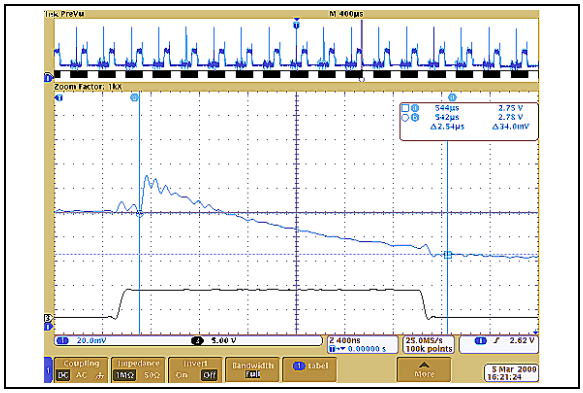

FIGURE 2-51: *50 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD}=5.5V).*

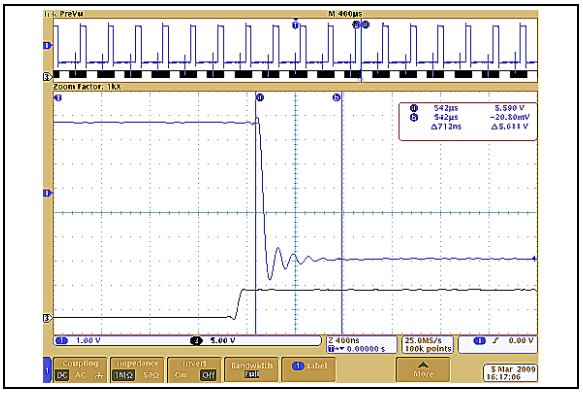

FIGURE 2-54: *50 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD}=5.5V).*

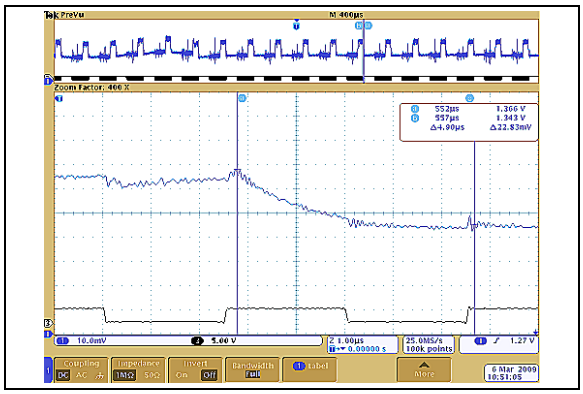

FIGURE 2-52: *50 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD}=2.7V).*

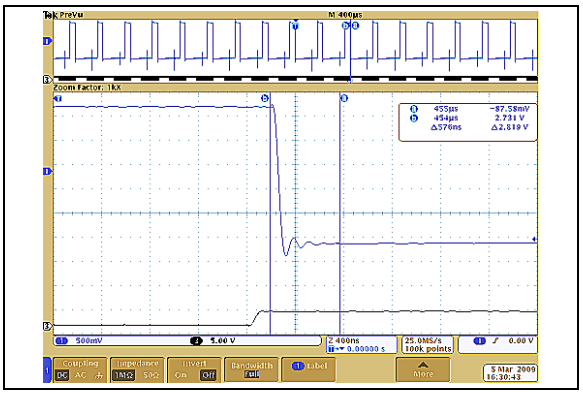

FIGURE 2-55: *50 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD}=2.7V).*

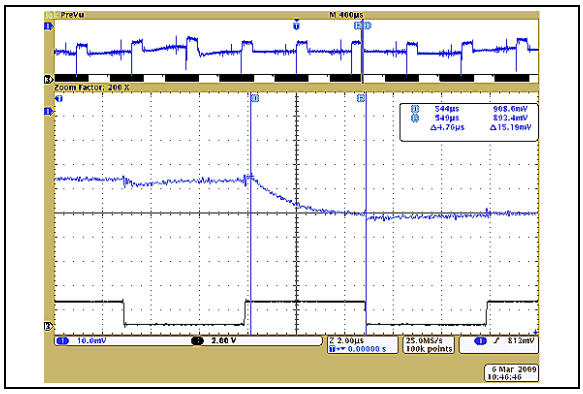

FIGURE 2-53: *50 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD}=1.8V).*

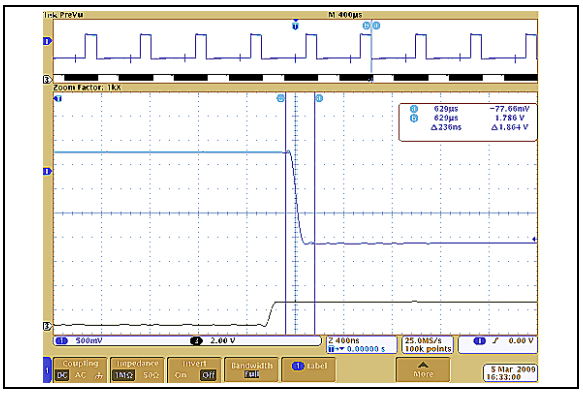

FIGURE 2-56: *50 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD}=1.8V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

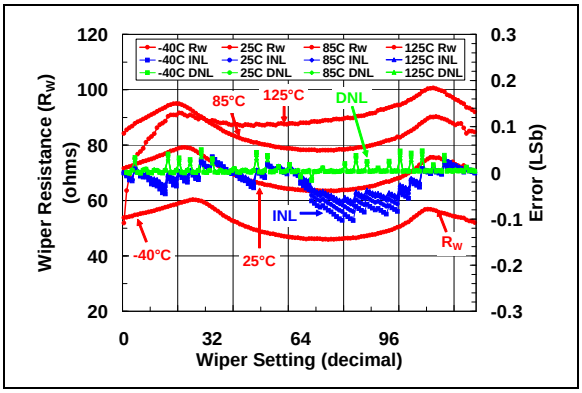


FIGURE 2-57: *100 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 5.5V).*

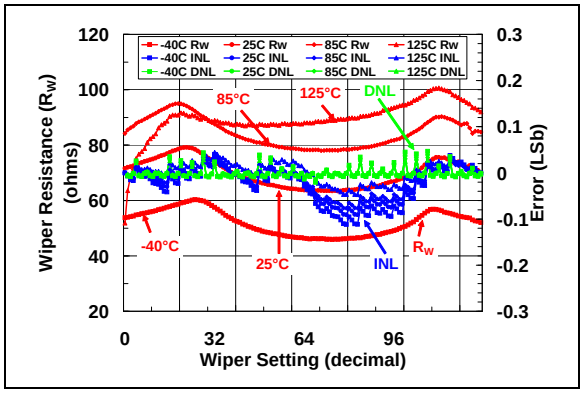


FIGURE 2-60: *100 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 5.5V). (I_W = 45 µA, B = V_{SS}).*

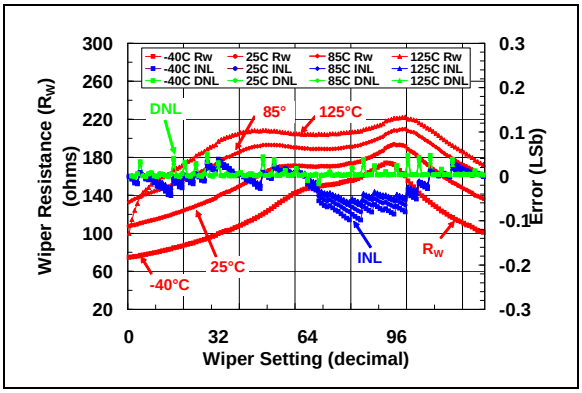


FIGURE 2-58: *100 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 2.7V).*

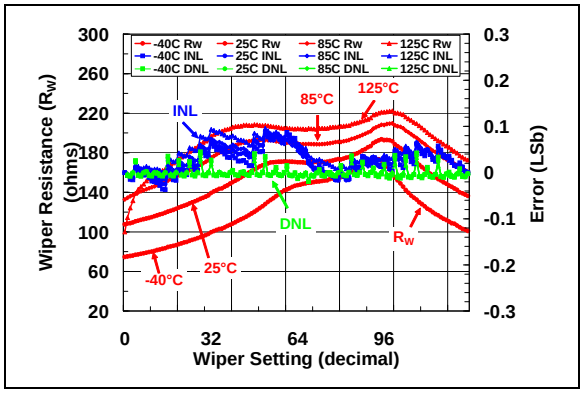
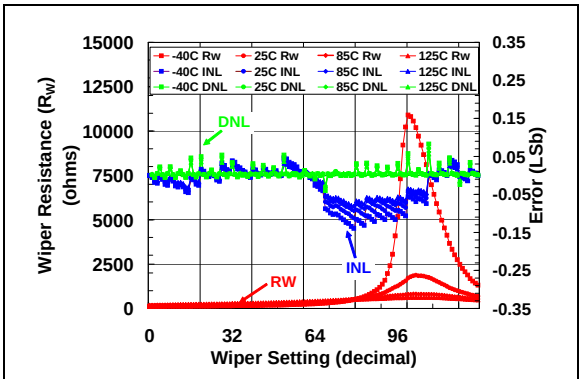
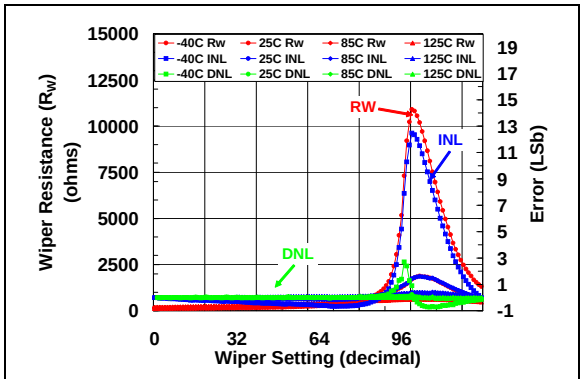


FIGURE 2-61: *100 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 2.7V). (I_W = 21 µA, B = V_{SS}).*



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-59: *100 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 1.8V).*



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-62: *100 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature (V_{DD} = 1.8V). (I_W =260 µA, B = V_{SS}).*

Downloaded from Arrow.com.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

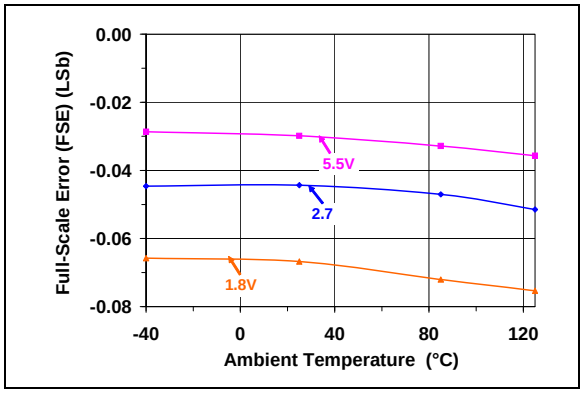


FIGURE 2-63: *100 kΩ: Full Scale Error (FSE) vs. Temperature (V_{DD} = 5.5V, 2.7V, 1.8V).*

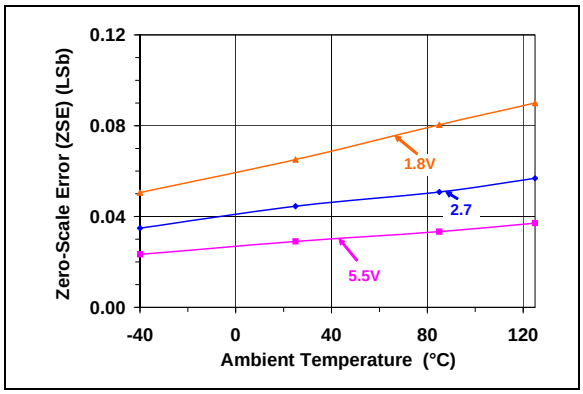


FIGURE 2-64: *100 kΩ: Zero Scale Error (ZSE) vs. Temperature (V_{DD} = 5.5V, 2.7V, 1.8V).*

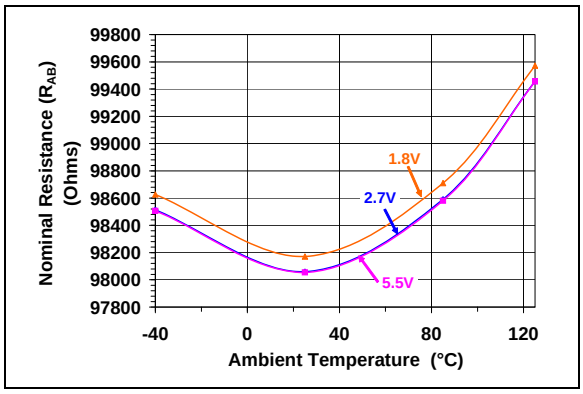


FIGURE 2-65: *100 kΩ: Nominal Resistance (Ω) vs. Temperature and V_{DD}.*

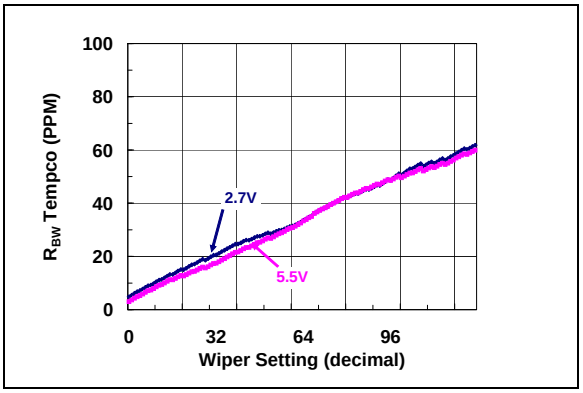


FIGURE 2-66: *100 kΩ: R_{BW} Tempco $\Delta R_{WB} / \Delta T$ vs. Code.*

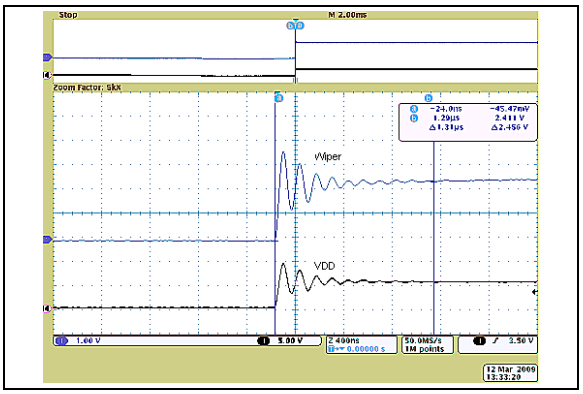


FIGURE 2-67: *100 kΩ: Power-Up Wiper Response Time.*

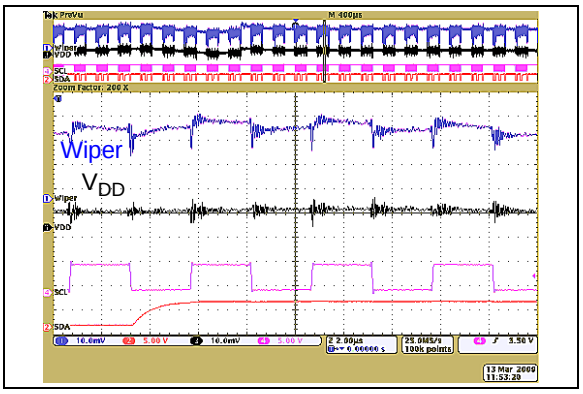


FIGURE 2-68: *100 kΩ: Digital Feedthrough (SCL signal coupling to Wiper pin).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

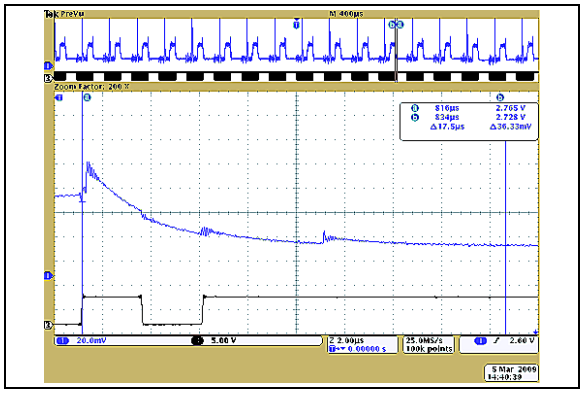

FIGURE 2-69: *100 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD} = 5.5V).*

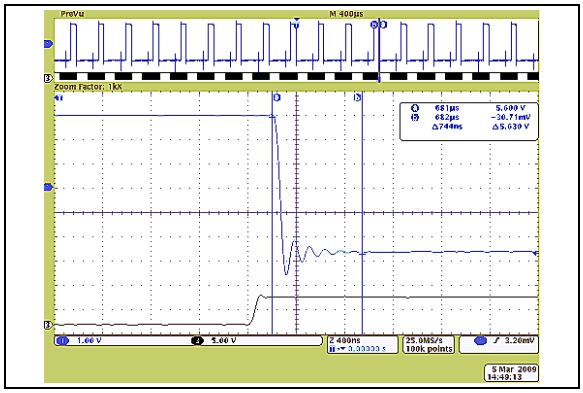

FIGURE 2-72: *100 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD} = 5.5V).*

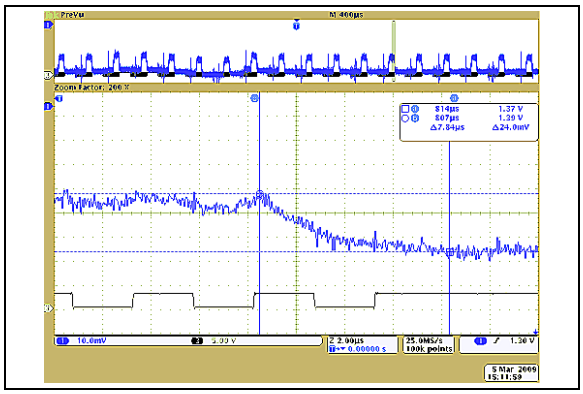

FIGURE 2-70: *100 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD} = 2.7V).*

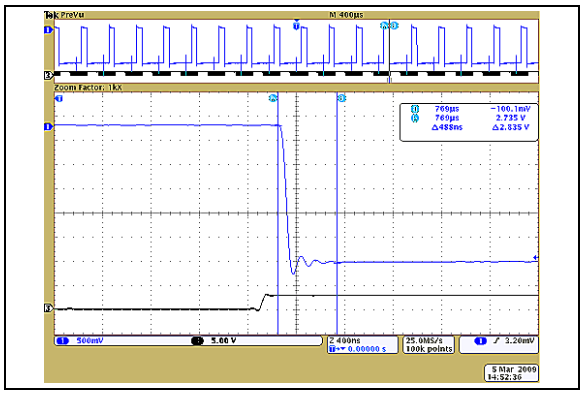

FIGURE 2-73: *100 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD} = 2.7V).*

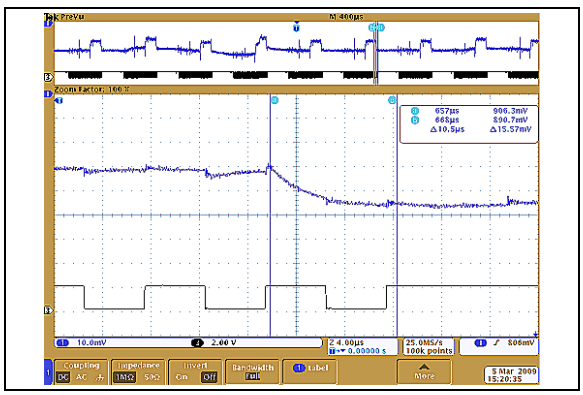

FIGURE 2-71: *100 kΩ: Write Wiper (40h → 3Fh) Settling Time (V_{DD} = 1.8V).*

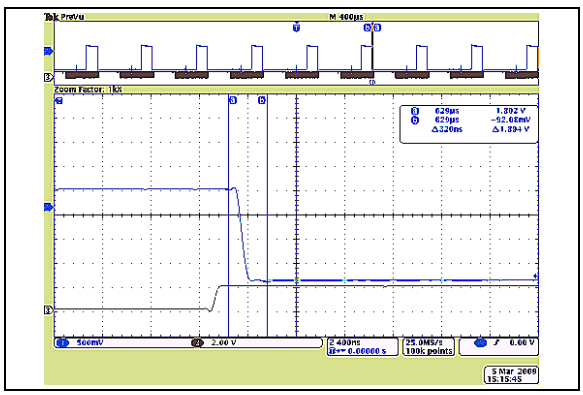

FIGURE 2-74: *100 kΩ: Write Wiper (FFh → 00h) Settling Time (V_{DD} = 1.8V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

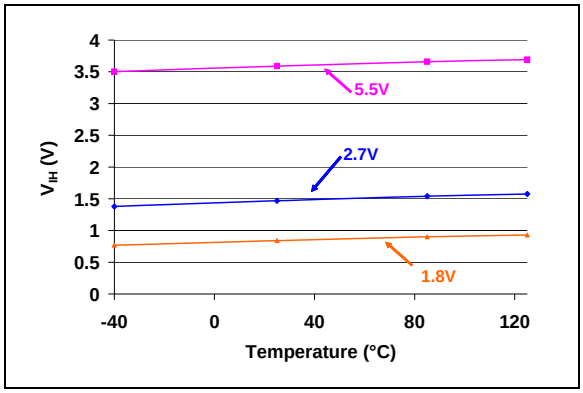

FIGURE 2-75: *V_{IH} (SCL, SDA) vs. V_{DD} and Temperature.*

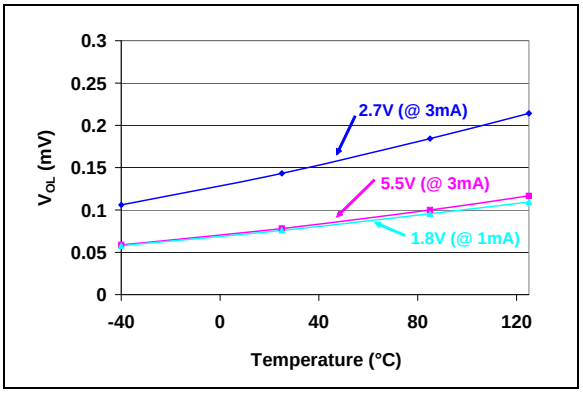

FIGURE 2-77: *V_{OL} (SDA) vs. V_{DD} and Temperature.*

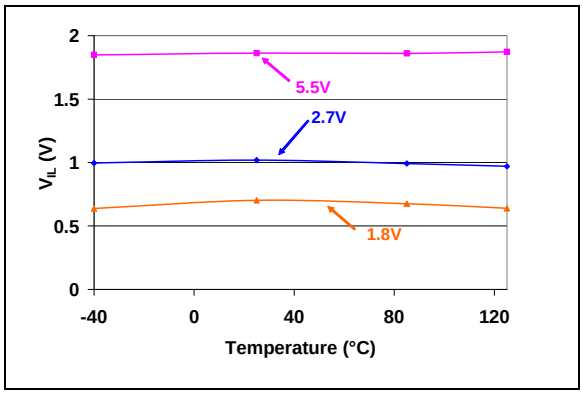

FIGURE 2-76: *V_{IL} (SCL, SDA) vs. V_{DD} and Temperature.*

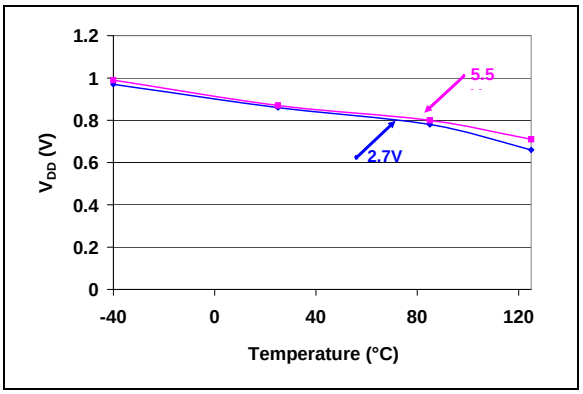

FIGURE 2-78: *POR/BOR Trip point vs. V_{DD} and Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

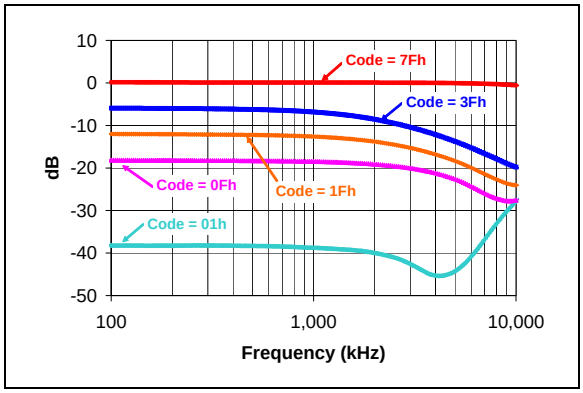

FIGURE 2-79: *5 kΩ – Gain vs. Frequency (-3 dB).*

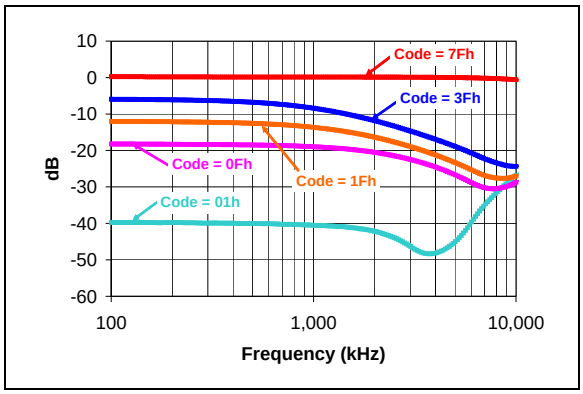

FIGURE 2-80: *10 kΩ – Gain vs. Frequency (-3 dB).*

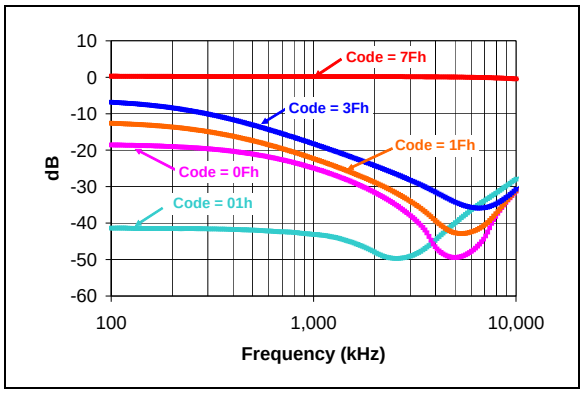

FIGURE 2-81: *50 kΩ – Gain vs. Frequency (-3 dB).*

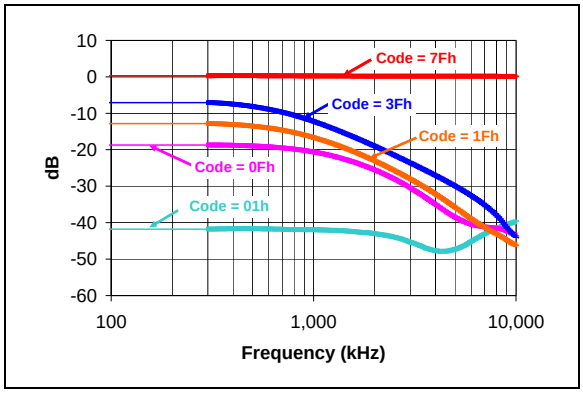

FIGURE 2-82: *100 kΩ – Gain vs. Frequency (-3 dB).*

2.1 Test Circuits

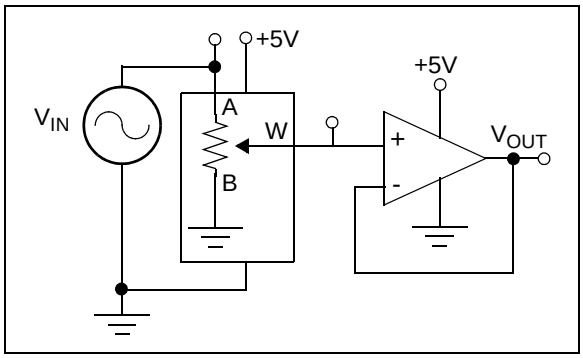

FIGURE 2-83: *Gain vs. Frequency Test (-3 dB).*

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NOTES:

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.
Additional descriptions of the device pins follow.

TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP40D17/18/19

Pin Name	Pin Number			Pin Type	Buffer Type	Function
	MCP40D17 (SC70-6)	MCP40D18 (SC70-6)	MCP40D19 (SC70-5)			
V_{DD}	1	1	1	P	—	Positive Power Supply Input
V_{SS}	2	2	2	P	—	Ground
SCL	3	3	3	I/O	ST (OD)	I^2C Serial Clock pin
SDA	4	4	4	I/O	ST (OD)	I^2C Serial Data pin
B	5	—	—	I/O	A	Potentiometer Terminal B
W	6	5	5	I/O	A	Potentiometer Wiper Terminal
A	—	6	—	I/O	A	Potentiometer Terminal A

Legend: A = Analog input ST (OD) = Schmitt Trigger with Open Drain
I = Input O = Output I/O = Input/Output P = Power

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3.1 Positive Power Supply Input (V_{DD})

The V_{DD} pin is the device's positive power supply input. The input power supply is relative to V_{SS} and can range from 1.8V to 5.5V. A de-coupling capacitor on V_{DD} (to V_{SS}) is recommended to achieve maximum performance.

While the device's voltage is in the range of $1.8V \leq V_{DD} < 2.7V$, the Resistor Network's electrical performance of the device may not meet the data sheet specifications.

3.2 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

3.3 I^2C Serial Clock (SCL)

The SCL pin is the serial clock pin of the I^2C interface. The MCP40D17/18/19 acts only as a slave and the SCL pin accepts only external serial clocks. The SCL pin is an open-drain output. Refer to **Section 5.0 "Serial Interface - I^2C Module"** for more details of I^2C Serial Interface communication.

3.4 I^2C Serial Data (SDA)

The SDA pin is the serial data pin of the I^2C interface. The SDA pin has a Schmitt trigger input and an open-drain output. Refer to **Section 5.0 "Serial Interface - I^2C Module"** for more details of I^2C Serial Interface communication.

3.5 Potentiometer Terminal B

The terminal B pin (available on some devices) is connected to the internal potentiometer's terminal B.

The potentiometer's terminal B is the fixed connection to the Zero Scale (0x00 tap) wiper value of the digital potentiometer.

The terminal B pin is available on the MCP40D17 device. The terminal B pin does not have a polarity relative to the terminal W pin. The terminal B pin can support both positive and negative current. The voltage on terminal B must be between V_{SS} and V_{DD}.

The terminal B pin is not available on the MCP40D18 and MCP40D19 devices. For these devices, the potentiometer's terminal B is internally connected to V_{SS}.

3.6 Potentiometer Wiper (W) Terminal

The terminal W pin is connected to the internal potentiometer's terminal W (the wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The terminal W pin does not have a polarity relative to terminals A or B pins. The terminal W pin can support both positive and negative current. The voltage on terminal W must be between V_{SS} and V_{DD}.

3.7 Potentiometer Terminal A

The terminal A pin (available on some devices) is connected to the internal potentiometer's terminal A.

The potentiometer's terminal A is the fixed connection to the Full Scale (0x7F tap) wiper value of the digital potentiometer.

The terminal A pin is available on the MCP40D18 devices. The terminal A pin does not have a polarity relative to the terminal W pin. The terminal A pin can support both positive and negative current. The voltage on terminal A must be between V_{SS} and V_{DD}.

The terminal A pin is not available on the MCP40D17 and MCP40D19 devices. For these devices, the potentiometer's terminal A is internally floating.

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4.0 GENERAL OVERVIEW

The MCP40D17/18/19 devices are general purpose digital potentiometers intended to be used in applications where a programmable resistance with moderate bandwidth is desired.

This Data Sheet covers a family of three Digital Potentiometer and Rheostat devices. The MCP40D18 device is the Potentiometer configuration, while the MCP40D17 and MCP40D19 devices are the Rheostat configuration.

Applications generally suited for the MCP40D17/18/19 devices include:

- Computer Servers
- Set point or offset trimming
- Sensor calibration
- Selectable gain and offset amplifier designs
- Cost-sensitive mechanical trim pot replacement

As the **Device Block Diagram** shows, there are four main functional blocks. These are:

- **POR/BOR Operation**
- **Serial Interface - I^2C Module**
- **Resistor Network**

The POR/BOR operation and the Memory Map are discussed in this section and the I^2C and Resistor Network operation are described in their own sections. The **Serial Commands** commands are discussed in **Section 5.4**.

4.1 POR/BOR Operation

The Power-on Reset is the case where the device is having power applied to it from V_{SS}. The Brown-out Reset occurs when a device had power applied to it, and that power (voltage) drops below the specified range.

The devices RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the Resistor Network's electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its volatile memory if the proper serial command is executed.

Table 4-1 shows the digital pot's level of functionality across the entire V_{DD} range, while Figure 4-1 illustrates the Power-up and Brown-out functionality.

4.1.1 POWER-ON RESET

When the device powers up, the device V_{DD} will cross the V_{POR}/V_{BOR} voltage. Once the V_{DD} voltage crosses the V_{POR}/V_{BOR} voltage, the following happens:

- Volatile wiper register is loaded with the default wiper value (3Fh)
- The device is capable of digital operation

4.1.2 BROWN-OUT RESET

When the device powers down, the device V_{DD} will cross the V_{POR}/V_{BOR} voltage. Once the V_{DD} voltage decreases below the V_{POR}/V_{BOR} voltage the following happens:

- Serial Interface is disabled

If the V_{DD} voltage decreases below the V_{RAM} voltage the following happens:

- Volatile wiper registers may become corrupted

As the voltage recovers above the V_{POR}/V_{BOR} voltage see **Section 4.1.1 "Power-on Reset"**.

Serial commands not completed due to a Brown-out condition may cause the memory location to become corrupted.

4.1.3 WIPER REGISTER (RAM)

The Wiper Register is volatile memory that starts functioning at the RAM retention voltage (V_{RAM}). The Wiper Register will be loaded with the default wiper value when V_{DD} will rise above the V_{POR}/V_{BOR} voltage.

4.1.4 DEVICE CURRENTS

The current of the device can be classified into two modes of the device operation. These are:

- Serial Interface Inactive (Static Operation)
- Serial Interface Active

Static Operation occurs when a Stop condition is received. Static Operation is exited when a Start condition is received.

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TABLE 4-1: DEVICE FUNCTIONALITY AT EACH V_{DD} REGION (NOTE 1)

V_{DD} Level	Serial Interface	Potentiometer Terminals	Wiper Setting	Comment
$V_{DD} < V_{BOR} < 1.8V$	Ignored	"unknown"	Unknown	
$V_{BOR} \leq V_{DD} < 1.8V$	"Unknown"	Operational with reduced electrical specs	Wiper Register loaded with POR/BOR value	
$1.8V \leq V_{DD} < 2.7V$	Accepted	Operational with reduced electrical specs	Wiper Register determines Wiper Setting	Electrical performance may not meet the data sheet specifications.
$2.7V \leq V_{DD} \leq 5.5V$	Accepted	Operational	Wiper Register determines Wiper Setting	Meets the data sheet specifications

Note 1: For system voltages below the minimum operating voltage, the customer will be recommended to use a voltage supervisor to hold the system in reset. This will ensure that MCP4017/18/19 commands are not attempted out of the operating range of the device.

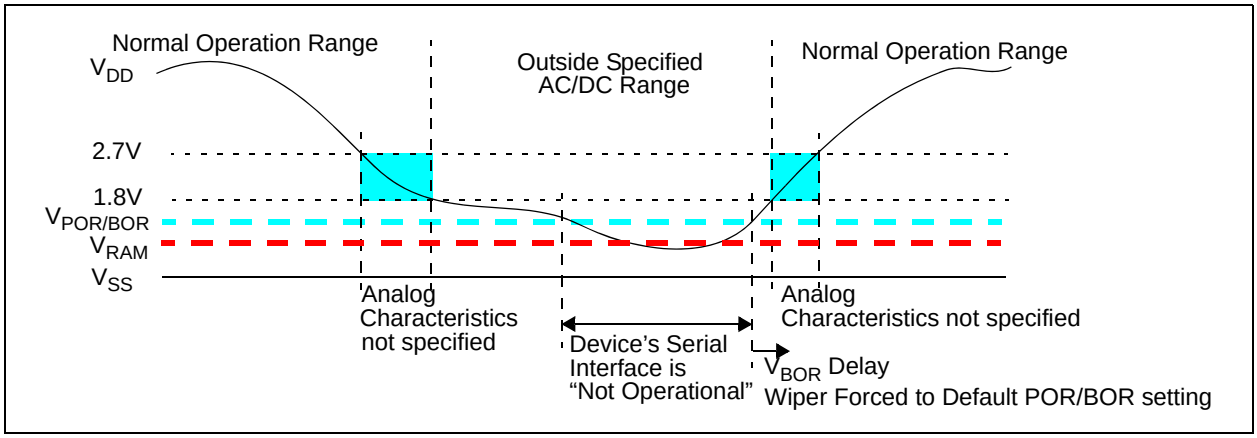

FIGURE 4-1: *Power-up and Brown-out.*

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5.0 SERIAL INTERFACE - I²C MODULE

A 2-wire I²C serial protocol is used to write or read the digital potentiometer's wiper register. The I²C protocol utilizes the SCL input pin and SDA input/output pin.

The I²C serial interface supports the following features:

- Slave mode of operation
- 7-bit addressing
- The following clock rate modes are supported:
  - Standard mode, bit rates up to 100 kb/s
  - Fast mode, bit rates up to 400 kb/s
- Support Multi-Master Applications

The serial clock is generated by the Master.

The I²C Module is compatible with the Phillips I²C specification. Philips only defines the field types, field lengths, timings, etc. of a frame. The frame *content* defines the behavior of the device. The frame content for the MCP40D17, MCP40D18, and MCP40D19 devices are defined in this section of the data sheet.

Figure 5-1 shows a typical I²C bus configurations.

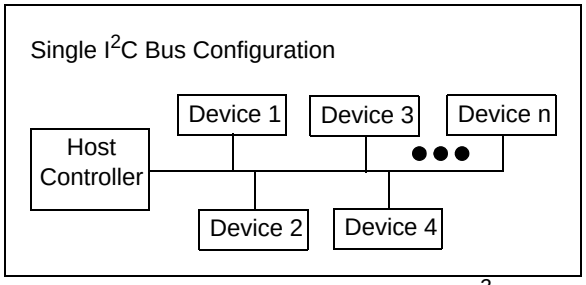

FIGURE 5-1: *Typical Application I²C Bus Configurations.*

Refer to **Section 2.0 "Typical Performance Curves"**, AC/DC Electrical Characteristics table for detailed input threshold and timing specifications.

5.1 I²C I/O Considerations

I²C specifications require active low, passive high functionality on devices interfacing to the bus. Since devices may be operating on separate power supply sources, ESD clamping diodes are not permitted. The specification recommends using open drain transistors tied to V_{SS} (common) with a pull-up resistor. The specification makes some general recommendations on the size of this pull-up, but does not specify the exact value since bus speeds and bus capacitance impacts the pull-up value for optimum system performance.

Common pull-up values range from 1 kΩ to a maximum of ~10 kΩ. Power sensitive applications tend to choose higher values to minimize current losses during communication but these applications also typically utilize lower V_{DD}.

The SDA and SCL float (are not driving) when the device is powered down.

A "glitch" filter is on the SCL and SDA pins when the pin is an input. When these pins are an output, there is a slew rate control of the pin that is independent of device frequency.

5.1.1 SLOPE CONTROL

The device implements slope control on the SDA output. The slope control is defined by the fast mode specifications.

For Fast (FS) mode, the device has spike suppression and Schmidt trigger inputs on the SDA and SCL pins.

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5.2 I²C Bit Definitions

I²C bit definitions include:

- **Start Bit**
- **Data Bit**
- **Acknowledge (A) Bit**
- **Repeated Start Bit**
- **Stop Bit**
- **Clock Stretching**

Figure 5-8 shows the waveform for these states.

5.2.1 START BIT

The Start bit (see Figure 5-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is “High”.

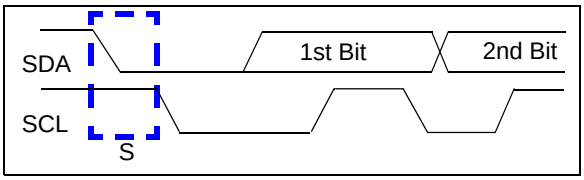

FIGURE 5-2: *Start Bit.*

5.2.2 DATA BIT

The SDA signal may change state while the SCL signal is Low. While the SCL signal is High, the SDA signal MUST be stable (see Figure 5-3).

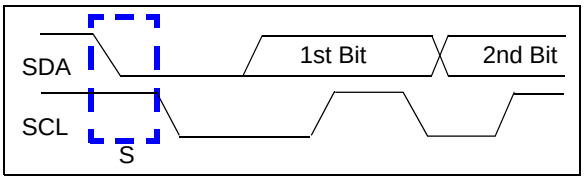

FIGURE 5-3: *Data Bit.*

5.2.3 ACKNOWLEDGE (A) BIT

The A bit (see Figure 5-4) is a response from the Slave device to the Master device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically the Slave device will supply an A response after the Start bit and 8 “data” bits have been received. The A bit will have the SDA signal low.

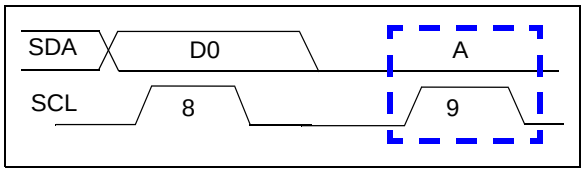

FIGURE 5-4: *Acknowledge Waveform.*

If the Slave Address is not valid, the Slave Device will issue a Not A ($\overline{A}$). The $\overline{A}$ bit will have the SDA signal high.

If an error condition occurs (such as an $\overline{A}$ instead of A) then a START bit must be issued to reset the command state machine.

TABLE 5-1: MCP40D17/18/19 A / $\overline{A}$ RESPONSES

Event	Acknowledge Bit Response	Comment
General Call	$\overline{A}$	
Slave Address valid	A	
Slave Address not valid	$\overline{A}$	
Bus Collision	N.A.	I²C Module Resets, or a “Don’t Care” if the collision occurs on the Masters “Start bit”.

5.2.4 REPEATED START BIT

The Repeated Start bit (see Figure 5-5) indicates the current Master Device wishes to continue communicating with the current Slave Device without releasing the I²C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is “High”.

Note 1: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low to high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

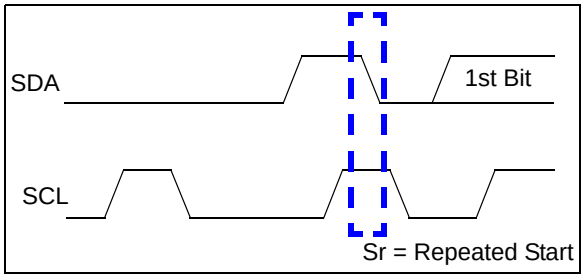

FIGURE 5-5: *Repeat Start Condition Waveform.*

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5.2.5 STOP BIT

The Stop bit (see Figure 5-6) Indicates the end of the I^2C Data Transfer Sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is “High”.

A Stop bit resets the I^2C interface of the other devices.

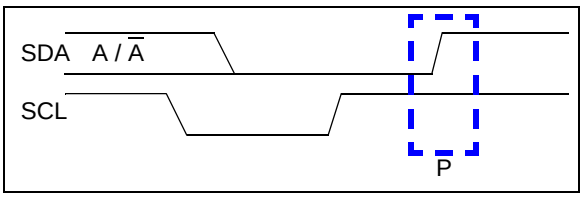

FIGURE 5-6: *Stop Condition Receive or Transmit Mode.*

5.2.6 CLOCK STRETCHING

“Clock Stretching” is something that the Secondary Device can do, to allow additional time to “respond” to the “data” that has been received.

The MCP40D17/18/19 will not strech the clock signal (SCL) since memory read accesses occur fast enough.

5.2.7 ABORTING A TRANSMISSION

If any part of the I^2C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a START or STOP condition. This is done so that noisy transmissions (usually an extra START or STOP condition) are aborted before they corrupt the device.

5.2.8 IGNORING AN I^2C TRANSMISSION AND “FALLING OFF” THE BUS

The MCP40D17/18/19 expects to receive entire, valid I^2C commands and will assume any command not defined as a valid command is due to a bus corruption and will enter a passive high condition on the SDA signal. All signals will be ignored until the next valid START condition and CONTROL BYTE are received.

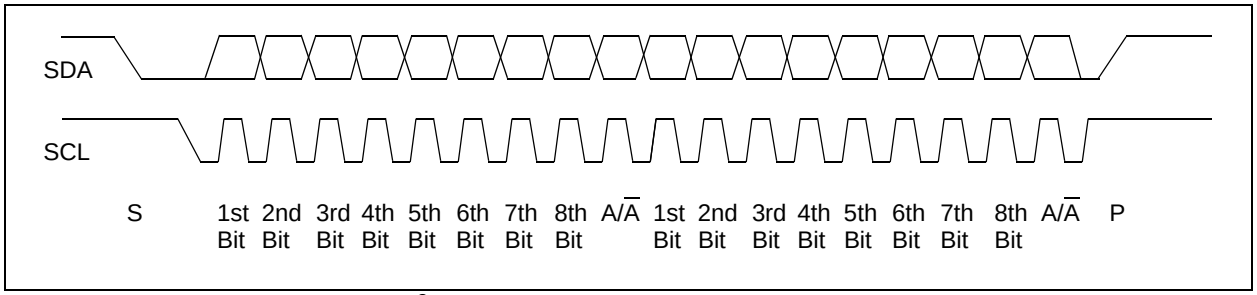

FIGURE 5-7: *Typical 16-bit I^2C Waveform Format.*

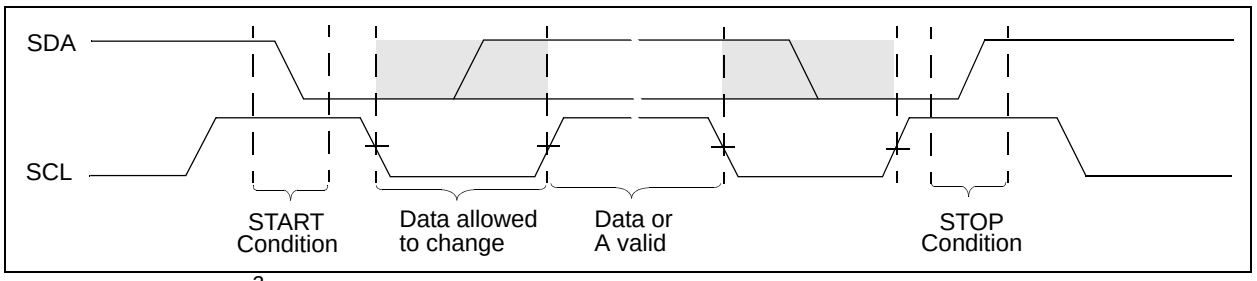

FIGURE 5-8: *I^2C Data States and Bit Sequence.*

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5.2.9 I²C COMMAND PROTOCOL

The MCP40D17/18/19 is a slave I²C device which supports 7-bit slave addressing. The slave address contains seven fixed bits. Figure 5-9 shows the control byte format.

5.2.9.1 Control Byte (Slave Address)

The Control Byte is always preceded by a START condition. The Control Byte contains the slave address consisting of seven fixed bits and the R/$\overline{W}$ bit. Figure 5-9 shows the control byte format and Table 5-2 shows the I²C address for the devices.

All devices are offered with the I²C slave address of "0101110", while the MCP40D18 also offers a second standard I²C slave address of "0111110".

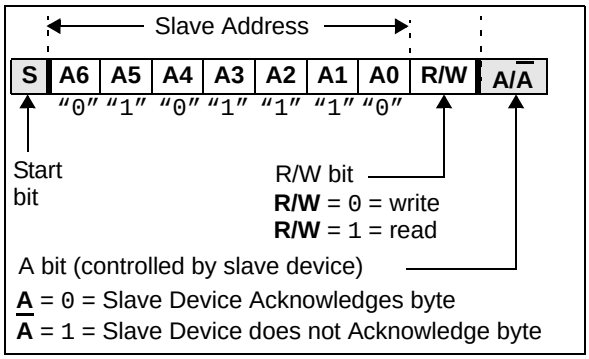

FIGURE 5-9: *Slave Address Bits in the I²C Control Byte (Slave Address = "0101110").*

TABLE 5-2: DEVICE I²C ADDRESS

Device	I²C Address	Comment
MCP40D17	'0101110'	
MCP40D18	'0101110'	MCP40D18-xxxE/LT
	'0111110'	MCP40D18-xxx**A**E/LT
MCP40D19	'0101110'	

5.2.9.2 Hardware Address Pins

The MCP40D17/MCP40D18/MCP40D19 does not support hardware address bits.

5.2.10 GENERAL CALL

The General Call is a method that the Master device can communicate with all other Slave devices.

The MCP40D17/18/19 devices do not respond to General Call address and commands, and therefore the communications are Not Acknowledged.

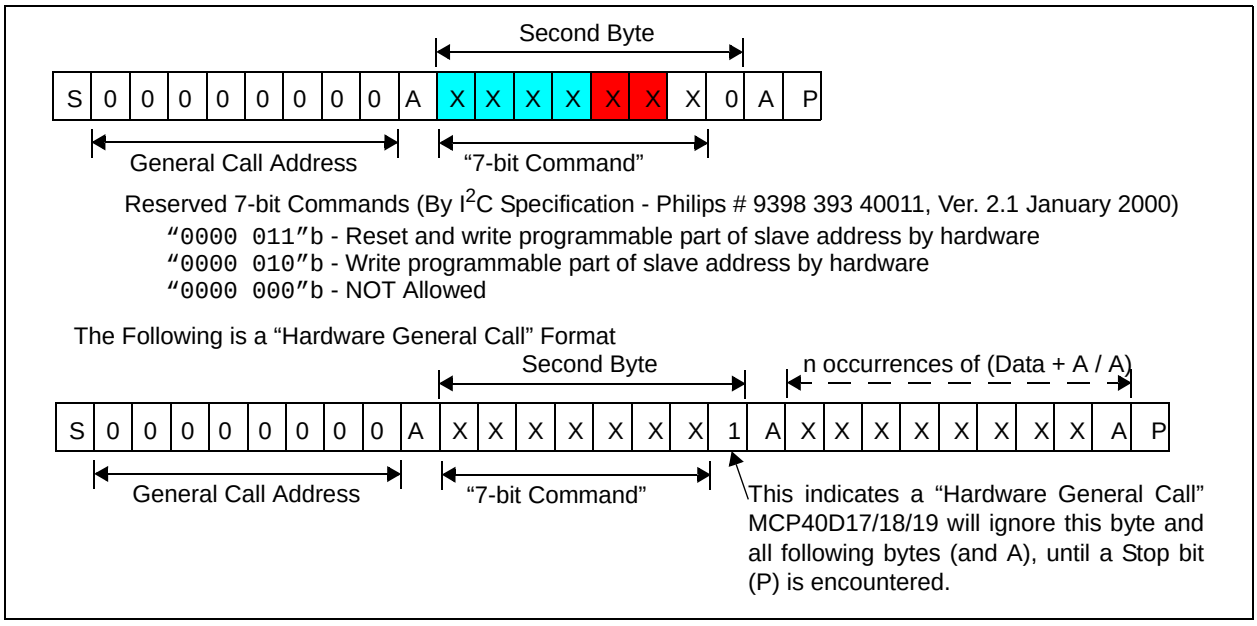

FIGURE 5-10: *General Call Formats.*

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5.3 Software Reset Sequence

Note:	This technique should be supported by any I²C compliant device. The 24XXXX I²C Serial EEPROM devices support this technique, which is documented in AN1028.

At times it may become necessary to perform a Software Reset Sequence to ensure the MCP40D17/18/19 device is in a correct and known I²C Interface state. This only resets the I²C state machine.

This is useful if the MCP40D17/18/19 device powers up in an incorrect state (due to excessive bus noise, etc), or if the Master Device is reset during communication. Figure 5-11 shows the communication sequence to software reset the device.

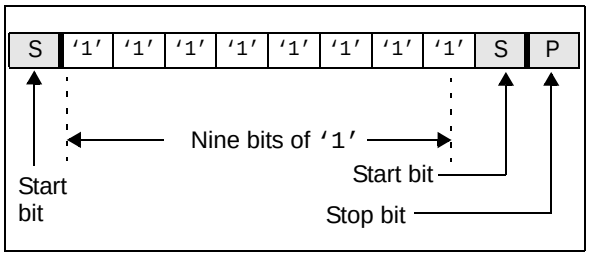

FIGURE 5-11: *Software Reset Sequence Format.*

The 1st Start bit will cause the device to reset from a state in which it is expecting to receive data from the Master Device. In this mode, the device is monitoring the data bus in Receive mode and can detect the Start bit forces an internal Reset.

The nine bits of '1' are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the MCP40D17/18/19 is driving an A on the I²C bus, or is in output mode (from a Read command) and is driving a data bit of '0' onto the I²C bus. In both of these cases, the previous Start bit could not be generated due to the MCP40D17/18/19 holding the bus low. By sending out nine '1' bits, it is ensured that the device will see a $\overline{A}$ (the Master Device does not drive the I²C bus low to acknowledge the data sent by the MCP40D17/18/19), which also forces the MCP40D17/18/19 to reset.

The 2nd Start bit is sent to address the rare possibility of an erroneous write. This could occur if the Master Device was reset while sending a Write command to the MCP40D17/18/19, AND then as the Master Device returns to normal operation and issues a Start condition while the MCP40D17/18/19 is issuing an A. In this case if the 2nd Start bit is not sent (and the Stop bit was sent) the MCP40D17/18/19 could initiate a write cycle.

Note:	The potential for this erroneous write ONLY occurs if the Master Device is reset while sending a Write command to the MCP40D17/18/19.

The Stop bit terminates the current I²C bus activity. The MCP40D17/18/19 wait to detect the next Start condition.

This sequence does not effect any other I²C devices which may be on the bus, as they should disregard this as an invalid command.

5.4 Serial Commands

The MCP40D17/18/19 devices support 2 serial commands. These commands are:

- **Write Operation**
- **Read Operations**

The I²C command formats have been defined so to support the SMBus version 2.0 Write Byte/Word Protocol formats and Read Byte/Word Protocol formats. The SMBus specification defines this operation is Section 5 of the Version 2.0 document (August 3, 2000).

This protocol format may be convienient for customers using library routines for the I²C bus, where all they need to do is specify the command (read, write, ...) with the Device Address, the Register Address, and the Data.

If higher data throughput is desired, please look at the MCP4017/18/19 devices which have a simplier I²C command format.

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5.4.1 WRITE OPERATION

The write operation requires the START condition, Control Byte, Acknowledge, Command Code, Acknowledge, Data Byte, Acknowledge and STOP (or RESTART) condition. The Control (Slave Address) Byte requires the R/$\overline{W}$ bit equal to a logic zero (R/$\overline{W}$ = "0") to generate a write sequence. The MCP40D17/18/19 is responsible for generating the Acknowledge (A) bits.

Data is written to the MCP40D17/18/19 after every byte transfer (during the A bit). If a STOP or RESTART condition is generated during a data transfer (before the A bit), the data will not be written to MCP40D17/18/19.

Data bytes may be written after each Acknowledge. The command is terminated once a Stop (P) condition occurs. Refer to Figure 5-12 for the single byte write sequence and Figure 5-13 for the generic (multi-byte) write sequence. For a single byte write, the master sends a STOP or RESTART condition after the 1st data byte is sent.

The MSb of each Data Byte is a don't care, since the wiper register is only 7-bits wide.

The command is terminated once a Stop (P) or Restart (S) condition occurs.

Figure 5-14 shows the I^2C write communication behavior of the Master Device and the MCP40D17/18/19 device and the resultant I^2C bus values.

Note:	A command code with a non-zero value will cause the data not to be written to the wiper register

5.4.2 READ OPERATIONS

The read operation requires the START condition, Control Byte, Acknowledge, Command Code, Acknowledge, Restart Condition, Control Byte, Acknowledge, Data Byte, the master generating the $\overline{A}$ and STOP (or RESTART) condition. The first Control Byte requires the R/$\overline{W}$ bit equal to a logic zero (R/$\overline{W}$ = "0") to write the Command Code, while the second Control Byte requires the R/$\overline{W}$ bit equal to a logic one (R/$\overline{W}$ = "1") to generate a read sequence. The MCP40D17/18/19 will A the Slave Address Byte and $\overline{A}$ all the Data Bytes. The I^2C Master will $\overline{A}$ the Slave Address Byte and the last Data Byte. If there are multiple Data Bytes, the I^2C Master will A all Data Bytes except the last Data Byte (which it will $\overline{A}$).

The MCP40D17/18/19 maintains control of the SDA signal until all data bits have been clocked out.

The command is terminated once a Stop (P) or Restart (S) condition occurs. Refer to Figure 5-15 for the read command sequence. For a single read, the master sends a STOP or RESTART condition after the 1st data byte (and A bit) is sent from the slave.

Figure 5-16 shows the I^2C read communication behavior of the Master Device and the MCP40D17/18/19 device and the resultant I^2C bus values.

Note:	A command code with a non-zero value will cause the data not to be read from the wiper register

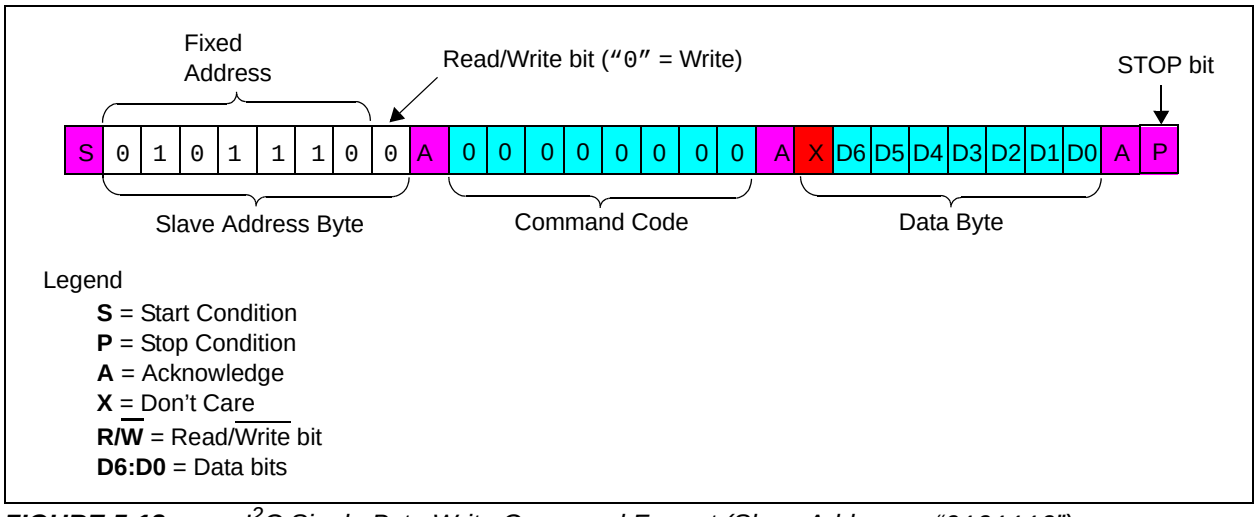

FIGURE 5-12: *I^2C Single Byte Write Command Format (Slave Address = "0101110").*

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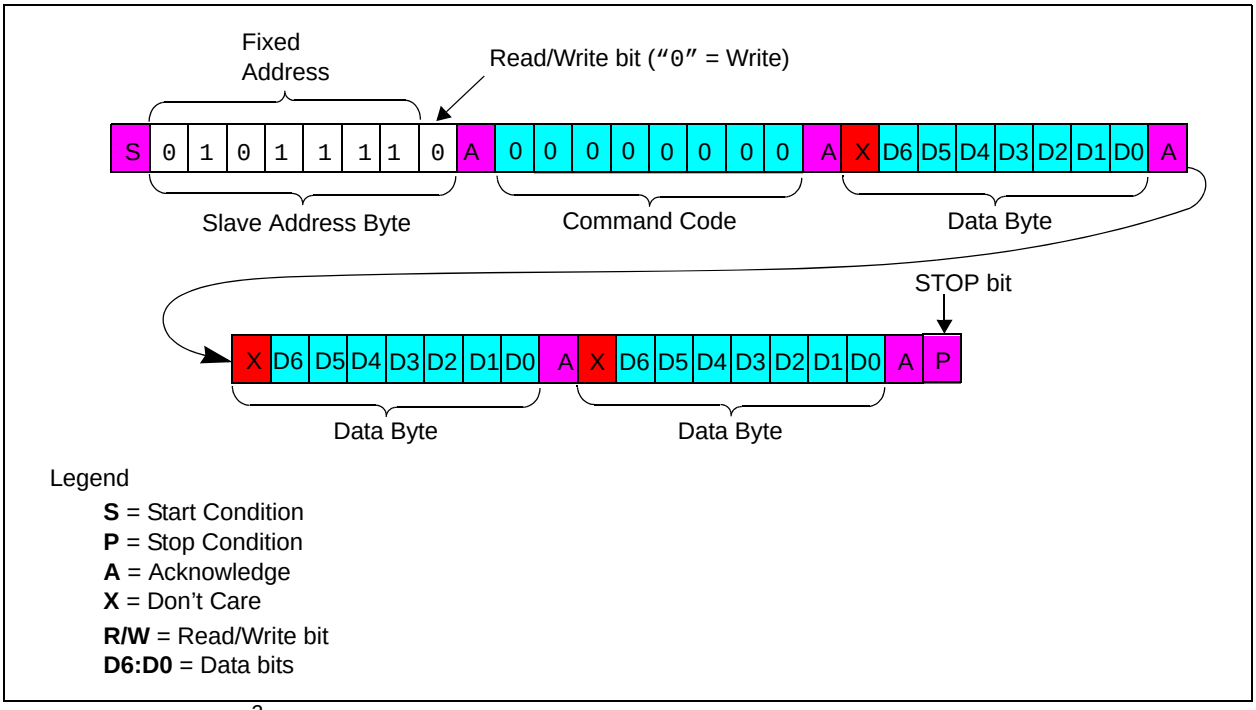

FIGURE 5-13: *I²C Write Command Format (Slave Address = "0101110").*

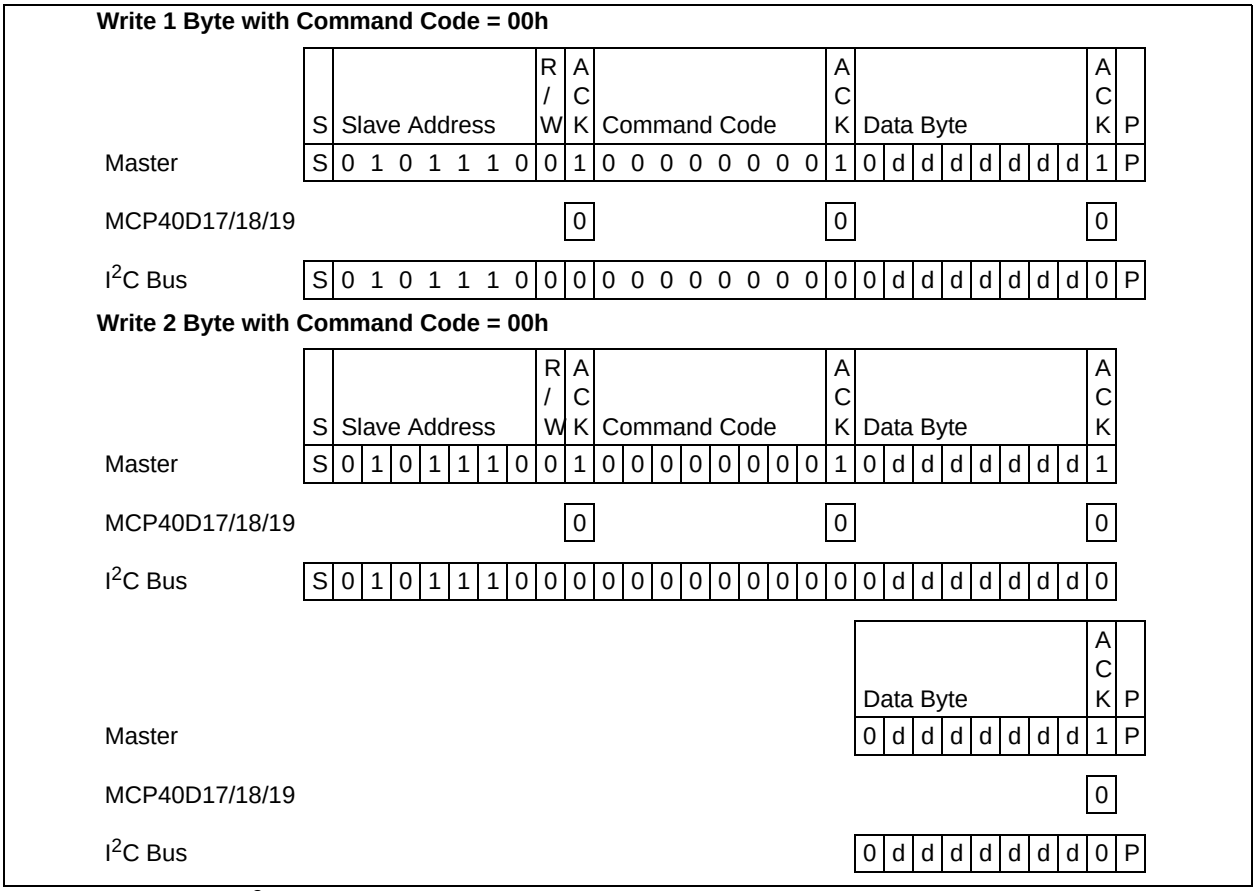

FIGURE 5-14: *I²C Write Communication Behavior (Slave Address = "0101110").*

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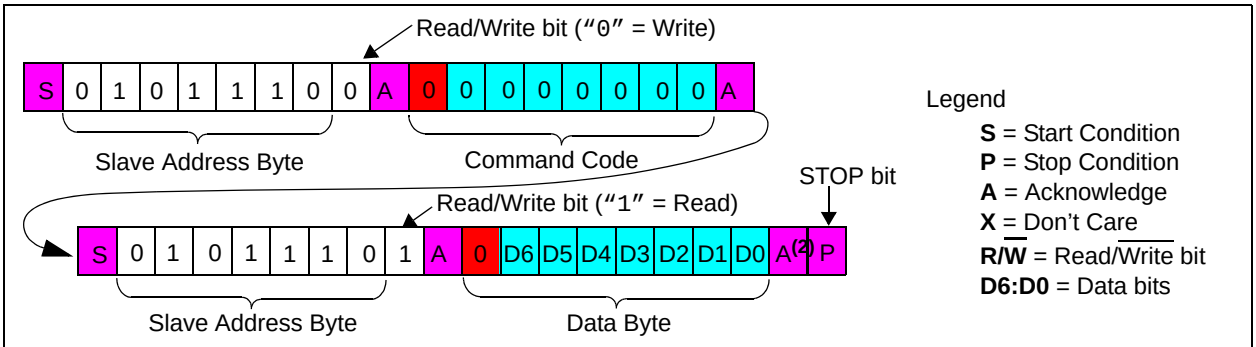

Note 1: Master Device is responsible for $\overline{\text{ACK}}$ / $\overline{\text{NACK}}$ signal. If a $\overline{\text{NACK}}$ signal occurs, the MCP40D17/18/19 will abort this transfer and release the bus.

2: The Master Device will Not $\overline{\text{ACK}}$, and the MCP40D17/18/19 will release the bus so the Master Device can generate a Stop or Repeated Start condition.

FIGURE 5-15: *I^2C Read Command Format (Slave Address = "0101110").*

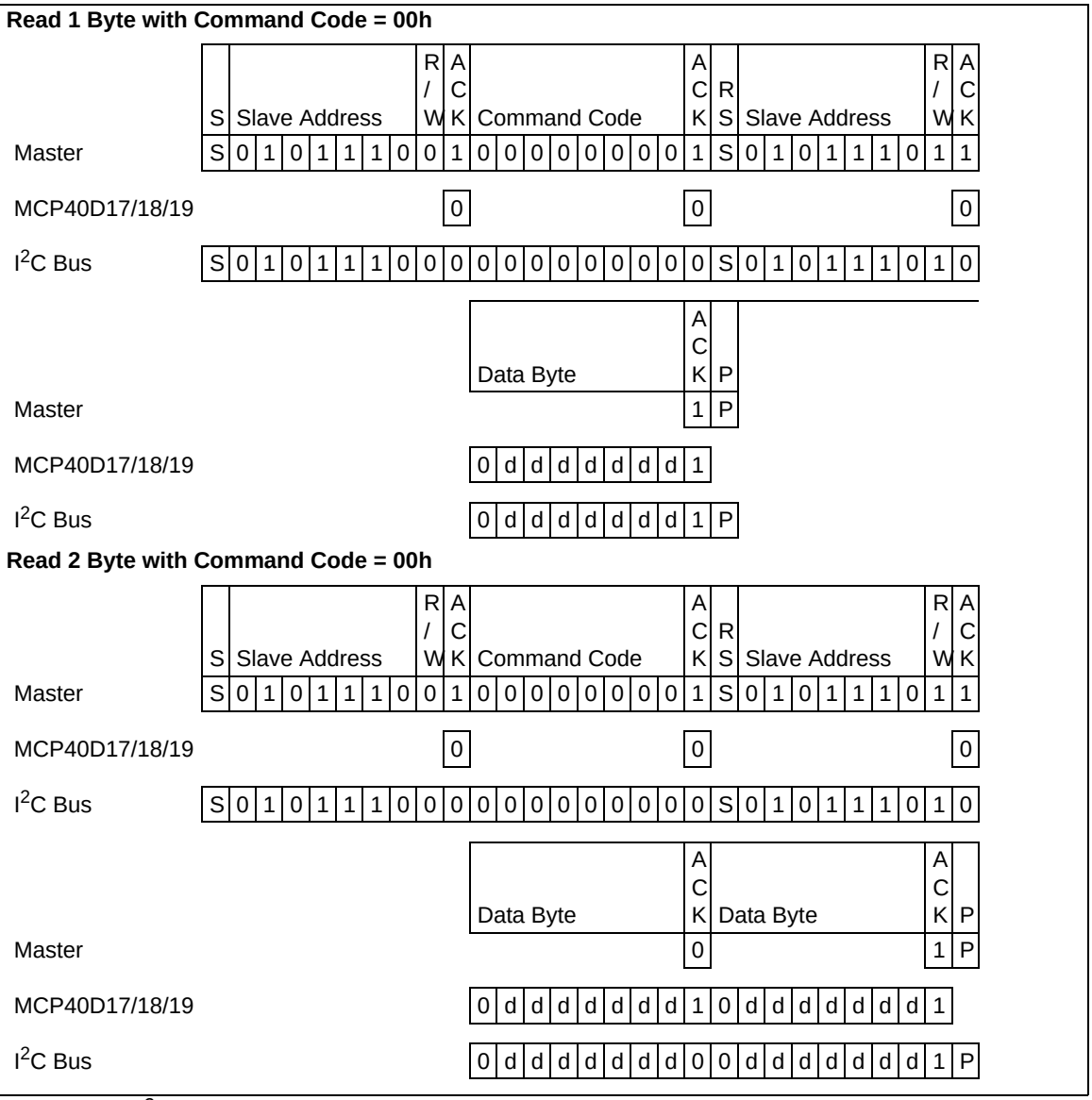

FIGURE 5-16: *I^2C Read Communication Behavior (Slave Address = "0101110").*

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6.0 RESISTOR NETWORK

The Resistor Network is made up of two parts. These are:

- Resistor Ladder
- Wiper

Figure 6-1 shows a block diagram for the resistive network.

Digital potentiometer applications can be divided into two resistor network categories:

- Rheostat configuration
- Potentiometer (or voltage divider) configuration

The MCP40D17 is a true rheostat, with terminal B and the wiper (W) of the variable resistor available on pins.

The MCP40D18 device offers a voltage divider (potentiometer) with terminal B internally connected to ground.

The MCP40D19 device is a Rheostat device with terminal A of the resistor floating, terminal B internally connected to ground, and the wiper (W) available on pin.

6.1 Resistor Ladder Module

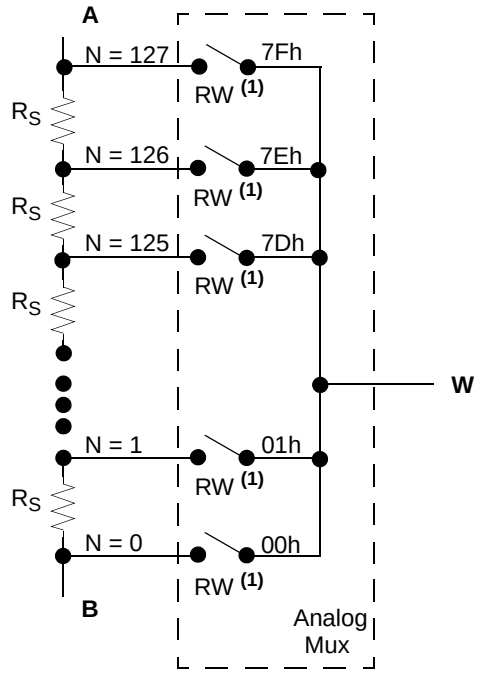
The resistor ladder is a series of equal value resistors (R_S) with a connection point (tap) between the two resistors. The total number of resistors in the series (ladder) determines the R_{AB} resistance (see Figure 6-1). The end points of the resistor ladder are connected to the device Terminal A and Terminal B pins. The R_{AB} (and R_S) resistance has small variations over voltage and temperature.

The Resistor Network has 127 resistors in a string between terminal A and terminal B. This gives 7-bits of resolution.

The wiper can be set to tap onto any of these 127 resistors thus providing 128 possible settings (including terminal A and terminal B). This allows zero scale to full scale connections.

A wiper setting of 00h connects the Terminal W (wiper) to Terminal B (Zero Scale). A wiper setting of 3Fh is the Mid scale setting. A wiper setting of 7Fh connects the Terminal W (wiper) to Terminal A (Full Scale). Table 6-1 illustrates the full wiper setting map.

Terminal A and B as well as the wiper W do not have a polarity. These terminals can support both positive and negative current.



Note 1: The wiper resistance is tap dependent. That is, each tap selection resistance has a small variation. This variation has more effect on devices with smaller R_{AB} resistance (5.0 kΩ).

FIGURE 6-1: *Resistor Network Block Diagram.*

TABLE 6-1: WIPER SETTING MAP

Wiper Setting	Properties
07Fh	Full Scale (W = A)
07Eh - 040h	W = N
03Fh	W = N (Mid Scale)
03Eh - 001h	W = N
000h	Zero Scale (W = B)

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Step resistance (R_S) is the resistance from one tap setting to the next. This value will be dependent on the R_{AB} value that has been selected. Equation 6-1 shows the calculation for the step resistance while Table 6-2 shows the typical step resistances for each device.

EQUATION 6-1: R_S CALCULATION

$$R_S = \frac{R_{AB}}{127}$$

Equation 6-2 illustrates the calculation used to determine the resistance between the wiper and terminal B.

EQUATION 6-2: R_{WB} CALCULATION

$$R_{WB} = \frac{R_{AB}N}{127} + R_W$$

N = 0 to 127 (decimal)

The digital potentiometer is available in four nominal resistances (R_{AB}) where the nominal resistance is defined as the resistance between terminal A and terminal B. The four nominal resistances are 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ.

The total resistance of the device has minimal variation due to operating voltage (see Figure 2-11, Figure 2-29, Figure 2-47, or Figure 2-65).

TABLE 6-2: STEP RESISTANCES

Part Number	Resistance (Ω)		
	Case	Total (R_{AB})	Step (R_S)
MCP40D17/18/19-502	Minimum	4000	31.496
	Typical	5000	39.370
	Maximum	6000	47.244
MCP40D17/18/19-103	Minimum	8000	62.992
	Typical	10000	78.740
	Maximum	12000	94.488
MCP40D17/18/19-503	Minimum	40000	314.961
	Typical	50000	393.701
	Maximum	60000	472.441
MCP40D17/18/19-104	Minimum	80000	629.921
	Typical	100000	787.402
	Maximum	120000	944.882

A POR/BOR event will load the Volatile Wiper register value with the default value. Table 6-3 shows the default values offered.

TABLE 6-3: DEFAULT FACTORY SETTINGS SELECTION

Resistance Code	Typical R_{AB} Value	Default POR Wiper	
		Setting	Code (1)
-502	5.0 kΩ	Mid-scale	3Fh
-103	10.0 kΩ	Mid-scale	3Fh
-503	50.0 kΩ	Mid-scale	3Fh
-104	100.0 kΩ	Mid-scale	3Fh

Note 1: Custom POR/BOR Wiper Setting options are available, contact the local Microchip Sales Office for additional information. Custom options have minimum volume requirements.

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6.2 Resistor Configurations

6.2.1 RHEOSTAT CONFIGURATION

When used as a rheostat, two of the three digital potentiometer's terminals are used as a resistive element in the circuit. With terminal W (wiper) and either terminal A or terminal B, a variable resistor is created. The resistance will depend on the tap setting of the wiper (and the wiper's resistance). The resistance is controlled by changing the wiper setting

The unused terminal (B or A) should be left floating. Figure 6-2 shows the two possible resistors that can be used. Reversing the polarity of the A and B terminals will not affect operation.

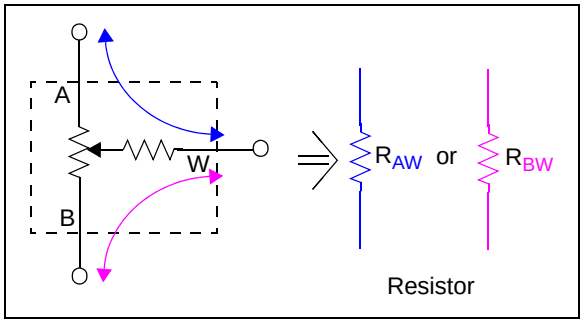

FIGURE 6-2: *Rheostat Configuration.*

This allows the control of the total resistance between the two nodes. The total resistance depends on the "starting" terminal to the Wiper terminal. So at the code 00h, the R_{BW} resistance is minimal (R_W), but the R_{AW} resistance in maximized ($R_{AB} + R_W$). Conversely, at the code 3Fh, the R_{AW} resistance is minimal (R_W), but the R_{BW} resistance in maximized ($R_{AB} + R_W$).

The resistance Step size (R_S) equates to one LSb of the resistor.

Note:	To avoid damage to the internal wiper circuitry in this configuration, care should be taken to insure the current flow never exceeds 2.5 mA.

The pinout for the rheostat devices is such that as the wiper register is incremented, the resistance of the resistor will increase (as measured from Terminal B to the W Terminal).

6.2.2 POTENTIOMETER CONFIGURATION

When used as a potentiometer, all three terminals of the device are tied to different nodes in the circuit. This allows the potentiometer to output a voltage proportional to the input voltage. This configuration is sometimes called voltage divider mode. The potentiometer is used to provide a variable voltage by adjusting the wiper position between the two endpoints as shown in Figure 6-3. Reversing the polarity of the A and B terminals will not affect operation.

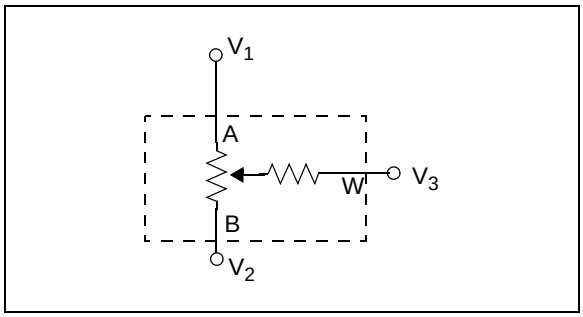

FIGURE 6-3: *Potentiometer Configuration.*

The temperature coefficient of the R_{AB} resistors is minimal by design. In this configuration, the resistors all change uniformly, so minimal variation should be seen.

The Wiper resistor temperature coefficient is different to the R_{AB} temperature coefficient. The voltage at node V_3 (Figure 6-3) is not dependent on this Wiper resistance, just the ratio of the R_{AB} resistors, so this temperature coefficient in most cases can be ignored.

Note:	To avoid damage to the internal wiper circuitry in this configuration, care should be taken to insure the current flow never exceeds 2.5 mA.

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6.3 Wiper Resistance

Wiper resistance is the series resistance of the analog switch that connects the selected resistor ladder node to the Wiper Terminal common signal (see Figure 6-1).

A value in the volatile wiper register selects which analog switch to close, connecting the W terminal to the selected node of the resistor ladder.

The resistance is dependent on the voltages on the analog switch source, gate, and drain nodes, as well as the device's wiper code, temperature, and the current through the switch. As the device voltage decreases, the wiper resistance increases (see Figure 6-4 and Table 6-4).

The wiper can connect directly to Terminal B or to Terminal A. A zero scale connections, connects the Terminal W (wiper) to Terminal B (wiper setting of 000h). A full scale connections, connects the Terminal W (wiper) to Terminal A (wiper setting of 7Fh). In these configurations the only resistance between the Terminal W and the other Terminal (A or B) is thaΩt of the analog switches.

The wiper resistance is typically measured when the wiper is positioned at either zero scale (00h) or full scale (3Fh).

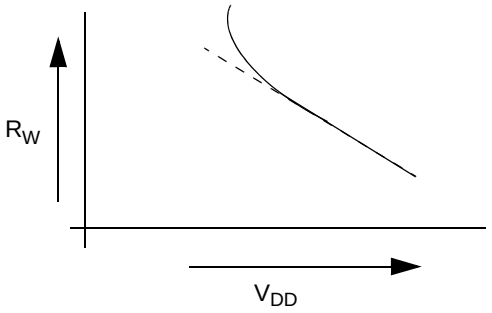
The wiper resistance in potentiometer-generated voltage divider applications is not a significant source of error.

The wiper resistance in rheostat applications can create significant nonlinearity as the wiper is moved toward zero scale (00h). The lower the nominal resistance, the greater the possible error.

In a rheostat configuration, this change in voltage needs to be taken into account. Particularly for the lower resistance devices. For the 5.0 kΩ device the maximum wiper resistance at 5.5V is approximately 3.2% of the total resistance, while at 2.7V it is approximately 6.5% of the total resistance.

In a potentiometer configuration, the wiper resistance variation does not effect the output voltage seen on the W pin.

The slope of the resistance has a linear area (at the higher voltages) and a non-linear area (at the lower voltages). In where resistance increases faster than the voltage drop (at low voltages).



Note: The slope of the resistance has a linear area (at the higher voltages) and a non-linear area (at the lower voltages).

FIGURE 6-4: *Relationship of Wiper Resistance (R_W) to Voltage.*

Since there is minimal variation of the total device resistance over voltage, at a constant temperature (see Figure 2-11, Figure 2-29, Figure 2-47, or Figure 2-65), the change in wiper resistance over voltage can have a significant impact on the INL and DNL error.

TABLE 6-4: TYPICAL STEP RESISTANCES AND RELATIONSHIP TO WIPER RESISTANCE

Resistance (?)					R_W / R_S (%) (1)			R_W / R_{AB} (%) (2)		
Typical		Wiper (R_W)								
Total (R_{AB})	Step (R_S)	Typical	Max @ 5.5V	Max @ 2.7V	R_W = Typical	R_W = Max @ 5.5V	R_W = Max @ 2.7V	R_W = Typical	R_W = Max @ 5.5V	R_W = Max @ 2.7V
5000	39.37	100	170	325	254.00%	431.80%	825.5%	2.00%	3.40%	6.50%
10000	78.74	100	170	325	127.00%	215.90%	412.75%	1.00%	1.70%	3.25%
50000	393.70	100	170	325	25.40%	43.18%	82.55%	0.20%	0.34%	0.65%
100000	787.40	100	170	325	12.70%	21.59%	41.28%	0.10%	0.17%	0.325%

Note 1: R_S is the typical value. The variation of this resistance is minimal over voltage.

2: R_{AB} is the typical value. The variation of this resistance is minimal over voltage.

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6.4 Operational Characteristics

Understanding the operational characteristics of the device's resistor components is important to the system design.

6.4.1 ACCURACY

6.4.1.1 Integral Non-linearity (INL)

INL error for these devices is the maximum deviation between an actual code transition point and its corresponding ideal transition point after offset and gain errors have been removed. These endpoints are from 0x00 to 0x7F. Refer to Figure 6-5.

Positive INL means higher resistance than ideal. Negative INL means lower resistance than ideal.

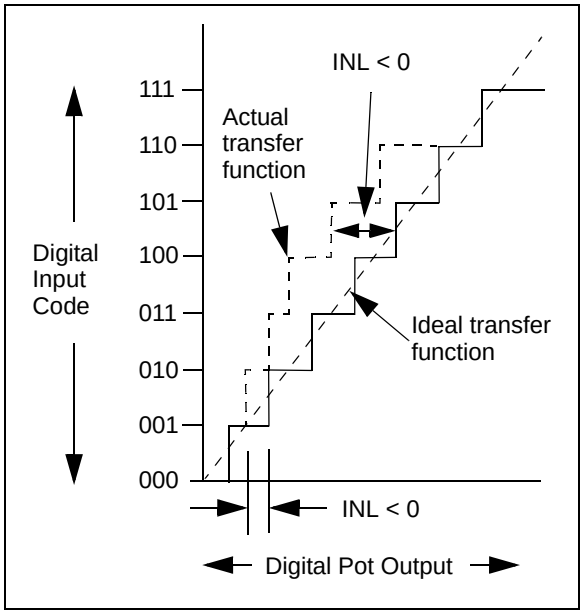

FIGURE 6-5: *INL Accuracy.*

6.4.1.2 Differential Non-linearity (DNL)

DNL error is the measure of variations in code widths from the ideal code width. A DNL error of zero would imply that every code is exactly 1 LSb wide.

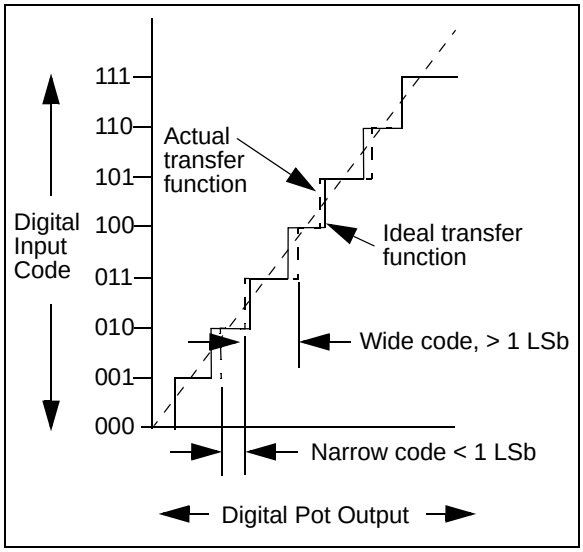

FIGURE 6-6: *DNL Accuracy.*

6.4.1.3 Ratiometric temperature coefficient

The ratiometric temperature coefficient quantifies the error in the ratio R_{AW}/R_{WB} due to temperature drift. This is typically the critical error when using a potentiometer device (MCP40D18) in a voltage divider configuration.

6.4.1.4 Absolute temperature coefficient

The absolute temperature coefficient quantifies the error in the end-to-end resistance (Nominal resistance R_{AB}) due to temperature drift. This is typically the critical error when using a rheostat device (MCP40D17 and MCP40D19) in an adjustable resistor configuration.

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6.4.2 MONOTONIC OPERATION

Monotonic operation means that the device's resistance increases with every step change (from terminal A to terminal B or terminal B to terminal A).

The wiper resistances difference at each tap location. When changing from one tap position to the next (either increasing or decreasing), the ΔR_W is less than the ΔR_S. When this change occurs, the device voltage and temperature are "the same" for the two tap positions.

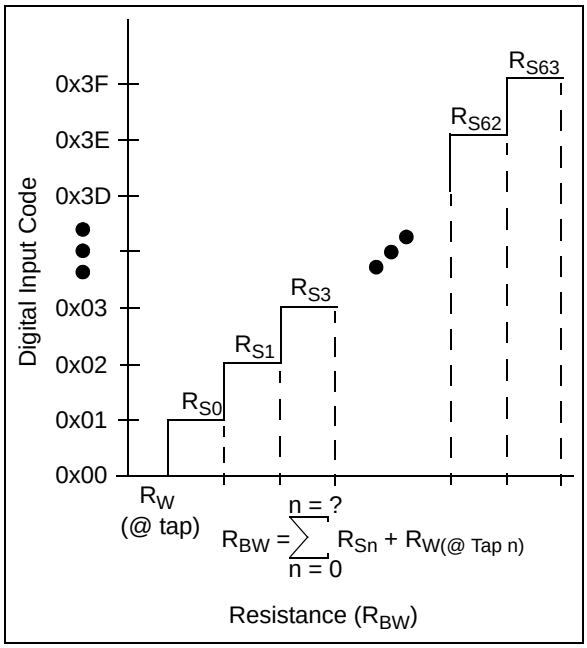

FIGURE 6-7: *R_{BW}.*

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7.0 DESIGN CONSIDERATIONS

In the design of a system with the MCP40D17/18/19 devices, the following considerations should be taken into account. These are:

- The Power Supply
- The Layout

In the design of a system with the MCP40D17/18/19 devices, the following considerations should be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

7.1 Power Supply Considerations

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 7-1 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close to the device power pin (V_{DD}) as possible (within 4 mm).

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} should reside on the analog plane.

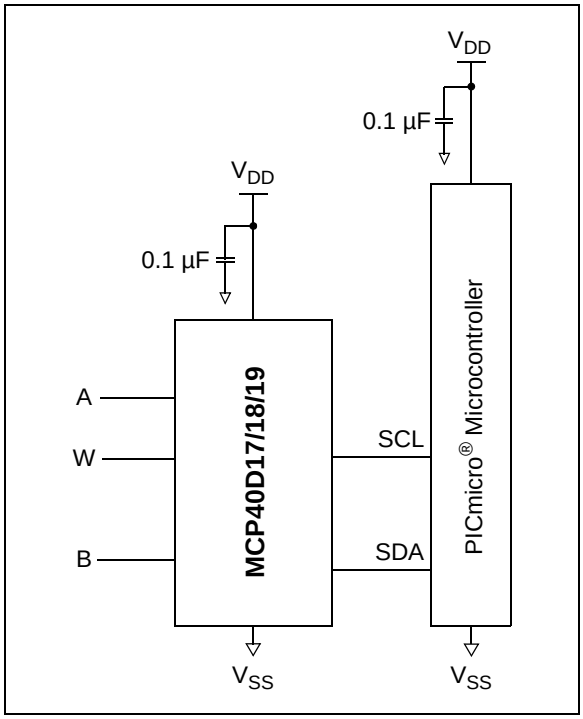

FIGURE 7-1: *Typical Microcontroller Connections.*

7.2 Layout Considerations

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP40D17/18/19's performance. Careful board layout will minimize these effects and increase the Signal-to-Noise Ratio (SNR). Bench testing has shown that a multi-layer board utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

If low noise is desired, breadboards and wire-wrapped boards are not recommended.

7.2.1 RESISTOR TEMPCO

Characterization curves of the resistor temperature coefficient (Tempco) are shown in Figure 2-11, Figure 2-29, Figure 2-47, and Figure 2-65.

These curves show that the resistor network is designed to correct for the change in resistance as temperature increases. This technique reduces the end to end change is R_{AB} resistance.

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NOTES:

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8.0 APPLICATIONS EXAMPLES

Digital potentiometers have a multitude of practical uses in modern electronic circuits. The most popular uses include precision calibration of set point thresholds, sensor trimming, LCD bias trimming, audio attenuation, adjustable power supplies, motor control overcurrent trip setting, adjustable gain amplifiers and offset trimming. The MCP40D17/18/19 devices can be used to replace the common mechanical trim pot in applications where the operating and terminal voltages are within CMOS process limitations (V_{DD} = 2.7V to 5.5V).

8.1 Set Point Threshold Trimming

Applications that need accurate detection of an input threshold event often need several sources of error eliminated. Use of comparators and operational amplifiers (op amps) with low offset and gain error can help achieve the desired accuracy, but in many applications, the input source variation is beyond the designer's control. If the entire system can be calibrated after assembly in a controlled environment (like factory test), these sources of error are minimized if not entirely eliminated.

Figure 8-1 illustrates a common digital potentiometer configuration. This configuration is often referred to as a "windowed voltage divider". Note that R_1 is not necessary to create the voltage divider, but its presence is useful when the desired threshold has limited range. It is "windowed" because R_1 can narrow the adjustable range of V_{TRIP} to a value much less than $V_{DD} - V_{SS}$. If the output range is reduced, the magnitude of each output step is reduced. This effectively increases the trimming resolution for a fixed digital potentiometer resolution. This technique may allow a lower-cost digital potentiometer to be utilized (64 steps instead of 256 steps).

The MCP40D18's low DNL performance is critical to meeting calibration accuracy in production without having to use a higher precision digital potentiometer.

EQUATION 8-1: CALCULATING THE WIPER SETTING FROM THE DESIRED V_{TRIP}

$$V_{TRIP} = V_{DD}\left(\frac{R_{WB}}{R_1 + R_2}\right)$$

$$R_{AB} = R_{Nominal}$$

$$R_{WB} = R_{AB} \bullet \left(\frac{D}{127}\right)$$

$$D = \left(\left(\frac{V_{TRIP}}{V_{DD}}\right) \bullet (R_1 + R_{AB})\right) \bullet 127$$

D = Digital Potentiometer Wiper Setting (0-127)

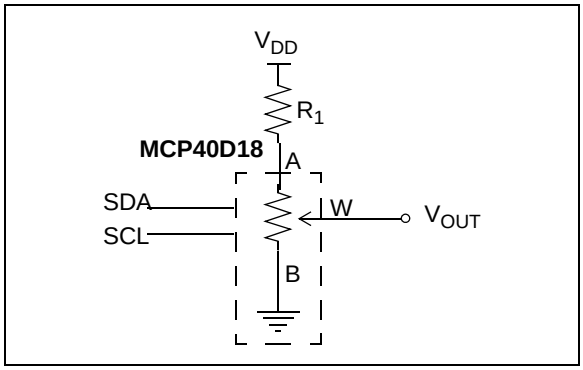

FIGURE 8-1: *Using the Digital Potentiometer to Set a Precise Output Voltage.*

8.1.1 TRIMMING A THRESHOLD FOR AN OPTICAL SENSOR

If the application has to calibrate the threshold of a diode, transistor or resistor, a variation range of 0.1V is common. Often, the desired resolution of 2 mV or better is adequate to accurately detect the presence of a precise signal. A "windowed" voltage divider, utilizing the MCP40D18, would be a potential solution. Figure 8-2 illustrates this example application.

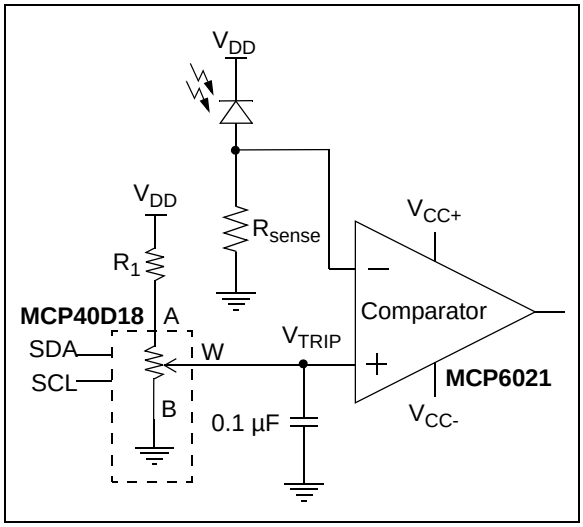

FIGURE 8-2: *Set Point or Threshold Calibration.*

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8.2 Operational Amplifier Applications

Figure 8-3 and Figure 8-4 illustrate typical amplifier circuits that could replace fixed resistors with the MCP40D17/18/19 to achieve digitally-adjustable analog solutions.

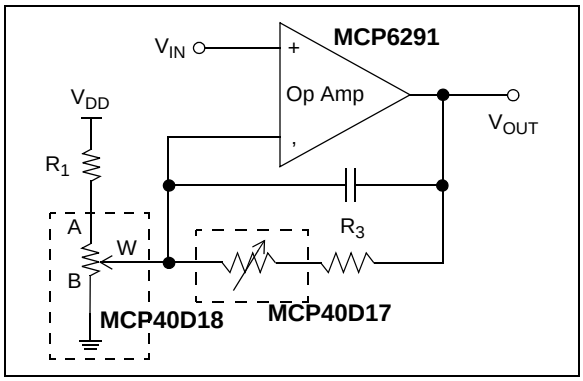

FIGURE 8-3: *Trimming Offset and Gain in a Non-Inverting Amplifier.*

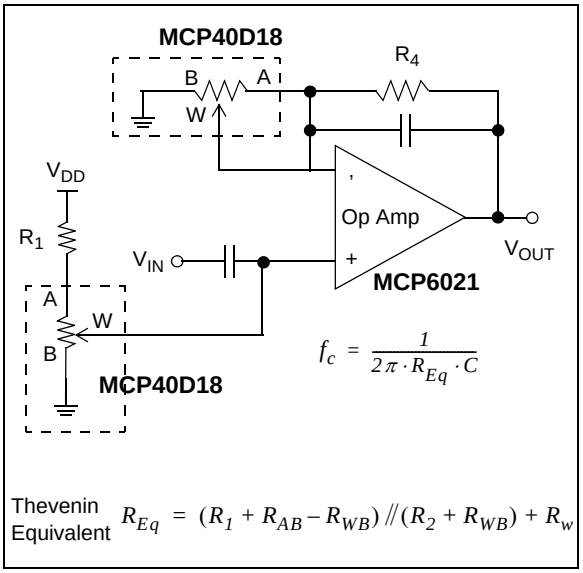

FIGURE 8-4: *Programmable Filter.*

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8.3 Temperature Sensor Applications

Thermistors are resistors with very predictable variation with temperature. Thermistors are a popular sensor choice when a low-cost temperature-sensing solution is desired. Unfortunately, thermistors have non-linear characteristics that are undesirable, typically requiring trimming in an application to achieve greater accuracy. There are several common solutions to trim and linearize thermistors. Figure 8-5 and Figure 8-6 are simple methods for linearizing a 3-terminal NTC thermistor. Both are simple voltage dividers using a Positive Temperature Coefficient (PTC) resistor (R_1) with a transfer function capable of compensating for the linearity error in the Negative Temperature Coefficient (NTC) thermistor.

The circuit, illustrated by Figure 8-5, utilizes a digital rheostat for trimming the offset error caused by the thermistor's part-to-part variation. This solution puts the digital potentiometer's R_W into the voltage divider calculation. The MCP40D17/18/19's R_{AB} temperature coefficient is a low 50 ppm (-20°C to +70°C). R_W's error is substantially greater than R_{AB}'s error because R_W varies with V_{DD}, wiper setting and temperature. For the 50 kΩ devices, the error introduced by R_W is, in most cases, insignificant as long as the wiper setting is > 6. For the 2 kΩ devices, the error introduced by R_W is significant because it is a higher percentage of R_{WB}. For these reasons, the circuit illustrated in Figure 8-5 is not the most optimum method for "exciting" and linearizing a thermistor.

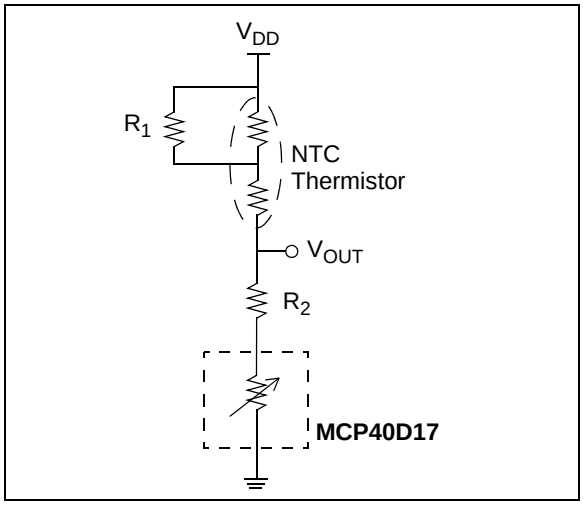

FIGURE 8-5: *Thermistor Calibration using a Digital Potentiometer in a Rheostat Configuration.*

The circuit illustrated by Figure 8-6 utilizes a digital potentiometer for trimming the offset error. This solution removes R_W from the trimming equation along with the error associated with R_W. R_2 is not required, but can be utilized to reduce the trimming "window" and reduce variation due to the digital pot's R_{AB} part-to-part variability.

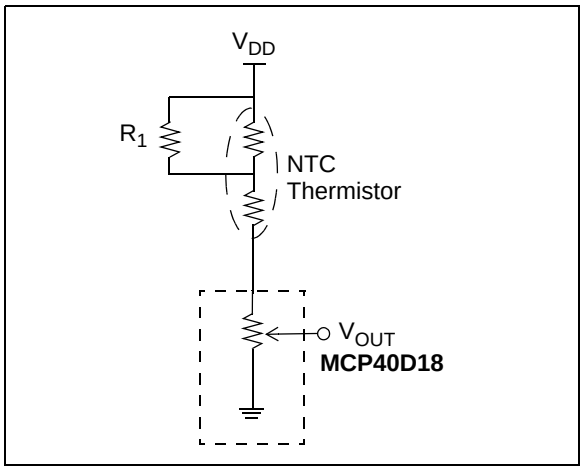

FIGURE 8-6: *Thermistor Calibration using a Digital Potentiometer in a Potentiometer Configuration.*

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8.4 Wheatstone Bridge Trimming

Another common configuration to “excite” a sensor (such as a strain gauge, pressure sensor or thermistor) is the wheatstone bridge configuration. The wheatstone bridge provides a differential output instead of a single-ended output. Figure 8-7 illustrates a wheatstone bridge utilizing one to three digital potentiometers. The digital potentiometers in this example are used to trim the offset and gain of the wheatstone bridge.

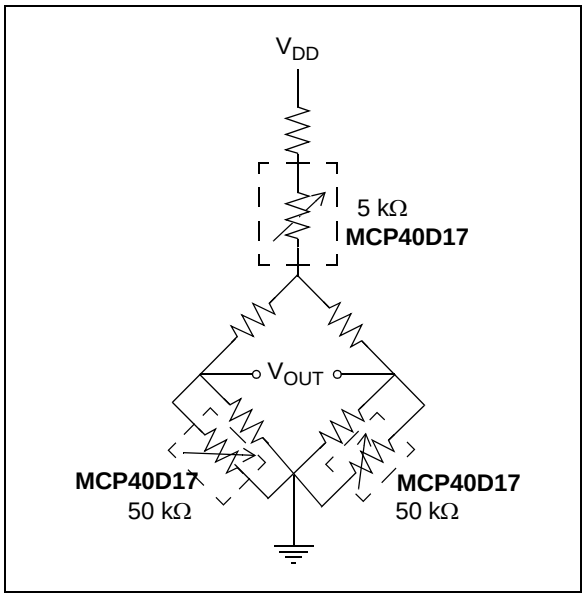

FIGURE 8-7: *Wheatstone Bridge Trimming.*

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9.0 DEVELOPMENT SUPPORT

9.1 Development Tools

The MCP40D17/18/19 devices can be evaluated with the MCP4XXXDM-PGA board, but it will require the removal of the MCP4017 device and the installation of the MCP40D17 device. Please check the Microchip web site for the release of this board. The board part number is tentatively MCP4XXXDM-PGA, and is expected to be available in the fall of 2009.

Note:	The MCP40D17 device is identical to the MCP4017 device with the exception of the I^2C interface protocol format.

9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-1 shows some of these documents.

TABLE 9-1: TECHNICAL DOCUMENTATION

Application Note Number	Title	Literature #
AN1080	Understanding Digital Potentiometers Resistor Variations	DS01080
AN737	Using Digital Potentiometers to Design Low-Pass Adjustable Filters	DS00737
AN692	Using a Digital Potentiometer to Optimize a Precision Single Supply Photo Detect	DS00692
AN691	Optimizing the Digital Potentiometer in Precision Circuits	DS00691
AN219	Comparing Digital Potentiometers to Mechanical Potentiometers	DS00219
—	Digital Potentiometer Design Guide	DS22017
—	Signal Chain Design Guide	DS21825

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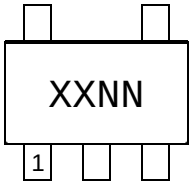
10.0 PACKAGING INFORMATION

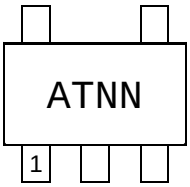
10.1 Package Marking Information

5-Lead SC70

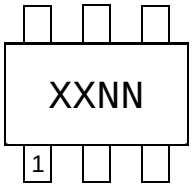


Part Number	Code
MCP40D19T-502E/LT	BTNN
MCP40D19T-103E/LT	BUNN
MCP40D19T-503E/LT	BVNN
MCP40D19T-104E/LT	BWNN

Example:

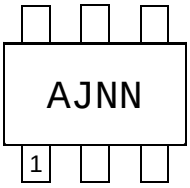


6-Lead SC70



Part Number	Code	Part Number	Code
MCP40D17T-502E/LT	AJNN	MCP40D18T-502E/LT	APNN
MCP40D17T-103E/LT	AKNN	MCP40D18T-502AE/LT	ATNN
MCP40D17T-503E/LT	ALNN	MCP40D18T-103E/LT	AQNN
MCP40D17T-104E/LT	AMNN	MCP40D18T-103AE/LT	AUNN
		MCP40D18T-503E/LT	ARNN
		MCP40D18T-503AE/LT	AVNN
		MCP40D18T-104E/LT	ASNN
		MCP40D18T-104AE/LT	AWNN

Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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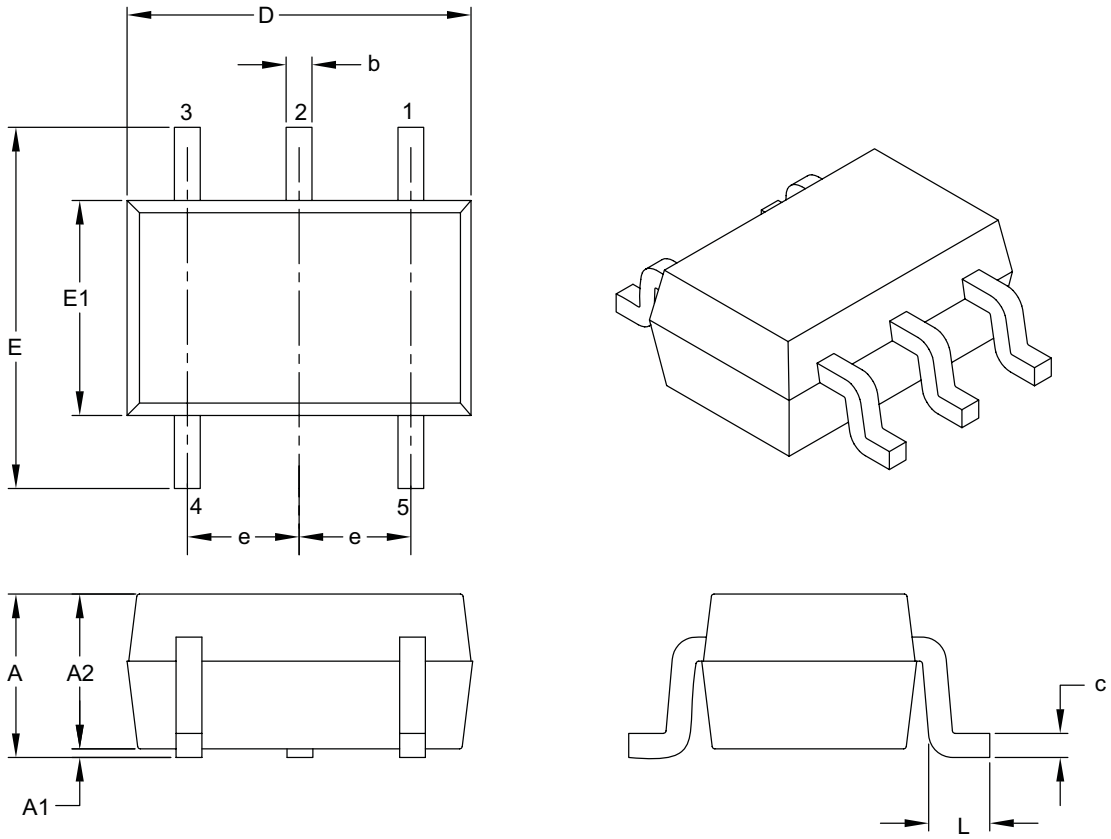
5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

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5-Lead Plastic Small Outline Transistor (LT) [SC70]

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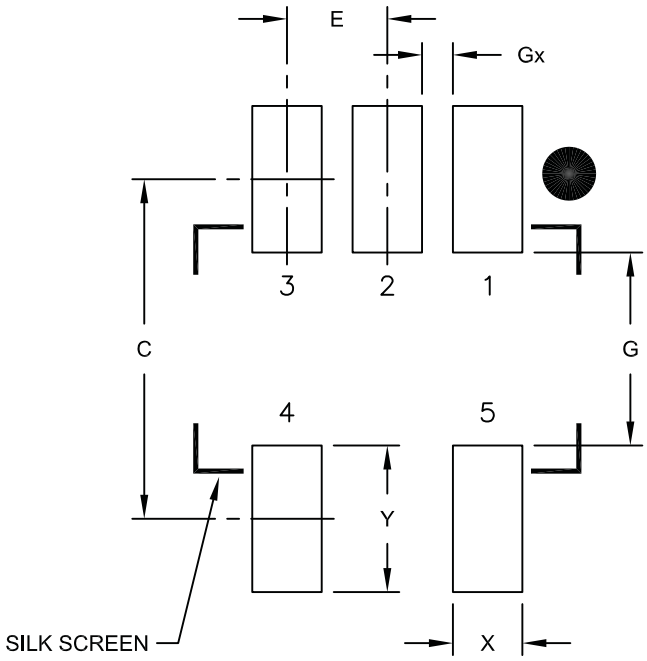

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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6-Lead Plastic Small Outline Transistor (LT) [SC70]

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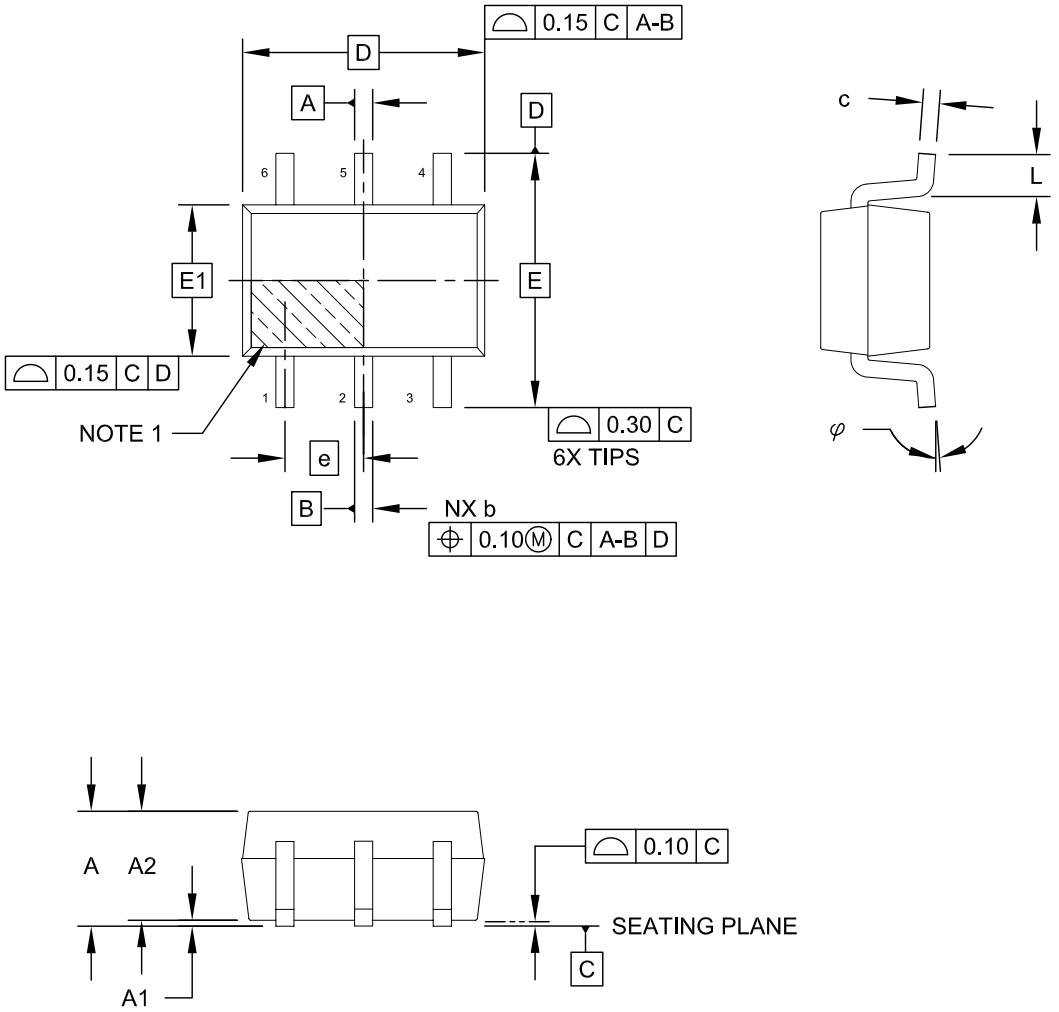

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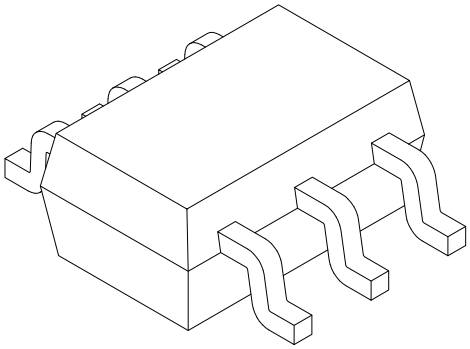
6-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Molded Package Thickness	A2	0.70	0.90	1.00
Standoff	A1	0.00	-	0.10
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Overall Length	D		2.00 BSC	
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.22
Lead Width	b	0.15	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-151A Sheet 2 of 2

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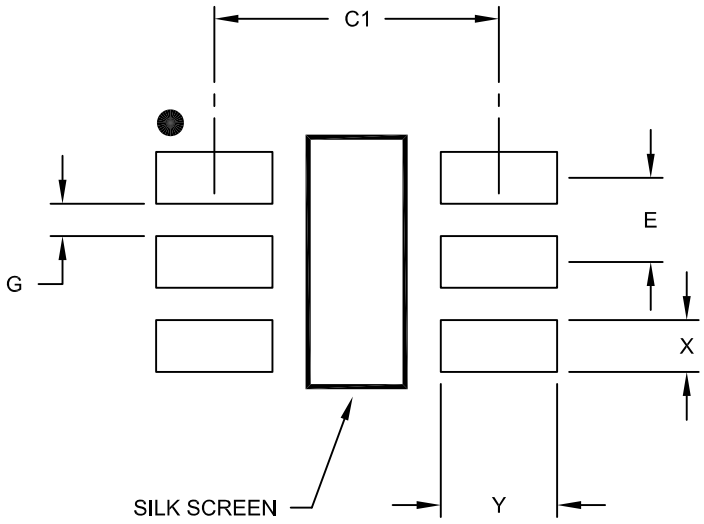
6-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width (X28)	X			0.40
Contact Pad Length (X28)	Y			0.90
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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APPENDIX A: REVISION HISTORY

Revision B (August 2009)

the following is the List of Modifications:

1. Document updated to include the new standard I^2C slave address ("0111110") for the MCP40D18 device.
2. **Section 10.0 "Packaging Information"**: Corrected the Marking codes for 5-lead SC70 Codes shown were for the 6-lead SC70. Updated Package Outline Drawings.

Revision A (May 2009)

- Original Release of this Document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XXX	X	X	/XX
Device	Resistance Version	I^2C Device Address	Temperature Range	Package

Device:	MCP40D17: Single Rheostat with I^2C interface MCP40D17T: Single Rheostat with I^2C interface (Tape and Reel) MCP40D18: Single Potentiometer to GND with I^2C Interface MCP40D18T: Single Potentiometer to GND with I^2C Interface (Tape and Reel) MCP40D19: Single Rheostat to GND with I^2C Interface MCP40D19T: Single Rheostat to GND with I^2C Interface (Tape and Reel)
Resistance Version:	502 = 5 kΩ 103 = 10 kΩ 503 = 50 kΩ 104 = 100 kΩ
I^2C Device Address Version:	blank = '0101110' A = '0111110' (1)
Temperature Range:	E = -40°C to +125°C
Package:	LT = Plastic Small Outline Transistor (SC70), 5-lead, 6-lead

Note 1: This address is a standard option on the MCP40D18 device only. It is a custom device on the MCP40D17 and MCP40D19 devices.

Examples:

a) MCP40D17T-502E/LT: 5 kΩ, 6-LD SC70
b) MCP40D17T-103E/LT: 10 kΩ, 6-LD SC70
c) MCP40D17T-503E/LT: 50 kΩ, 6-LD SC70
d) MCP40D17T-104E/LT: 100 kΩ, 6-LD SC70

a) MCP40D18T-502E/LT: 5 kΩ, 6-LD SC70
b) MCP40D18T-103E/LT: 10 kΩ, 6-LD SC70
c) MCP40D18T-503E/LT: 50 kΩ, 6-LD SC70
d) MCP40D18T-104E/LT: 100 kΩ, 6-LD SC70

a) MCP40D18T-502AE/LT: 5 kΩ, 6-LD SC70
b) MCP40D18T-103AE/LT: 10 kΩ, 6-LD SC70
c) MCP40D18T-503AE/LT: 50 kΩ, 6-LD SC70
d) MCP40D18T-104AE/LT: 100 kΩ, 6-LD SC70

a) MCP40D19T-502E/LT: 5 kΩ, 5-LD SC70
b) MCP40D19T-103E/LT: 10 kΩ, 5-LD SC70
c) MCP40D19T-503E/LT: 50 kΩ, 5-LD SC70
d) MCP40D19T-104E/LT: 100 kΩ, 5-LD SC70

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