

Figure 1. Pinout: 14-Lead (Top View)

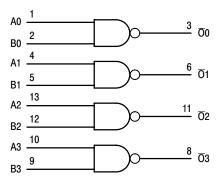


Figure 2. Logic Diagram

PIN NAMES

Pins	Function		
An, Bn	Data Inputs		
On	Outputs		

TRUTH TABLE

Inputs		Outputs
An Bn		On
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

H = High Voltage Level L = Low Voltage Level

For I_{CC} reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0		V
VI	DC Input Voltage	$-0.5 \le V_1 \le +7.0$		V
Vo	DC Output Voltage	$-0.5 \le V_{O} \le V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
lok	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
Io	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Туре	Max	Unit
V _{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
VI	Input Voltage		0		5.5	V
V _O	Output Voltage	(HIGH or LOW State) (3-State)	0		V _{CC}	V
I _{OH}	HIGH Level Output Current	V _{CC} = 3.0 V - 3.6 V V _{CC} = 2.7 V - 3.0 V V _{CC} = 2.3 V - 2.7 V			-24 -12 -8	mA
I _{OL}	LOW Level Output Current	V _{CC} = 3.0 V - 3.6 V V _{CC} = 2.7 V - 3.0 V V _{CC} = 2.3 V - 2.7 V			+24 +12 +8	mA
T _A	Operating Free-Air Temperature		-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from	0.8 V to 2.0 V, V _{CC} = 3.0 V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

			T _A = -40°C		
Symbol	Characteristic	Condition	Min	Max	Unit
V _{IH}	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V _{CC} ≤ 3.6 V	2.0		1
V _{IL}	LOW Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V _{CC} ≤ 3.6 V		0.8	1
V _{OH}	HIGH Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{ I}_{OH} = -100 \mu\text{A}$	V _{CC} – 0.2		V
		$V_{CC} = 2.3 \text{ V; } I_{OH} = -8 \text{ mA}$	1.8		1
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		1
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		1
		V _{CC} = 3.0 V; I _{OH} = -24 mA	2.2		1
V _{OL}	LOW Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{I}_{OL} = 100 \mu\text{A}$		0.2	V
		$V_{CC} = 2.3 \text{ V; } I_{OL} = 8 \text{ mA}$		0.6	1
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	1
		V _{CC} = 3.0 V; I _{OL} = 16 mA		0.4	1
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	1
I _I	Input Leakage Current	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; 0 \text{ V} \le \text{V}_{I} \le 5.5 \text{ V}$		±5	μΑ
I _{CC}	Quiescent Supply Current	$2.3 \le V_{CC} \le 3.6 \text{ V}; V_I = \text{GND or } V_{CC}$		10	μΑ
		$2.3 \le V_{CC} \le 3.6 \text{ V}; 3.6 \le V_{I} \text{ or } V_{O} \le 5.5 \text{ V}$		±10	1
ΔI_{CC}	Increase in I _{CC} per Input	$2.3 \le V_{CC} \le 3.6 \text{ V}; V_{IH} = V_{CC} - 0.6 \text{ V}$		500	μΑ

^{2.} These values of V_{I} are used to test DC electrical characteristics only.

AC CHARACTERISTICS $t_R = t_F = 2.5 \text{ ns}$; $R_L = 500 \Omega$

					Lim	nits			
				$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$					
			V _{CC} = 3.3	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 2.7 \text{ V}$ $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$					
			C _L = 9	50 pF	C _L = 9	50 pF	C _L = 3	30 pF	
Symbol	Parameter	Waveform	Min	Max	Min	Max	Min	Max	Unit
t _{PLH}	Propagation Delay Time	1	1.5	5.5	1.5	6.2	1.5	6.6	ns
t _{PHL}	Input-to-Output		1.5	5.5	1.5	6.2	1.5	6.6	
toshl	Output-to-Output Skew			1.0					ns
toslh	(Note 3)			1.0					

Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (toSHL) or LOW-to-HIGH (toSLH); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

			T _A = +25°C			
Symbol	Characteristic	Condition	Min	Тур	Max	Unit
V _{OLP}	Dynamic LOW Peak Voltage	$V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$		0.8		V
	(Note 4)	$V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$		0.6		V
V _{OLV}	Dynamic LOW Valley Voltage	$V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$		-0.8		V
	(Note 4)	$V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$		-0.6		V

^{4.} Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

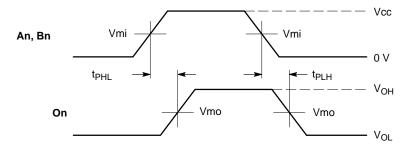
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	er Condition		Unit
C _{IN}	Input Capacitance	$V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	7	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	25	pF

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LCX00D	SOIC-14	55 Units / Rail
MC74LCX00DR2	SOIC-14	2500 Tape & Reel
MC74LCX00DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LCX00DT	TSSOP-14*	96 Units / Rail
MC74LCX00DTR2	TSSOP-14*	2500 Tape & Reel
MC74LCX00MEL	SOEIAJ-14	2000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. *This package is inherently Pb–Free.

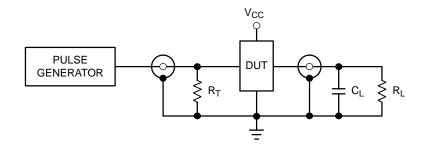


WAVEFORM 1 - PROPAGATION DELAYS

 $t_R = t_F = 2.5 \text{ ns}, 10\% \text{ to } 90\%; f = 1 \text{ MHz}; t_W = 500 \text{ ns}$

	Vcc				
Symbol	3.3 V <u>+</u> 0.3 V	2.7 V	2.5 V <u>+</u> 0.2 V		
Vmi	1.5 V	1.5 V	Vcc/2		
Vmo	1.5 V	1.5 V	Vcc/2		

Figure 3. AC Waveforms



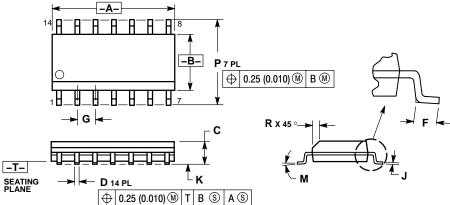
 $C_L=50$ pF at $V_{CC}=3.3\pm0.3$ V or equivalent (includes jig and probe capacitance) $C_L=30$ pF at $V_{CC}=2.5\pm0.2$ V or equivalent (includes jig and probe capacitance) $R_L=R_1=500~\Omega$ or equivalent

 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

PACKAGE DIMENSIONS

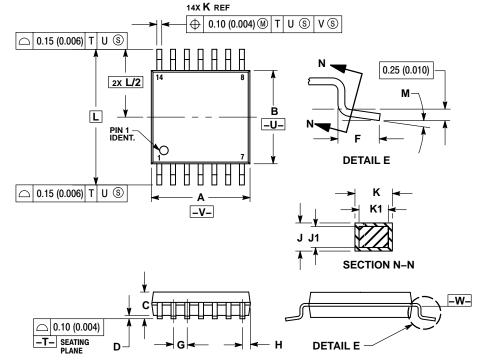
SOIC-14 **D SUFFIX** CASE 751A-03 ISSUE G



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE
 DAMBAR PROTRUSION. ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.127
 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050 BSC	
7	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
М	0 °	7°	0 °	7°
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP-14 **DT SUFFIX** CASE 948G-01 **ISSUE O**



- OTES.

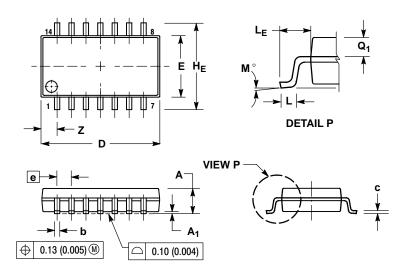
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.
- 2. OMTHOLIUM DIMELTION, MILEUITETT.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH,
 PROTRUSIONS OR GATE BURRS. MOLD FLASH
 OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED
- PROTRUSION SHALL NOT EXCEED
 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
 EXCESS OF THE K DIMENSION AT MAXIMUM
 MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	0.65 BSC		BSC
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

SOEIAJ-14 **M SUFFIX** CASE 965-01 **ISSUE O**



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10°
Q ₁	0.70	0.90	0.028	0.035
Z		1.42		0.056

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