Absolute Maximum Ratings (Note 1)

V_{IN} to SGND .....-0.3V to +80V
EN/UVLO to SGND .....-0.3V to +26V
EXTVCC to SGND .....-0.3V to +26V
LX to PGND.....-0.3V to (V_{IN} + 0.3V)
FB, $\overline{RESET}$, SS, MODE/ILIM, V_{CC}, RT/SYNC to SGND .....-0.3V to +6V
PGND to SGND.....-0.3V to +0.3V
LX Total RMS Current .....±1.6A

Continuous Power Dissipation (T_A = +70°C) (derate 24.4mW/°C above +70°C) (Multilayer board).....1951.2mW
Output Short-Circuit Duration .....Continuous
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Package Information

PACKAGE TYPE: 12 TDFN	
Package Code	TD1233+1C
Outline Number	**21-0664**
Land Pattern Number	**90-0397**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8.5°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 24V, $V_{EN/UVLO}$ = unconnected, R_{RT} = 105kΩ (f_{SW} = 400kHz), LX = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		76	V
Input Shutdown Current	I_{IN-SH}	V_{EN} = 0V, shutdown mode	2.5	5	10	µA
Input Quiescent Current	I_{Q_PFM}	R_{ILIM} = open or 422kΩ		195		µA
	I_{Q_PWM}	R_{ILIM} = 243kΩ or 121kΩ	3	4	5	mA
ENABLE/UVLO (EN)						
EN Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.09	1.115	1.14	
	$V_{EN-TRUESD}$	$V_{EN/UVLO}$ falling, true shutdown		0.7		
EN Pullup Current	I_{EN}	VEN/UVLO = 1.215V	2.2	2.5	2.8	µA

Electrical Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = unconnected, R_{RT} = 105kΩ (f_{SW} = 400kHz), LX = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO (V_{CC})						
V_{CC} Output Voltage Range	VCC	6V < V_{IN} < 76V, 0mA < I_{VCC} < 5mA	4.75	5	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 12V	13	26	52	mA
V_{CC} Dropout	VCC-DO	V_{IN} = 4.5V, I_{VCC} = 5mA			0.25	V
V_{CC} UVLO	VCC-UVR	V_{CC} rising	4.05	4.2	4.35	V
	VCC-UVF	V_{CC} falling	3.65	3.8	3.95	V
EXT LDO						
EXTVCC Switchover Threshold		EXTVCC rising	4.65	4.744	4.85	V
EXTVCC Switchover Threshold Hysteresis				0.3		V
EXTVCC Dropout	EXTVCC-DO	EXTVCC = 4.75V, I_{VCC} = 5mA			0.1	V
EXTVCC Current Limit	IVCC-MAX	V_{CC} = 4.3V, EXTVCC = 5V	15	21	34	mA
POWER MOSFETs						
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A, sourcing		0.9	1.8	Ω
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A, sinking		0.275	0.55	Ω
LX Leakage Current	I_{LX-LKG}	V_{IN} = 76V, T_A = +25°C, V_{LX} = (V_{PGND} + 1V) to (V_{IN} - 1V)	-1		+1	µA
SOFT-START						
Charging Current	I_{SS}		4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}	R_{ILIM} = 243kΩ or 121kΩ	0.788	0.8	0.812	V
FB Regulation Voltage	V_{FB-REG}	R_{ILIM} = open or 422kΩ	0.788	0.812	0.824	V
FB Input Leakage Current	I_{FB}	V_{FB} = 1V, T_A = +25°C	-100		+100	nA
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{SOURCE-LIMIT}$	R_{ILIM} = open or R_{ILIM} = 243KΩ	1.41	1.6	1.83	A
		R_{ILIM} = 121kΩ or R_{ILIM} = 422kΩ	0.94	1.14	1.3	A
Negative Current-Limit Threshold	$I_{SINK-LIMIT}$	R_{ILIM} = open or R_{ILIM} = 422kΩ		2.5		mA
		R_{ILIM} = 243kΩ	0.57	0.65	0.725	A
		R_{ILIM} = 121kΩ	0.35	0.455	0.56	A
PFM Current Level	IPFM	R_{ILIM} = open	0.235	0.33	0.44	A
		R_{ILIM} = 422kΩ	0.125	0.23	0.32	A

Electrical Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = unconnected, R_{RT} = 105kΩ (f_{SW} = 400kHz), LX = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

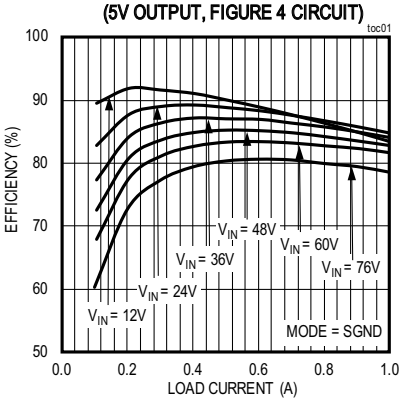
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MODE						
MODE PFM Threshold		Rising	1	1.22	1.44	V
Hysteresis				0.19		V
TIMINGS						
Minimum On-Time	t_{ON-MIN}		45	70	110	ns
Maximum Duty Cycle	DMAX		90	93	97	%
OSCILLATOR						
Switching Frequency	f_{SW}	R_{RT} = 210kΩ	180	200	220	kHz
		R_{RT} = 140kΩ	270	300	330	kHz
		R_{RT} = 105kΩ	360	400	440	kHz
		R_{RT} = 69.8KΩ	540	600	660	kHz
Switching Frequency Adjustable Range			200		600	kHz
SYNC Input Frequency			1.15 × f_{SW}		1.4 × f_{SW}	kHz
SYNC Pulse Minimum Off time			40			ns
SYNC High Threshold	V_{SYNC-H}		1	1.22	1.44	V
Hysteresis	$V_{SYNC-HYS}$			0.18		V
Number of SYNC Pulses to Enable Synchronization				1		Cycles
$\overline{\text{RESET}}$						
FB Threshold for $\overline{\text{RESET}}$ Rising	V_{FB-OKR}	V_{FB} rising		95		%
FB Threshold for $\overline{\text{RESET}}$ Falling	V_{FB-OKF}	V_{FB} falling		92		%
$\overline{\text{RESET}}$ Delay After FB Reaches 95% Regulation				2.1		ms
$\overline{\text{RESET}}$ Output Level Low		$I_{\overline{\text{RESET}}}$ = 1mA			0.07	V
$\overline{\text{RESET}}$ Output Leakage Current		V_{FB} = 1.063 × V_{FB-REG}, T_A = +25°C			1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		160		°C
Thermal-Shutdown Hysteresis				20		°C

Note 2: All limits are 100% tested at +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Typical Operating Characteristics

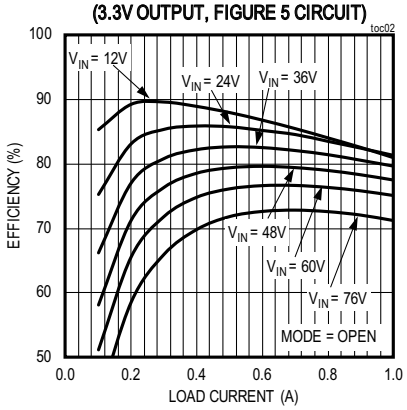
(V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, $V_{EN/UVLO}$ = Open, C_{SS} = 5600pF, MODE/ILIM = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

EFFICIENCY VS. LOAD CURRENT
(5V OUTPUT, FIGURE 4 CIRCUIT)



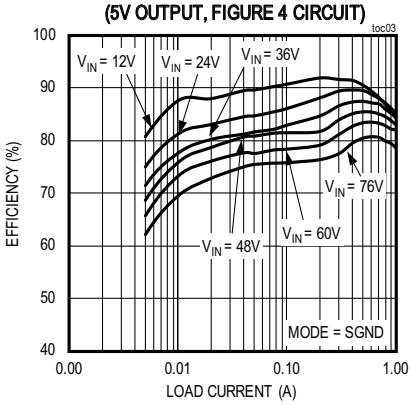
CONDITIONS: PWM MODE, f_{SW} = 400kHz

EFFICIENCY VS. LOAD CURRENT
(3.3V OUTPUT, FIGURE 5 CIRCUIT)



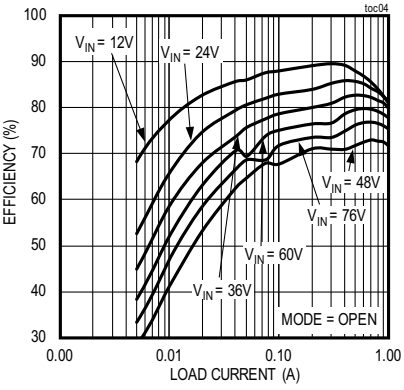
CONDITIONS: PWM MODE, f_{SW} = 400kHz

EFFICIENCY VS. LOAD CURRENT
(5V OUTPUT, FIGURE 4 CIRCUIT)



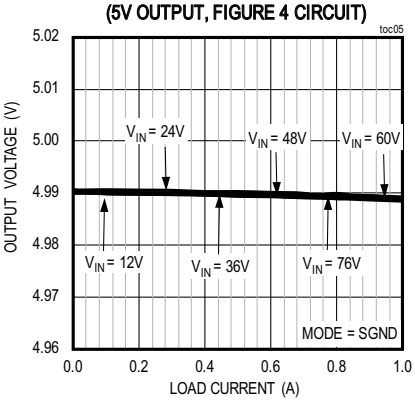
CONDITIONS: PFM MODE, f_{SW} = 400kHz

EFFICIENCY VS. LOAD CURRENT
(3.3V OUTPUT, FIGURE 5 CIRCUIT)



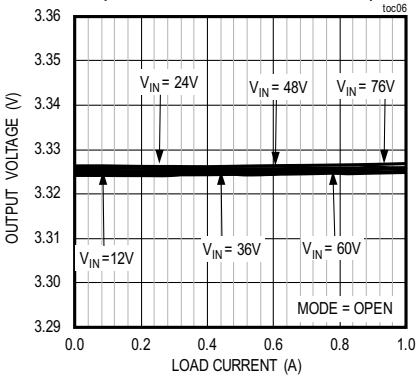
CONDITIONS: PFM MODE, f_{SW} = 400kHz

LOAD AND LINE REGULATION
(5V OUTPUT, FIGURE 4 CIRCUIT)



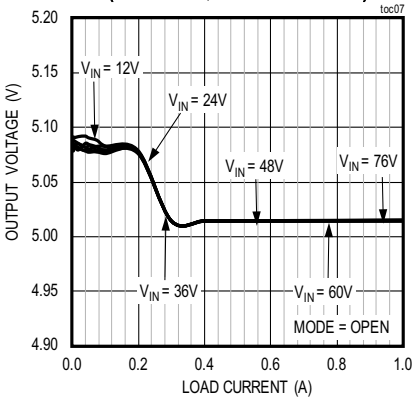
CONDITIONS: PWM MODE

LOAD AND LINE REGULATION
(3.3V OUTPUT, FIGURE 5 CIRCUIT)



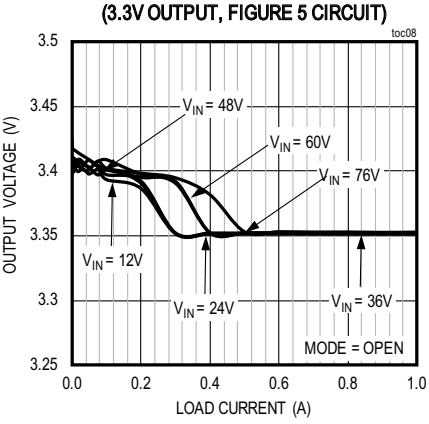
CONDITIONS: PWM MODE

LOAD AND LINE REGULATION
(5V OUTPUT, FIGURE 4 CIRCUIT)



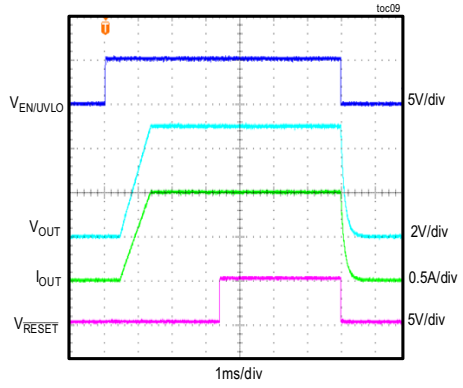
CONDITIONS: PFM MODE

LOAD AND LINE REGULATION
(3.3V OUTPUT, FIGURE 5 CIRCUIT)



CONDITIONS: PFM MODE

SOFT-START/SHUTDOWN FROM EN/UVLO
(5V OUTPUT, FIGURE 4 CIRCUIT)

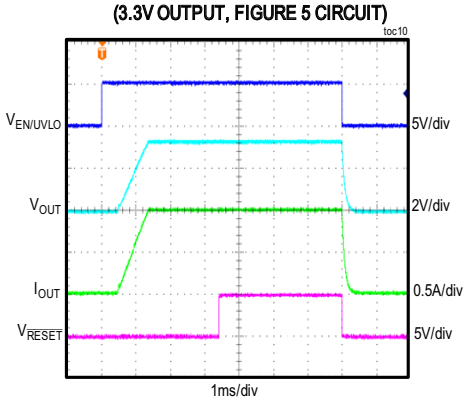


CONDITIONS: 1A LOAD CURRENT

Typical Operating Characteristics (continued)

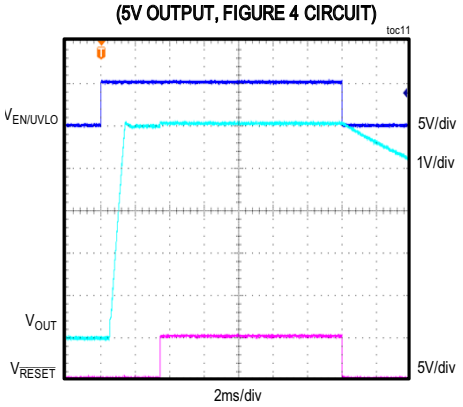
(V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, $V_{EN/UVLO}$ = Open, C_{SS} = 5600pF, MODE/ILIM = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

SOFT-START/SHUTDOWN FROM EN/UVLO (3.3V OUTPUT, FIGURE 5 CIRCUIT)



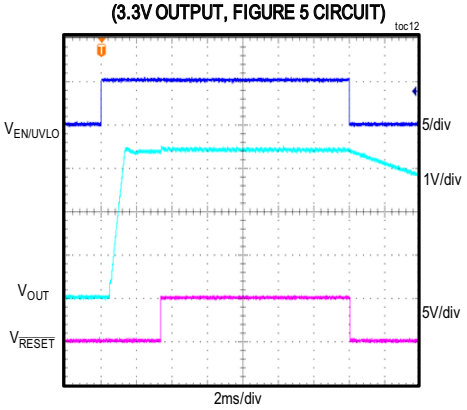
CONDITIONS: 1A LOAD CURRENT

SOFT-START/SHUTDOWN FROM EN/UVLO (5V OUTPUT, FIGURE 4 CIRCUIT)



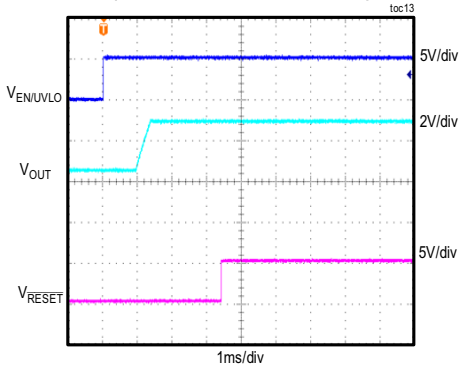
CONDITIONS: PFM MODE, 5MA LOAD CURRENT

SOFT-START/SHUTDOWN FROM EN/UVLO (3.3V OUTPUT, FIGURE 5 CIRCUIT)



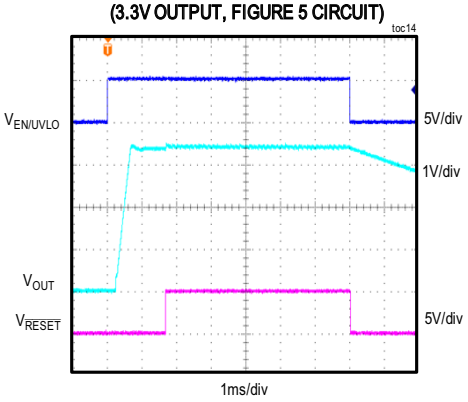
CONDITIONS: PFM MODE, 5MA LOAD CURRENT

SOFT-START WITH 2.5V PREBIAS (5V OUTPUT, FIGURE 4 CIRCUIT)



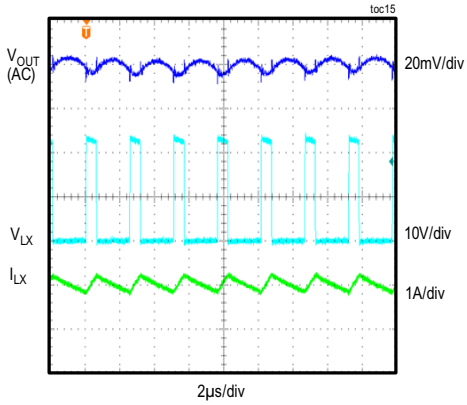
CONDITIONS: PWM MODE

SOFT-START WITH 2.5V PREBIAS (3.3V OUTPUT, FIGURE 5 CIRCUIT)



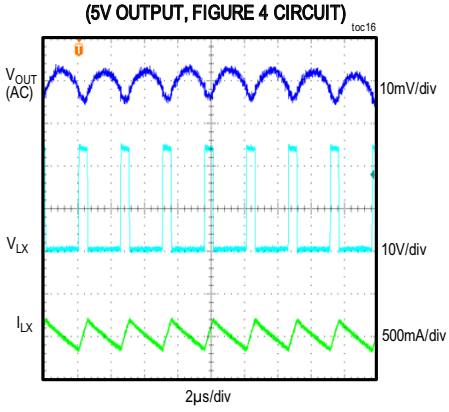
CONDITIONS: PWM MODE

STEADY-STATE SWITCHING WAVEFORMS (5V OUTPUT, FIGURE 4 CIRCUIT)



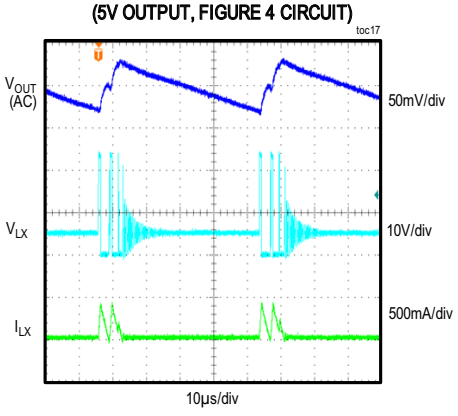
CONDITIONS: 1A LOAD CURRENT

STEADY-STATE SWITCHING WAVEFORMS (5V OUTPUT, FIGURE 4 CIRCUIT)



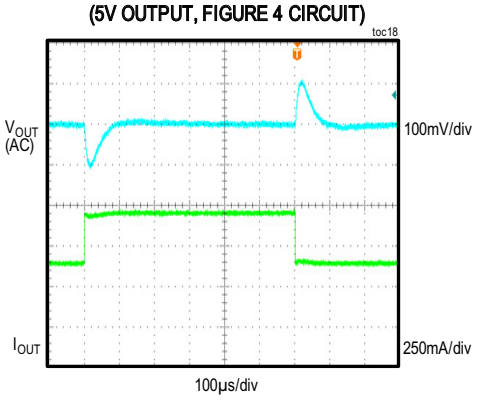
CONDITIONS: NO LOAD CURRENT

STEADY-STATE SWITCHING WAVEFORMS (5V OUTPUT, FIGURE 4 CIRCUIT)



CONDITIONS: PFM MODE, 25mA LOAD CURRENT

LOAD CURRENT STEPPED FROM 0.5A TO 0.75A (5V OUTPUT, FIGURE 4 CIRCUIT)

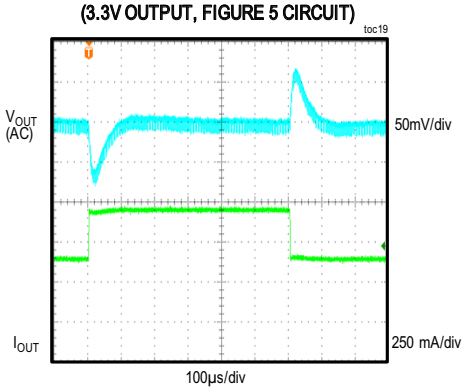


CONDITIONS: PWM MODE

Typical Operating Characteristics (continued)

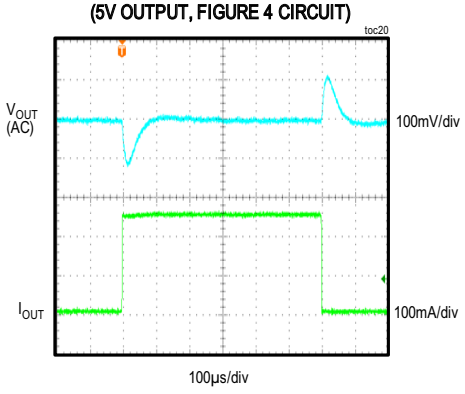
(V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, $V_{EN/UVLO}$ = Open, C_{SS} = 5600pF, MODE/ILIM = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

LOAD CURRENT STEPPED FROM 0.5A TO 0.75A
(3.3V OUTPUT, FIGURE 5 CIRCUIT)



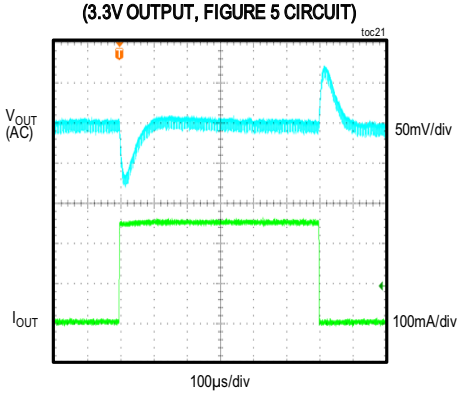
CONDITIONS: PWM MODE

LOAD CURRENT STEPPED FROM 0A TO 0.25A
(5V OUTPUT, FIGURE 4 CIRCUIT)



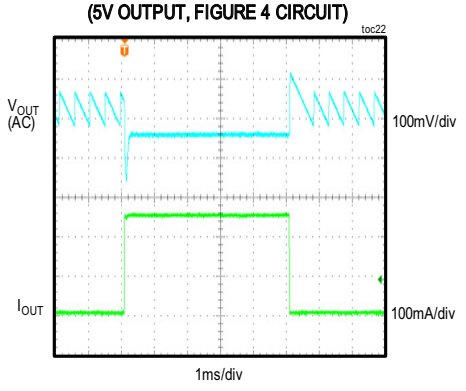
CONDITIONS: PWM MODE

LOAD CURRENT STEPPED FROM 0A TO 0.25A
(3.3V OUTPUT, FIGURE 5 CIRCUIT)



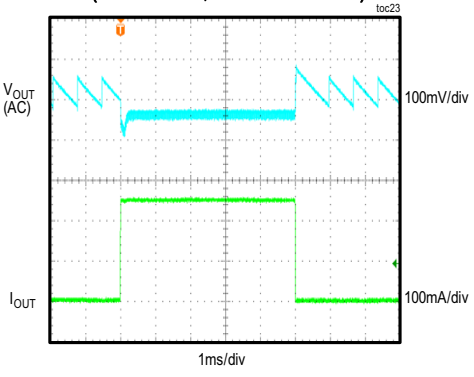
CONDITIONS: PWM MODE

LOAD CURRENT STEPPED FROM 0A TO 0.25A
(5V OUTPUT, FIGURE 4 CIRCUIT)



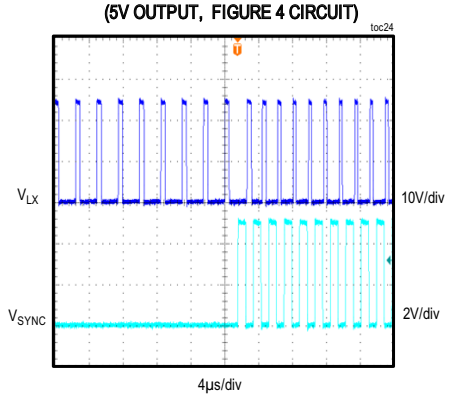
CONDITIONS: PFM MODE

LOAD CURRENT STEPPED FROM 0A TO 0.25A
(3.3V OUTPUT, FIGURE 5 CIRCUIT)

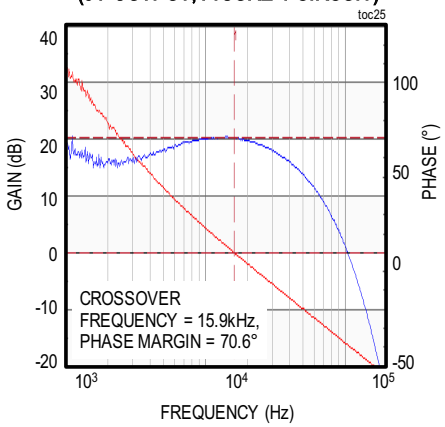


CONDITIONS: PFM MODE

APPLICATION OF EXTERNAL CLOCK AT 600kHz
(5V OUTPUT, FIGURE 4 CIRCUIT)

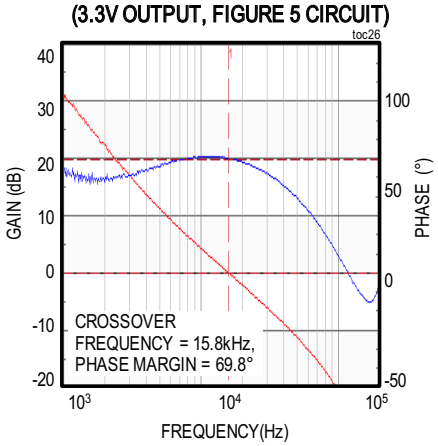


BODE PLOT
(5V OUTPUT, FIGURE 4 CIRCUIT)



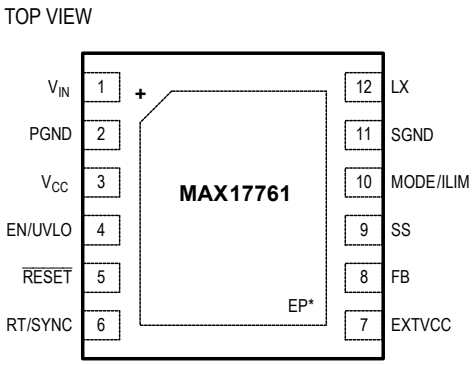
CONDITIONS: 1A LOAD CURRENT

BODE PLOT
(3.3V OUTPUT, FIGURE 5 CIRCUIT)



CONDITIONS: 1A LOAD CURRENT

Pin Configuration



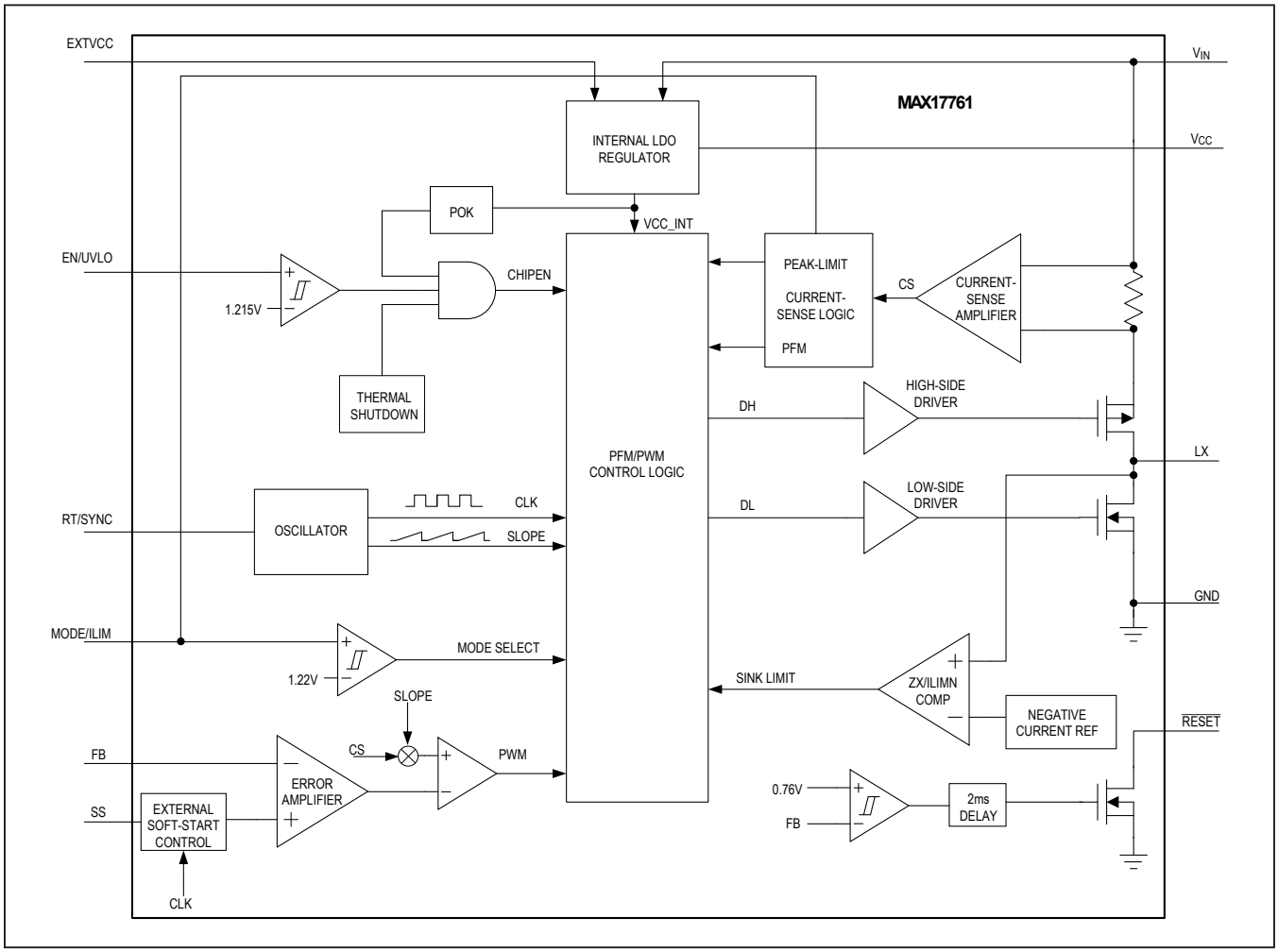
TDFN
(3mm x 3mm)

*EP = EXPOSED PAD , CONNECTED TO SGND

Pin Description

PIN	NAME	FUNCTION
V_{IN}	1	Power-Supply Input. 4.5V to 76V input supply range. Decouple to PGND with a 2.2µF capacitor; place the capacitor close to the V_{IN} and PGND pins.
PGND	2	Power Ground Pin of the Converter. Connect externally to the power ground plane. Connect the SGND and PGND pins together at the ground return path of the V_{CC} bypass capacitor.
V_{CC}	3	5V LDO Output. Bypass V_{CC} with a 1µF ceramic capacitance to SGND.
EN/UVLO	4	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect to the center of the resistor-divider between V_{IN} and SGND to set the input voltage at which the part turns on. Leave the pin floating for always on operation.
$\overline{RESET}$	5	Open-Drain $\overline{RESET}$ Output. The $\overline{RESET}$ output is driven low if FB drops below 92% of its set value. $\overline{RESET}$ goes high 2.1ms after FB rises above 95% of its set value.
RT/SYNC	6	Connect a resistor from RT/SYNC to SGND to set the switching frequency of the part between 200kHz and 600kHz. An external clock can be connected to the RT/SYNC pin to synchronize the part with an external frequency.
EXTVCC	7	External Power Supply Input for the Internal LDO.
FB	8	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to SGND to set the output voltage.
SS	9	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
MODE/ILIM	10	Connect a resistor from MODE/ILIM to SGND to program the peak and runaway current limits and mode of operation of the part. See the *Current Limit and Mode of Operation Selection* section for more details.
SGND	11	Analog Ground.
LX	12	Switching Node. Connect LX pin to the switching-side of the inductor.
EP	—	Exposed Pad. Connect to the SGND pin. Connect to a large copper plane below the IC to improve heat dissipation capability. Add thermal vias below the exposed pad.

Functional (or Block) Diagram



Detailed Description

The MAX17761 step-down regulator operates from 4.5V to 76V and delivers up to 1A load current on output. Feedback voltage regulation accuracy meets ±1.5% over load, line, and temperature.

The device uses a peak-current-mode control scheme. An internal transconductance error amplifier generates an integrated error voltage. The error voltage sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator.

At each rising-edge of the clock, the high-side pMOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected.

During the high-side MOSFET's on-time, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side nMOSFET turns on and remains on until either the next rising edge of the clock arrives or sink current limit is detected. The inductor releases the stored energy as its current ramps down, and provides current to the output. The internal low R_{DSON} pMOS/nMOS switches ensure high efficiency at full load.

This device also integrates switching frequency selector pin, current limit and mode of operation selector pin, enable/undervoltage lockout (EN/UVLO) pin, programmable soft-start pin and open-drain $\overline{RESET}$ signal.

Current Limit and Mode of Operation Selection

The following table lists the value of the resistors to program PWM or PFM modes of operation and 1.6A or 1.14A peak current limits.

The mode of operation cannot be changed on-the-fly after power-up.

Table 1. R_{ILIM} Resistor vs. Modes of Operation and Peak Current Limit

R_{ILIM} (kΩ)	MODE OF OPERATION	PEAK CURRENT LIMIT (A)
OPEN	PFM	1.6
422	PFM	1.14
243	PWM	1.6
121	PWM	1.14

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to the PFM mode of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak every clock cycle until the output rises to 102% of the nominal voltage. Once the output reaches 102% of the nominal voltage, both the high side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks and again commences the process of delivering pulses of energy to the output until it reaches 102% of the nominal output voltage.

The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. However, the output-voltage ripple is higher compared to PWM mode of operation and switching frequency is not constant at light loads.

Linear Regulator (V_{CC})

The MAX17761 has two internal low dropout regulators (LDO), which power V_{CC}. One LDO is powered from input voltage and the other LDO is powered from the EXTVCC pin. Only one of the two LDOs is in operation at a time, depending on the voltage levels present at the EXTVCC pin.

If EXTVCC is greater than 4.74V (typ), V_{CC} is powered from the EXTVCC pin. If EXTVCC is lower than 4.44V (typ), V_{CC} is powered from input voltage. Powering V_{CC} from EXTVCC increases efficiency particularly at higher input voltages. Typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 1µF cap. Both the LDOs can source up to 13mA.

When V_{CC} falls below its undervoltage lockout (3.8V(typ)), the internal step-down controller is turned off, and LX switching is disabled. The LX switching is enabled again when the V_{CC} voltage exceeds 4.2V (typ). The 400mV (typ) hysteresis prevents chattering on power-up/power-down.

When the EXTVCC is connected to the output and the output is shorted such that inductive ringings cause the output voltage to become temporarily negative, a R-C network should be connected between the output and the EXTVCC pin. A 4.7Ω between the output and the pin and a 0.1µF from the pin to ground is recommended.

Switching Frequency Selection and External Frequency synchronization

The RT/SYNC pin programs the switching frequency of the converter. Connect a resistor from RT/SYNC to SGND to set the switching frequency of the part at any one of four discrete frequencies—200kHz, 300kHz, 400kHz, and 600kHz. Table 2 provides resistor values.

The internal oscillator of the device can be synchronized to an external clock signal on the RT/SYNC pin. The external synchronization clock frequency must be between 1.15 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the frequency programmed by the resistor connected from the RT/SYNC pin.

Table 2. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT/SYNC RESISTOR VALUE (kΩ)
200	210
300	140
400	105
600	69.8

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR} + 0.55))}{D_{MAX}} + (I_{OUT(MAX)} \times 1.25)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON(MIN)}}$$

where,

V_{OUT} = The steady-state output voltage,

$I_{OUT(MAX)}$ = The maximum load current,

R_{DCR} = The DC resistance of the inductor,

D_{MAX} = The maximum allowable duty ratio (0.9),

$f_{SW(MAX)}$ = The maximum switching frequency,

$t_{ON(MIN)}$ = The worst-case minimum switch on-time (110ns).

Overcurrent Protection

The device is provided with a robust overcurrent-protection scheme that protects the device under overload and output short-circuits conditions. The positive current limit is triggered when the peak value of the inductor current hits a fixed threshold (ILIM_P, 1.6A/1.14A, depending on the value of the resistor connected to the MODE/ILIM pin). At this point, the high-side switch is turned off and the low-side switch is turned on. The low-side switch is kept on until the inductor current discharges below 0.7 x ILIM_P.

While in PWM mode of operation, the negative current limit is triggered when the valley value of the inductor current hits a fixed threshold (ILIM_N, -0.65A/-0.455A, depending on the value of the resistor connected to the MODE/ILIM pin). At this point, the low-side switch is turned off and the high-side switch is turned on.

$\overline{\text{RESET}}$ Output

The device includes $\overline{\text{RESET}}$ pin to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) in 2.1ms after the output voltage increases above 95% of the nominal voltage. $\overline{\text{RESET}}$ goes low when the output voltage drops to below 92% of the nominal voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown.

Prebiased Output

When the device starts into a prebiased output, both the high-side and low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences first with the high-side switch. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +160°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown protection in normal operation.

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) for a single output is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ = The maximum load current, I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1-D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where,

D = V_{OUT}/V_{IN} is the duty ratio of the controller,

f_{SW} = The switching frequency,

ΔV_{IN} = The allowable input voltage ripple,

η = The efficiency.

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

For R_{ILIM} = OPEN or R_{ILIM} = 243kΩ,

$$L = \frac{2.6 \times V_{OUT}}{f_{SW}}$$

For R_{ILIM} = 121kΩ or R_{ILIM} = 422kΩ,

$$L = \frac{3.7 \times V_{OUT}}{f_{SW}}$$

where, V_{OUT} and f_{SW} are nominal values. Select an inductor whose value is nearest to the value calculated by the previous formula.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in Industrial applications. The output capacitor is sized to support a step load of 25% of the maximum output current in the application, such that the output voltage deviation is contained to 3% of the output voltage change. The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.33}{f_C}$$

where,

I_{STEP} = The load-current step,

$t_{RESPONSE}$ = The response time of the controller,

ΔV_{OUT} = The allowable output-voltage deviation,

f_C = The target closed-loop crossover frequency (f_C is chosen to be 15kHz or 1/20th of f_{SW}, whichever is lower),

f_{SW} = The switching frequency.

Derating of ceramic capacitors with DC-voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors.

Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time for the corresponding output voltage. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 30 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{6.25 \times 10^{-6}}$$

For example, to program a 2ms soft-start time, a 12nF capacitor should be connected from the SS pin to SGND.

Adjusting Output Voltage

Set the output voltage with resistive voltage-dividers connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (Figure 1). Connect the centre node of the divider to the FB pin. To optimize efficiency and output accuracy, use the following calculations to choose the resistive divider values:

$$R4 = \frac{15 \times V_{OUT}}{0.8}$$

$$R5 = \frac{R4 \times 0.8}{(V_{OUT} - 0.8)}$$

where R4 and R5 are in kΩ.

Setting the Undervoltage Lockout Level

Drive EN/UVLO high to enable the output. Leave the pin floating for always on operation. Set the voltage at which each converter turns on with a resistive voltage-divider connected from V_{IN} to SGND (see Figure 2). Connect the center node of the divider to EN/UVLO pin.

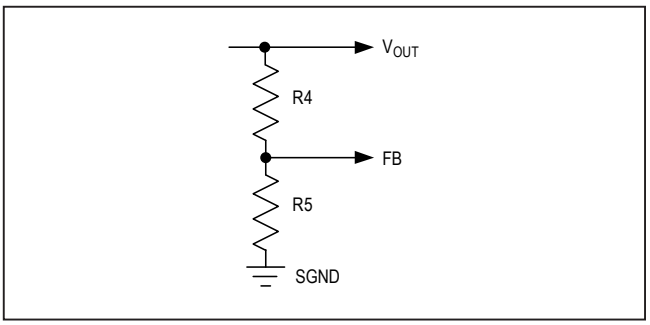


Figure 1. Adjusting Output Voltage

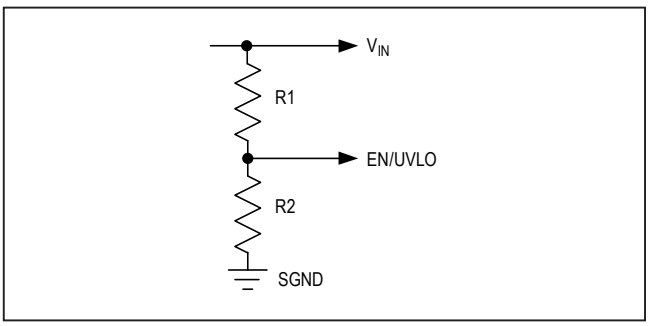


Figure 2. Setting the Undervoltage Lockout Level

Choose R1 as follows:

$$R1 \le (110000 \times V_{INU})$$

where V_{INU} is the input voltage at which the MAX17761 is required to turn on and R1 is in Ω. Calculate the value of R2 as follows:

$$R2 = \frac{1.215 \times R1}{(V_{INU} - 1.215 + (2.5\mu A \times R1))}$$

Series R-C Selection Across Bottom Feedback Resistor

In order to achieve the targeted bandwidth, R-C series circuit is connected across bottom feedback resistor (Figure 3). Selection procedure for series R-C (R6 and C6) values are as follows:

$$R6 = \frac{R4 \times R5}{R4 + R5} \times \frac{k}{1 - 0.99k}$$

$$C6 = \frac{1.125 \times 10^6}{f_C \times \sqrt{\frac{k}{1 - K^2}} \times R6}$$

where,

$$k = \frac{f_C \times C_{OUT} \times \left(1 + \frac{R4}{R5}\right)}{3.6274 \times 10^6}$$

C_{OUT} = The actual derated capacitance value for a given bias voltage of selected output capacitor in µF,

f_C = The targeted crossover frequency in Hz,

R4 and R5 = The feedback network values in kΩ,

R6 and C6 are in kΩ and nF respectively.

Power Dissipation

The exposed pad of the IC should be properly soldered to the PCB to ensure good thermal contact.

At a particular operating condition, the power losses that lead to temperature rise of the device are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - \left(I_{OUT}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where,

P_{OUT} = The output power,

η = The efficiency of the device

R_{DCR} = The DC resistance of the output inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

For a typical multilayer board, the thermal performance metrics for the 12-pin TDFN package are given as:

$$\theta_{JA} = 41°C/W$$

$$\theta_{JC} = 8.5°C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the following equation:

$$T_{J\_MAX} = T_{A\_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J\_MAX} = T_{EP\_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperatures greater than +125°C degrade operating lifetimes.

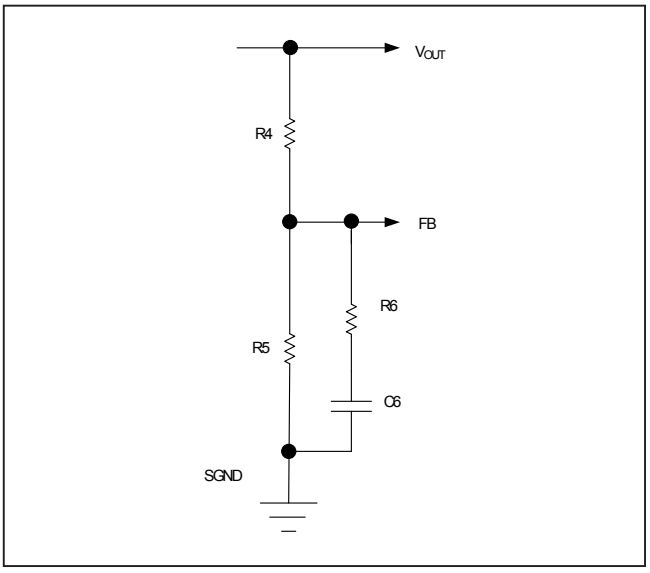


Figure 3. Setting R-C Series Network

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and stable operation. For a sample layout that ensures first-pass success, refer to the MAX17761 evaluation kit layouts available at **www.maximintegrated.com**. Follow these guidelines for good PCB layout:

All connections carrying pulsed currents must be very short and as wide as possible. The loop area of these connections must be made very small to reduce stray inductance and radiated EMI.

A ceramic input filter capacitor should be placed close to the V_{IN} pin of the device. The bypass capacitor for the V_{CC} pin should also be placed close to the V_{CC} pin. The feedback trace should be routed as far as possible from the inductor.

The analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at minimum, typically the return terminal of the V_{CC} bypass capacitor. The ground plane should be kept continuous as much as possible.

A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the device for efficient heat dissipation.

Typical Application Circuits

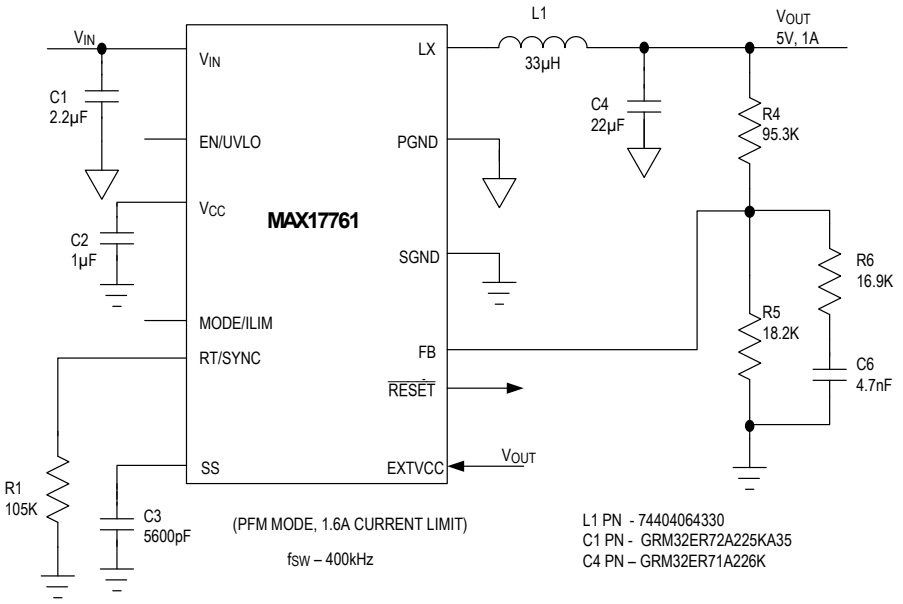


Figure 4. ***5V Output*** *Typical Application Circuit (Part is Always On when the EN/UVLO Pin is Unconnected)*

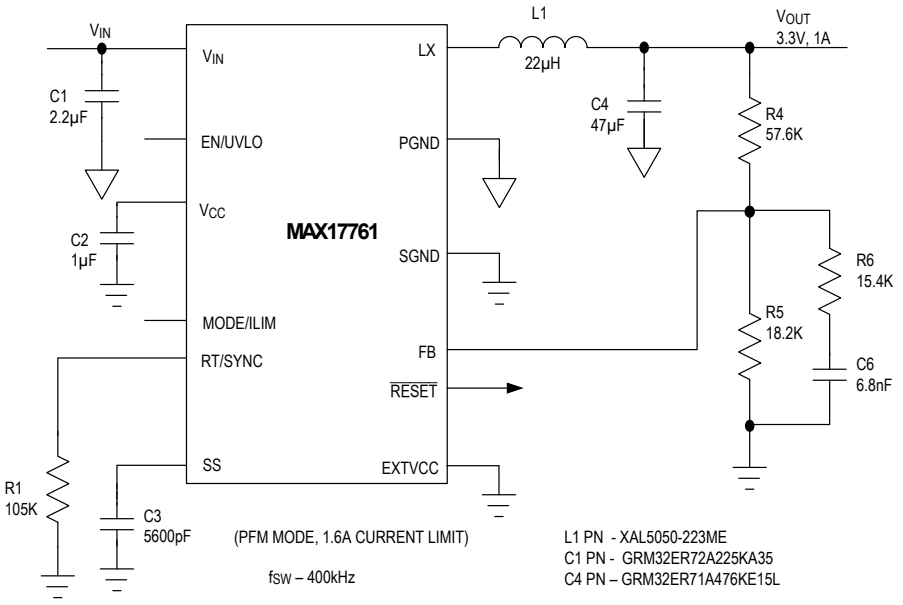


Figure 5. ***3.3V Output*** *Typical Application Circuit (Part is Always On when the EN/UVLO Pin is Unconnected)*

Ordering Information

PART	PIN-PACKAGE	PIN-PACKAGE
MAX17761ATC+	12 TDFN-EP*	3mm x 3mm

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—

