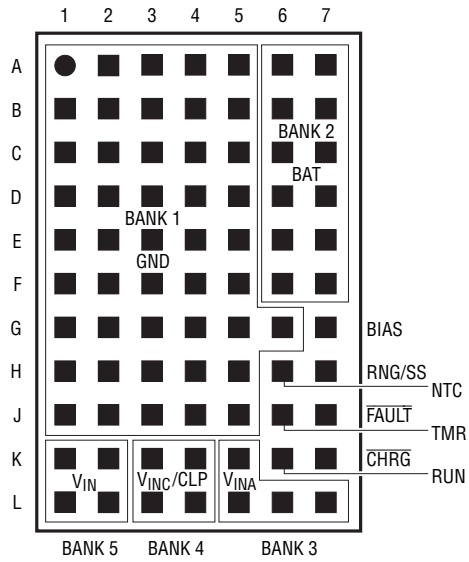
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{INA}, $V_{INC/CLP}$, V_{IN} 40V
RUN, $\overline{CHRG}$, $\overline{FAULT}$ ..... V_{IN} + 0.5, 40V
TMR, RNG/SS, NTC 2.5V
BIAS, BAT 10V
Internal Operating Temperature
(Note 2) ..... 125°C
Maximum Body Solder Temperature ..... 245°C

PIN CONFIGURATION



LGA PACKAGE
77-LEAD (15mm × 9mm × 4.32mm)

T_{JMAX} = 125°C, θ_{JA} = 17.0°C/W, θ_{JCtop} = 16.2°C/W,
$\theta_{JCbottom}$ = 6.1°C/W, θ_{JB} = 11.2°C/W,
θ values determined per JEDEC 51-9, 51-12
Weight = 1.7g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM8061EV-4.1#PBF	LTM8061EV-4.1#PBF	LTM8061V-41	77-Lead (15mm × 9mm × 4.32mm)	–40°C to 125°C
LTM8061IV-4.1#PBF	LTM8061IV-4.1#PBF	LTM8061V-41	77-Lead (15mm × 9mm × 4.32mm)	–40°C to 125°C
LTM8061EV-4.2#PBF	LTM8061EV-4.2#PBF	LTM8061V-42	77-Lead (15mm × 9mm × 4.32mm)	–40°C to 125°C
LTM8061IV-4.2#PBF	LTM8061IV-4.2#PBF	LTM8061V-42	77-Lead (15mm × 9mm × 4.32mm)	–40°C to 125°C
LTM8061EV-8.2#PBF	LTM8061EV-8.2#PBF	LTM8061V-82	77-Lead (15mm × 9mm × 4.32mm)	–40°C to 125°C
LTM8061IV-8.2#PBF	LTM8061IV-8.2#PBF	LTM8061V-82	77-Lead (15mm × 9mm × 4.32mm)	–40°C to 125°C
LTM8061EV-8.4#PBF	LTM8061EV-8.4#PBF	LTM8061V-84	77-Lead (15mm × 9mm × 4.32mm)	–40°C to 125°C
LTM8061IV-8.4#PBF	LTM8061IV-8.4#PBF	LTM8061V-84	77-Lead (15mm × 9mm × 4.32mm)	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C. RUN = 2V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage					32	V
V_{IN} Start Voltage	LTM8061-4.1/LTM8061-4.2 LTM8061-8.2/LTM8061-8.4	● ●			7.5 11.5	V V
V_{IN} OVLO Threshold	V_{IN} Rising		32	35	40	V
V_{IN} OVLO Hysteresis				1		V
V_{IN} UVLO Threshold	LTM8061-4.1/LTM8061-4.2 LTM8061-8.2/LTM8061-8.4, V_{IN} Rising			4.6 8.7		V V
V_{IN} UVLO Hysteresis				0.3		V
V_{INA} to V_{INC}/CLP Diode Forward Voltage Drop	V_{INA} Current = 2A			0.55		V
BAT Float Voltage	LTM8061-4.1 LTM8061-4.2 LTM8061-8.2 LTM8061-8.4 	 ● ● ● ●	4.08 4.06 4.18 4.16 8.16 8.12 8.36 8.32	4.1 4.2 8.2 8.4 	4.12 4.14 4.22 4.24 8.24 8.28 8.44 8.48	V V V V V V V V
Maximum BAT Charge Current	(Note 3)		1.70		2.0	A
BAT Recharge Threshold Voltage	LTM8061-4.1/LTM8061-4.2, Relative to BAT Float Voltage LTM8061-8.2/LTM8061-8.4, Relative to BAT Float Voltage			–100 –200		mV mV
BAT Precondition Threshold Voltage	LTM8061-4.1/LTM8061-4.2 LTM8061-8.2 LTM8061-8.4			2.9 5.65 5.80		V V V
BAT Precondition Threshold Hysteresis Voltage				90		mV
Input Supply Current	Standby Mode, Not Switching RUN = 0.4V			85 15		µA µA
Minimum BIAS Voltage for Proper Operation					2.9	V
V_{INC}/CLP Threshold Voltage				50		mV
V_{INC}/CLP Input Bias Current				200		nA
NTC Range Limit Voltage (High)	V_{NTC} Rising		1.25	1.36	1.45	V
NTC Range Limit Voltage (Low)	V_{NTC} Falling		0.265	0.29	0.315	V
NTC Threshold Hysteresis	For Both High and Low Range Limits			20		%
NTC Disable Impedance	(Note 4)		250	500		kΩ
NTC Bias Current	V_{NTC} = 0.8V		47.5	50	52.5	µA
RNG/SS Bias Current			45	50	55	µA
Current Charge Programming: $V_{RNG/SS}$/BAT Current			0.42	0.50	0.58	V/A
RUN Threshold Voltage	V_{RUN} Rising		1.15	1.20	1.25	V
RUN Hysteresis Voltage				120		mV
RUN Input Bias Current				1		µA
$\overline{CHRG}$, $\overline{FAULT}$ Output Low Voltage	10mA Load on $\overline{CHRG}$, $\overline{FAULT}$ Pins				0.4	V
TMR Charge/Discharge Current				25		µA
TMR Disable Threshold Voltage			0.1	0.25		V
C/10 Termination Current	RNG/SS Open			200		mA
Operating Frequency			0.9	1	1.1	MHz

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

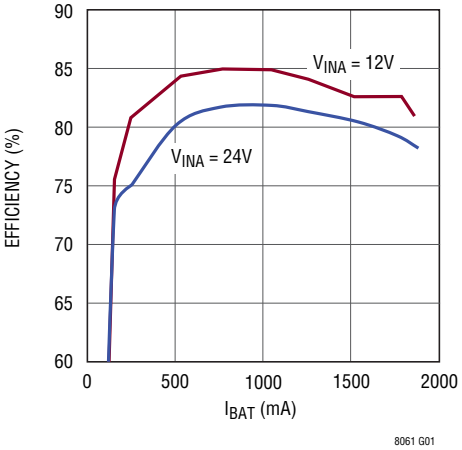
Note 2: The LTM8061E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C internal temperature range are assured by design, characterization and correlation with statistical process controls. LTM8061I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The maximum BAT charge current is reduced by thermal foldback. See the Typical Performance Characteristics section for details.

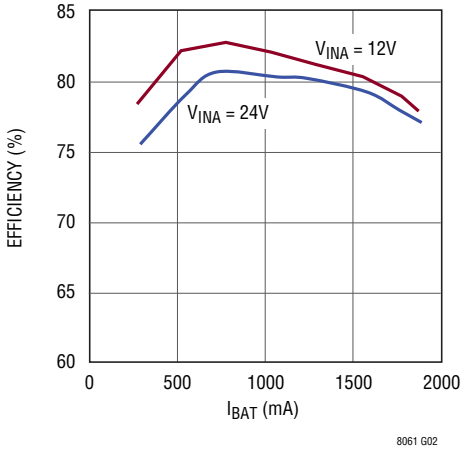
Note 4: Guaranteed by design and correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

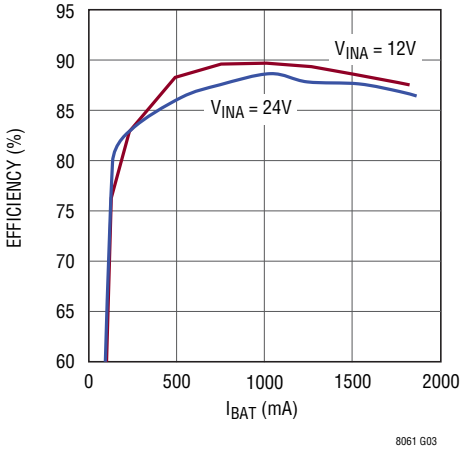
Efficiency vs I_{BAT}, 4.1V_{BAT}



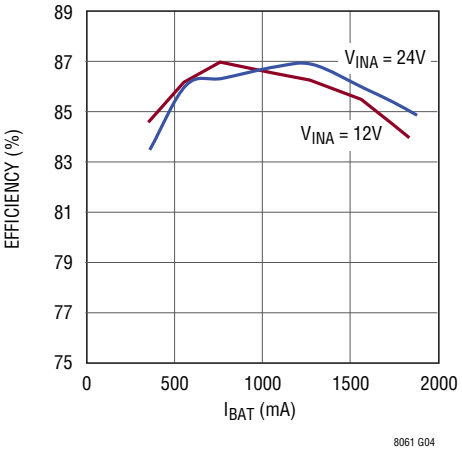
Efficiency vs I_{BAT}, 4.2V_{BAT}



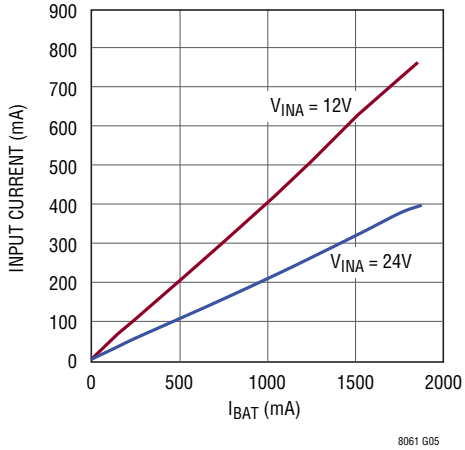
Efficiency vs I_{BAT}, 8.2V_{BAT}



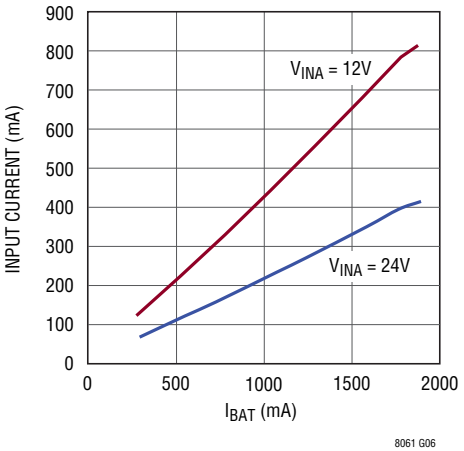
Efficiency vs I_{BAT}, 8.4V_{BAT}



Input Current vs I_{BAT}, 4.1V_{BAT}

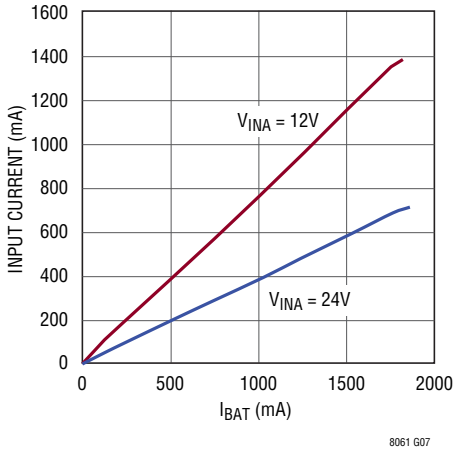


Input Current vs I_{BAT}, 4.2V_{BAT}

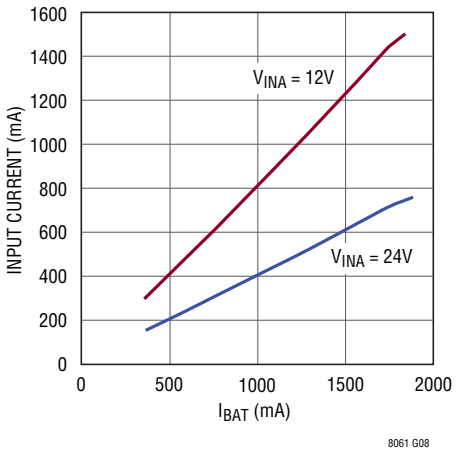


TYPICAL PERFORMANCE CHARACTERISTICS

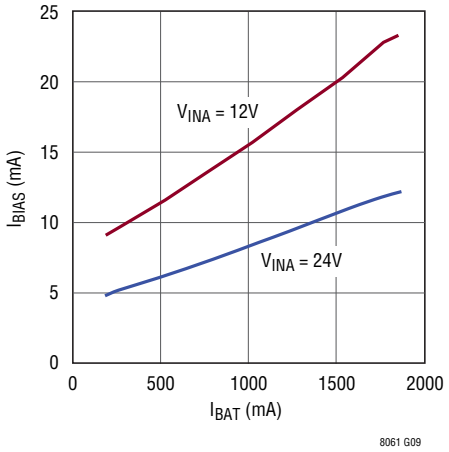
Input Current vs I_{BAT}, 8.2V_{BAT}



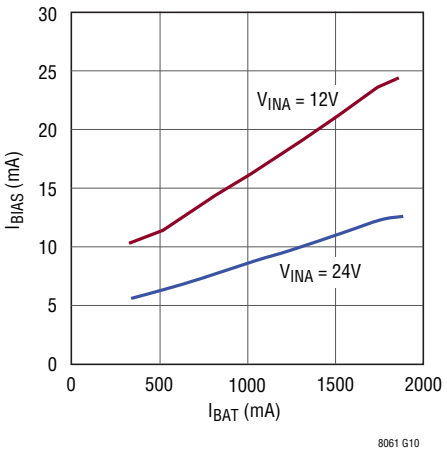
Input Current vs I_{BAT}, 8.4V_{BAT}



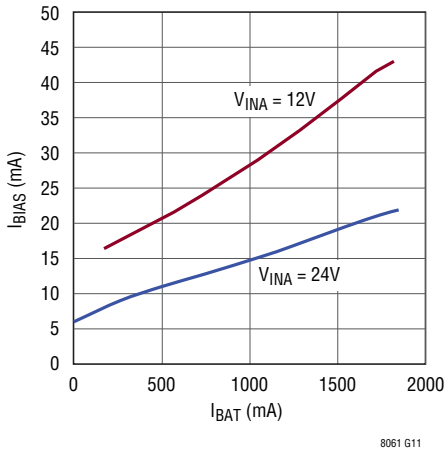
I_{BIAS} vs I_{BAT}, 4.1V_{BAT}



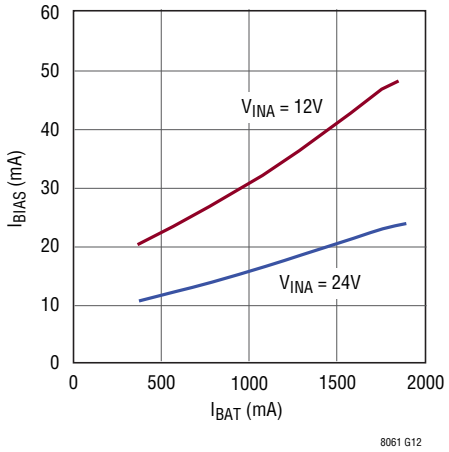
I_{BIAS} vs I_{BAT}, 4.2V_{BAT}



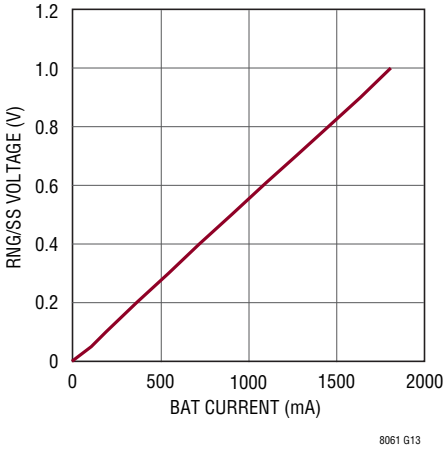
I_{BIAS} vs I_{BAT}, 8.2V_{BAT}



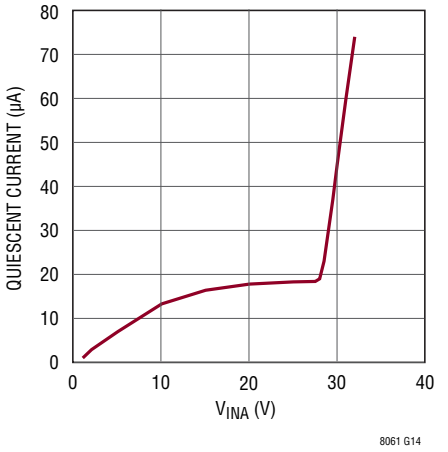
I_{BIAS} vs I_{BAT}, 8.4V_{BAT}



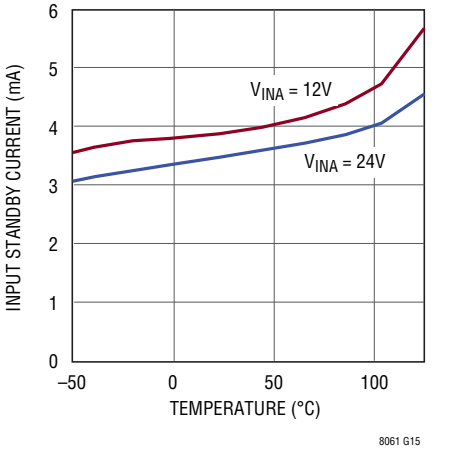
RNG/SS vs Maximum I_{BAT}



Quiescent Current vs V_{INA}, RUN = 0V

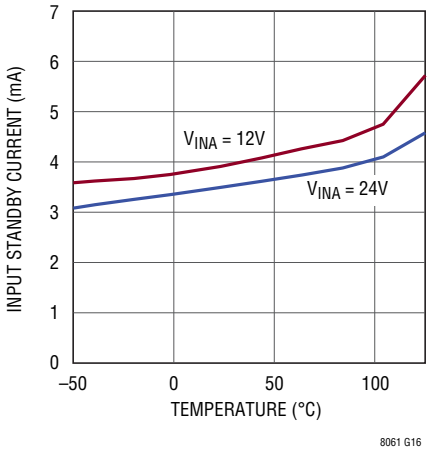


Input Standby Current vs Temperature, 4.1V_{BAT}

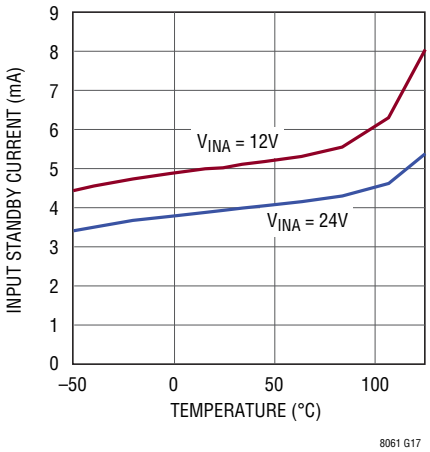


TYPICAL PERFORMANCE CHARACTERISTICS

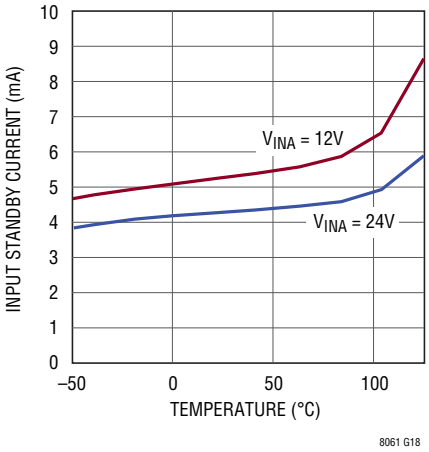
Input Standby Current vs Temperature, 4.2V_{BAT}



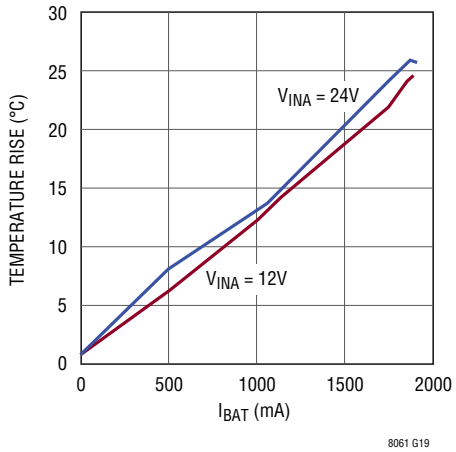
Input Standby Current vs Temperature, 8.2V_{BAT}



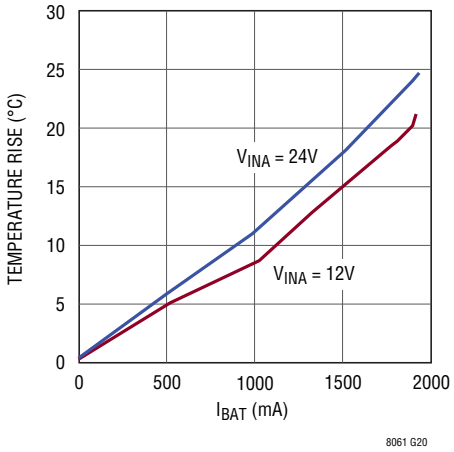
Input Standby Current vs Temperature, 8.4V_{BAT}



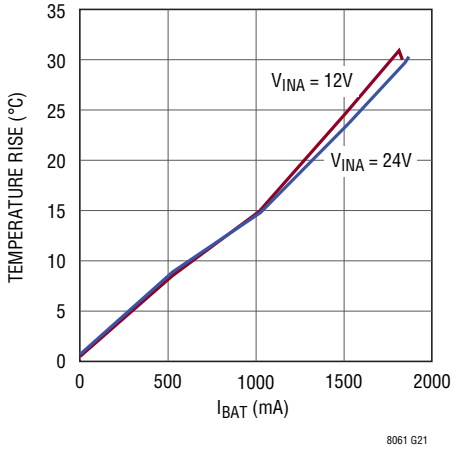
Temperature Rise vs I_{BAT}, 4.1V_{BAT}



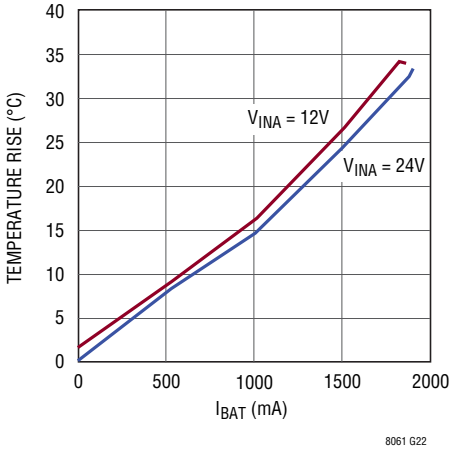
Temperature Rise vs I_{BAT}, 4.2V_{BAT}



Temperature Rise vs I_{BAT}, 8.2V_{BAT}



Temperature Rise vs I_{BAT}, 8.4V_{BAT}



PIN FUNCTIONS

GND (Bank 1): Power and Signal Ground Return.

BAT (Bank 2): Battery Charge Current Output Bus. The charge function operates to achieve the final float voltage at this pin. The auto-restart feature initiates a new charge cycle when the voltage at the BAT pin falls 2.5% below the float voltage. Once the charge cycle is terminated, the input bias current of the BAT pin is reduced to minimize battery discharge while the charger remains connected. In most applications, connect BIAS to BAT.

V_{INA} (Bank 3): Anode of Input Reverse Protection Schottky Diode. Connect the input power here if input voltage protection is desired.

V_{INC}/CLP (Bank 4): This pad bank connects to the cathode of the input reverse protection diode. In addition, system current levels can be monitored by connecting a sense resistor from this pin to the V_{IN} pin. Additional system load is drawn from the V_{IN} pin connection, and maximum system load is achieved when $V_{VINC/CLP} - V_{VIN} = 50mV$. The LTM8061 servos the charge current required to maintain programmed maximum system current. If this function is not desired, connect the V_{INC}/CLP pin to the V_{IN} pin (see the Applications Information section). Do not raise this pin above V_{IN} + 0.5V.

V_{IN} (Bank 5): Charger Input Supply. Apply C_{IN} here. Connect the input power here if no input power rectification is required.

BIAS (Pin G7): The BIAS pin connects to the internal power bus. Connect to a power source greater than 2.5V and less than 10V. In most applications, connect BIAS to BAT.

$\overline{CHRG}$ (Pin K7): Open-Collector Charger Status Output. Typically pulled up through a resistor to a reference voltage. This status pin can be pulled up to voltages as high as V_{IN} and can sink currents up to 10mA. During a battery charge cycle, $\overline{CHRG}$ is pulled low. When the charge cycle terminates, the $\overline{CHRG}$ pin becomes high impedance. If the internal timer is used for termination, the pin stays low during the charge cycle until the charge current drops below a C/10 rate even though the charger will continue to top off the battery until the end-of-charge timer terminates the charge cycle. A temperature fault also causes this pin to be pulled low (see the Applications Information section). If RUN is low, or the LTM8061 is otherwise powered down, the state of the $\overline{CHRG}$ pin is invalid.

NTC (Pin H6): Battery Temperature Monitor Pin. This pin is the input to the NTC (negative temperature coefficient) thermistor temperature monitoring circuit. This function is enabled by connecting a 10kΩ, β = 3380 NTC thermistor from the NTC pin to ground. The pin sources 50µA, and monitors the voltage across the 10kΩ thermistor. When the voltage on this pin is above 1.36V (T < 0°C) or below 0.29V (T > 40°C), charging is disabled and the $\overline{CHRG}$ and $\overline{FAULT}$ pins are both pulled low. If internal timer termination is being used, the timer is paused, suspending the charge cycle. Charging resumes when the voltage on NTC returns to within the 0.29V to 1.36V active region. There is approximately 5°C of temperature hysteresis associated with each of the temperature thresholds. The temperature monitoring function remains enabled while thermistor resistance to ground is less than 250kΩ. If this function is not desired, leave the NTC pin unconnected.

PIN FUNCTIONS

RNG/SS (Pin H7): Charge Current Programming/Soft-Start Pin. This pin allows the maximum charge current to be reduced from the default 2A level, and can be used to employ a soft-start function. This pin has an effective range from 0V to 1V, with the maximum BAT charge current determined by I_{BAT}.

50µA is sourced from this pin, so the maximum charge current can be programmed by connecting a resistor ($R_{RNG/SS}$) from RNG/SS to ground, and the maximum battery charge current is:

$$I_{BAT} = 2A \bullet V_{RNG/SS}$$

$$I_{BAT} = 2A \bullet 50\mu A \bullet R_{RNG/SS}$$

where $R_{RNG/SS}$ is less than or equal to 20kΩ. With the RNG/SS pin left open, the charge current is 2A.

Soft-start functionality can be implemented by connecting a capacitor ($C_{RNG/SS}$) from RNG/SS to ground, such that the time required to charge the capacitor to 1V (full charge current) is the desired soft-start interval (t_{SS}). With no $R_{RNG/SS}$ resistor applied, this capacitor value follows the relation:

$$C_{RNG/SS} = 50\mu A \bullet t_{SS}$$

The RNG/SS pin is pulled low during fault conditions, allowing graceful recovery from faults should soft-start functionality be implemented. Both the soft-start capacitor and the programming resistor can be implemented in parallel. All C/10 monitoring functions are disabled while $V_{RNG/SS}$ is below 0.1V to accommodate long soft-start intervals.

RNG/SS voltage can also be manipulated using an active device, employing a pull-down transistor to disable charge current or to dynamically servo maximum charge current. Manipulation of the RNG/SS pin with active devices that have low impedance pull-up capability is not allowed (see the Applications Information section).

$\overline{\text{FAULT}}$ (Pin J7): Open-Collector Fault Status Output. Typically pulled up through a resistor to a reference voltage. This status pin can be pulled up to voltages as high as V_{IN}, and can sink currents up to 10mA. This pin indicates charge cycle fault conditions during a battery charge cycle. A temperature fault causes this pin to be pulled low. If the internal timer is used for termination, a bad battery fault also causes this pin to be pulled low. If no fault conditions exist, the $\overline{\text{FAULT}}$ pin remains high impedance (see the Applications Information section). If RUN is low, or the LTM8061 is otherwise powered down, the state of the $\overline{\text{FAULT}}$ pin is invalid.

TMR (Pin J6): End-Of-Cycle Timer Programming Pin. If a timer-based charge termination is desired, connect a capacitor from this pin to ground. Full charge end-of cycle time (in hours) is programmed with this capacitor following the equation:

$$t_{EOC} = C_{TIMER} \bullet 4.4 \bullet 10^6$$

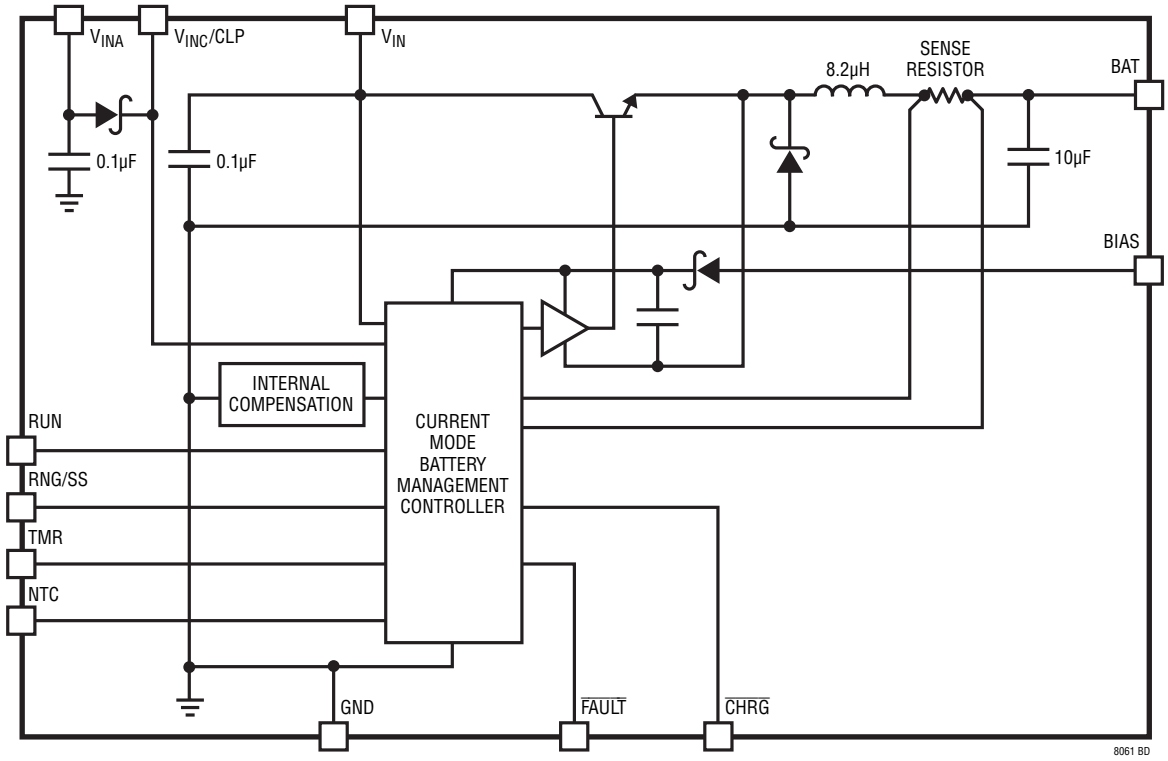
A bad battery fault is generated if the battery does not reach the precondition threshold voltage within one-eighth of t_{EOC}, or:

$$t_{PRE} = C_{TIMER} \bullet 5.5 \bullet 10^5$$

A 0.68µF capacitor is typically used, which generates a timer EOC of three hours, and a precondition limit time of 22.5 minutes. If a timer-based termination is not desired, the timer function is disabled by connecting the TMR pin to ground. With the timer function disabled, charging terminates when the charge current drops below a C/10 rate, or $I_{CHG(MAX)}/10$.

RUN (Pin K6): Precision Threshold Enable Pin. The RUN threshold is 1.20V (rising), with 120mV of input hysteresis. When in shutdown mode, all charging functions are disabled. The precision threshold allows use of the RUN pin to incorporate UVLO functions. If the RUN pin is pulled below 0.4V, the µModule enters a low current shutdown mode where the V_{IN} pin current is reduced to 15µA. Typical RUN pin input bias current is 1µA. If the shutdown function is not desired, connect the pin to the V_{IN} pin.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Overview

The LTM8061 is a complete monolithic, mid-power, Li-Ion battery charger, addressing high input voltage applications with solutions that use a minimum of external components. The product is available in four variants: 4.1V, 4.2V, 8.2V and 8.4V fixed float voltages, each using 1MHz constant-frequency, average current mode step-down architecture. A 2A power Schottky diode is integrated within the µModule for reverse input voltage protection. A wide input range allows the operation to full charge from 6V to 32V for the LTM8061-4.1/LTM8061-4.2 and 11V to 32V for the LTM8061-8.2/LTM8061-8.4 versions. A precision threshold RUN pin allows incorporation of UVLO functionality using a simple resistor divider. The charger can also be put into a low current shutdown mode, in which the input supply bias is reduced to only 15µA.

The LTM8061 incorporates several degrees of charge current control freedom. The maximum charge current is internally set to approximately 2A. A maximum charge current programming pin (RNG/SS) allows the charge current to be reduced from the default 2A level. The LTM8061 also incorporates an input supply current limit control feature (V_{INC}/CLP) that servos the battery charge current to accommodate overall system load requirements.

The LTM8061 automatically enters a battery precondition mode if the sensed battery voltage is very low. In this mode, the charge current is reduced to 300mA. Once the battery voltage climbs above the internally set precondition threshold (2.9V for the LTM8061-4.1/LTM8061-4.2, 5.65V for the LTM8061-8.2, and 5.8V for the LTM8061-8.4), the µModule automatically increases the maximum charge current to the full programmed value.

The LTM8061 can use a charge current based C/10 termination scheme, which ends a charge cycle when the battery charge current falls to one-tenth the programmed charge current. The LTM8061 also contains an internal charge cycle control timer, for timer-based termination. When using the internal timer, the charge cycle can continue beyond the C/10 level to top-off a battery. The charge cycle terminates when the programmed time elapses, typically chosen to be three hours. The $\overline{CHRG}$ status pin continues to signal charging at a C/10 rate, regardless of which termination scheme is used. When the timer-based scheme is used, the device also supports bad battery detection, which triggers a system fault if a battery stays in precondition mode for more than one-eighth of the total programmed charge cycle time.

Once charging terminates and the LTM8061 is not actively charging, the device automatically enters a low current standby mode in which supply bias currents are reduced to 85µA. If the battery voltage drops 2.5% from the full charge float voltage, the LTM8061 engages an automatic charge cycle restart. The device also automatically restarts a new charge cycle after a bad-battery fault once the failed battery is removed and replaced with another battery.

The LTM8061 contains a battery temperature monitoring circuit. This feature, using a thermistor, monitors battery temperature and will not allow charging to begin, or will suspend charging, and signal a fault condition if the battery temperature is outside a safe charging range. The LTM8061 contains two digital open-collector outputs, which provide charger status and signal fault conditions. These binary coded pins signal battery charging, standby or shutdown modes, battery temperature faults and bad battery faults. For reference, C/10 and TMR based charging cycles are shown in Figures 1 and 2.

APPLICATIONS INFORMATION

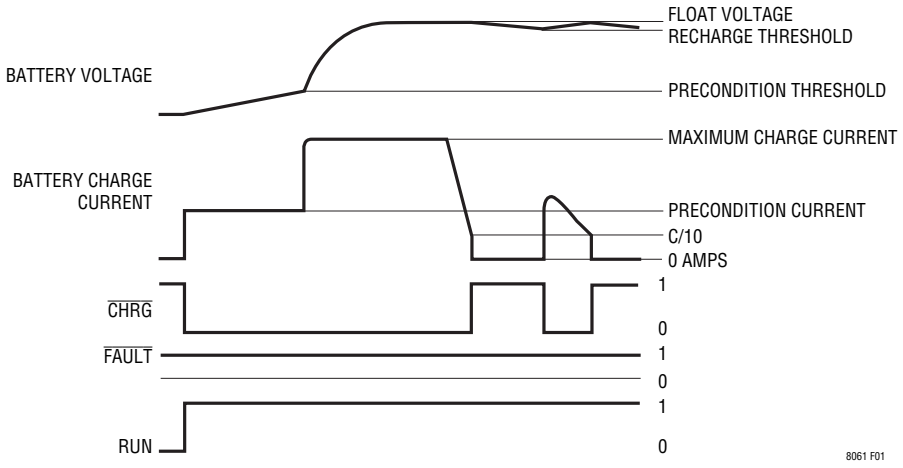


Figure 1. Typical C/10 Terminated Charge Cycle (TMR Grounded, Time Not to Scale)

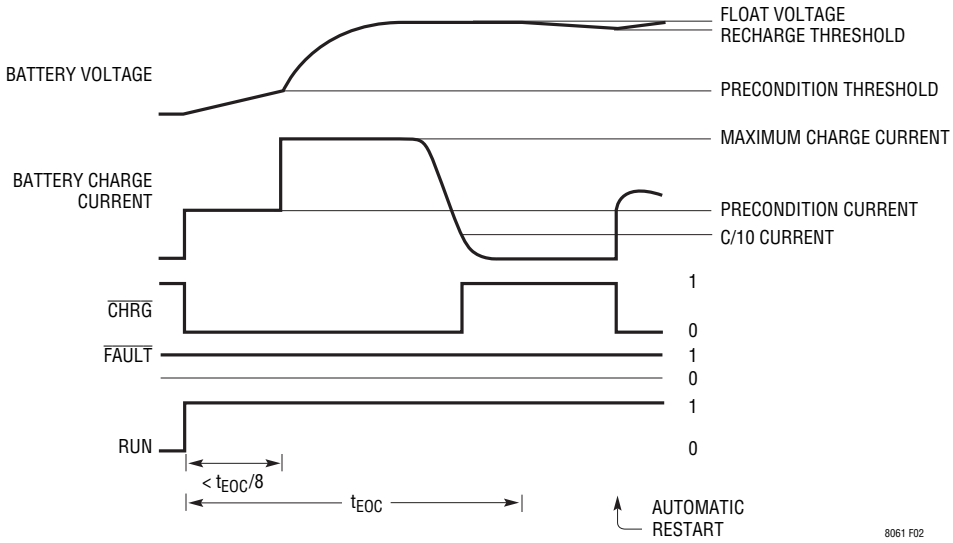


Figure 2. Typical EOC (Timer-Based) Terminated Charge Cycle (Capacitor Connected to TMR, Time Not to Scale)

APPLICATIONS INFORMATION

V_{IN} Input Supply

The LTM8061 is biased directly from the charger input supply through the V_{IN} pin. This pin carries large switched currents, so a high quality, low ESR decoupling capacitor is recommended to minimize voltage glitches on V_{IN}. A 4.7µF capacitor is typically adequate for most charger applications.

Reverse Protection Diode

The LTM8061 integrates a high voltage power Schottky diode to provide input reverse voltage protection. The anode of this diode is connected to V_{INA}, and the cathode is connected to $V_{INC/CLP}$. There is a small amount of capacitance at each end; please see the Block Diagram.

BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 2.9V and no more than the absolute maximum rating of 10V. In most applications, connect BIAS to BAT.

When charging a 2-cell battery using a relatively high input voltage, the LTM8061 power dissipation can be reduced by connecting BIAS to a 3.3V source.

BAT Decoupling Capacitance

In many applications, the internal BAT capacitance of the LTM8061 is sufficient for proper operation. There are cases, however, where it may be necessary to add capacitance or otherwise modify the output impedance of the LTM8061. Case 1: the µModule charger is physically located far from the battery and the added line impedance may interfere with the control loop. Case 2: the battery ESR is very small or very large; the LTM8061 controller is designed for a wide range, but some battery packs have an ESR outside of this range. Case 3: there is no battery at all. As the charger is designed to work with the ESR of the battery, the output may oscillate if no battery is present.

The optimum ESR is about 100mΩ, but ESR values both higher and lower will work. Table 1 shows a sample of parts verified by Linear Technology:

Table 1. Recommended BAT Capacitors

PART NUMBER	DESCRIPTION	MANUFACTURER
16TQC22M	22µF, 16V, POSCAP	Sanyo
35SVPD18M	18µF, 35V, OS-CON	Sanyo
TPSD226M025R0100	22µF, 25V Tantalum	AVX
T495D226K025AS	22µF, 25V, Tantalum	Kemet
TPSC686M006R0150	68µF, 6V, Tantalum	AVX
TPSB476M006R0250	47µF, 6V, Tantalum	AVX
APXE100ARA680ME61G	68µF, 10V Aluminum	Nippon Chemicon
APS-150ELL680MHB5S	68µF, 25V Aluminum	Nippon Chemicon

If system constraints preclude the use of electrolytic capacitors, a series R-C network may be used. Use a ceramic capacitor of at least 22µF and an equivalent resistance of 100mΩ.

CLP: Input Current Limit

The LTM8061 contains a PowerPath™ control feature to support multiple load systems. The charger adjusts charge current in response to a system load if input supply current exceeds the programmed maximum value. Maximum input supply current is set by connecting a sense resistor (R_{CLP}) as shown in Figure 3. The LTM8061 begins to limit the charge current when the voltage across the sense resistor is 50mV. The maximum input current is defined by:

$$R_{CLP} = 0.05/(\text{Max Input Current})$$

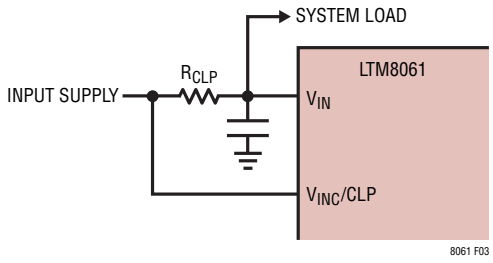


Figure 3. R_{CLP} Sets the Input Supply Current Limit

APPLICATIONS INFORMATION

A 1.5A system limit, for example, would use a 33mΩ sense resistor. Figure 4 gives an example of the system current for the situation where the input current happens to be 1A, and then gets reduced as the additional system load increases beyond 0.5A. The LTM8061 integrates the CLP signal internally, so average current limiting is performed in most cases without the need for external filter elements.

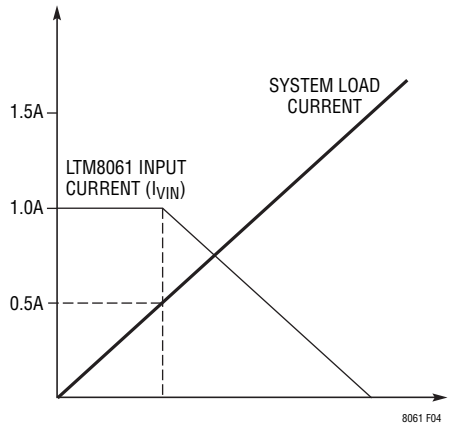


Figure 4. LTM8061 Input Current vs System Load Current with 1.5A Input Current Limit

RNG/SS: Dynamic Charge Current Adjust

The LTM8061 gives the user the capability to reduce the maximum charge current dynamically through the RNG/SS pin. The maximum charge current of the LTM8061 is 2A and the control voltage range on the RNG/SS pin is 1V, so the maximum charge current can be expressed as:

$$I_{BAT} = 2A \bullet V_{RNG/SS}$$

where I_{BAT} is the maximum charge current and $V_{RNG/SS}$ is between 0V to 1V. Voltages higher than 1V have no effect on the maximum charge current.

The LTM8061 sources 50µA from the RNG/SS pin, such that a current control voltage can be set by simply connecting an appropriately valued resistor to ground, following the equation:

$$R_{RNG/SS} = V_{RNG/SS}/50\mu A$$

For example, to reduce the maximum charge current to 50% of the original value, set RNG/SS to 0.5V. The necessary resistor value is:

$$R_{RNG/SS} = 0.5V/50\mu A = 10k\Omega$$

This feature could be used, for example, to switch in a reduced charge current level. Applying an active voltage can also be used to control the maximum charge current but only if the voltage source can sink current. Figures 5 and 6 give two examples of circuits that control the charging current by sinking current. Active circuits that source current cannot be used to drive the RNG/SS pin. Care must be taken not to exceed the 2.5V absolute maximum voltage on the pin.

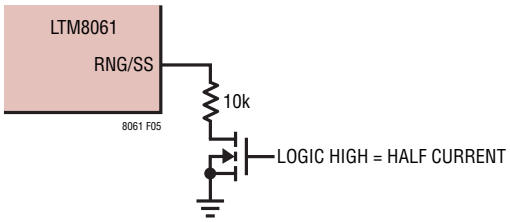


Figure 5. Using the RNG/SS Pin for Digital Control of Maximum Charge Current

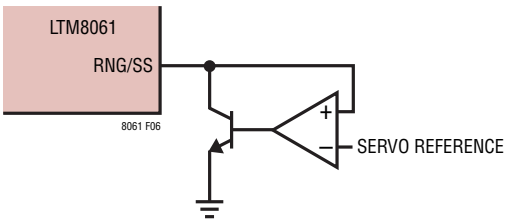


Figure 6. Driving the RNG/SS Pin with a Current-Sink Active Servo Amplifier

APPLICATIONS INFORMATION

RNG/SS: Soft-Start

Soft-start functionality is also supported by the RNG/SS pin. 50µA is sourced from the RNG/SS pin, so connecting a capacitor from the RNG/SS pin to ground ($C_{RNG/SS}$ in Figure 7) creates a linear voltage ramp. The maximum charge current follows this voltage. Thus, the charge current increases from zero to the fully programmed value as the capacitor charges from 0V to 1V. The value of $C_{RNG/SS}$ is calculated based on the desired time to full current (t_{SS}) following the equation:

$$C_{RNG/SS} = 50\mu A \bullet t_{SS}$$

The RNG/SS pin is pulled to ground internally when charging terminates so each new charge cycle begins with a soft-start cycle. RNG/SS is also pulled to ground during bad-battery and NTC fault conditions, producing a graceful recovery from a fault.

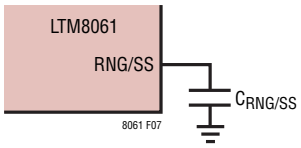


Figure 7. Using the RNG/SS Pin for Soft-Start

Status Pins

The LTM8061 reports charger status through two open-collector outputs, the $\overline{CHRG}$ and $\overline{FAULT}$ pins. These pins can accept voltages as high as V_{IN}, and can sink up to 10mA when enabled. The $\overline{CHRG}$ pin indicates that the charger is delivering current at greater than a C/10 rate, or one-tenth of the programmed charge current. The $\overline{FAULT}$ pin signals bad-battery and NTC faults. These pins are binary coded as shown in Table 2:

Table 2. Status Pin State

$\overline{CHRG}$	$\overline{FAULT}$	STATUS
High	High	Standby, Shutdown Mode, or Charging at Less than C/10
High	Low	Bad-Battery Fault (Precondition Timeout/ EOC Failure)
Low	High	Normal Charging at C/10 or Greater
Low	Low	NTC Fault (Pause)

If the battery is removed from an LTM8061 charger that is configured for C/10 termination, a low amplitude sawtooth waveform appears at the charger output, due to cycling between termination and recharge events. This cycling results in pulsing at the $\overline{CHRG}$ output. An LED connected to this pin will exhibit a blinking pattern, indicating to the user that a battery is not present. The frequency of this blinking pattern is dependent on the output capacitance.

C/10 Termination

The LTM8061 supports a low current based termination scheme, where a battery charge cycle terminates when the charge current falls below one-tenth the programmed charge current, or about 200mA. This termination mode is engaged by shorting the TMR pin to ground. When C/10 termination is used, an LTM8061 charger sources battery charge current as long as the average current level remains above the C/10 threshold. As the full-charge float voltage is achieved, the charge current falls until the C/10 threshold is reached, at which time the charger terminates and the LTM8061 enters standby mode. The $\overline{CHRG}$ status is high impedance when the charger is sourcing less than C/10. There is no provision for bad-battery detection if C/10 termination is used.

Timer Termination

The LTM8061 supports a timer-based termination scheme, where a battery charge cycle terminates after a specific amount of time elapses. Timer termination is enabled by connecting a capacitor (C_{TIMER}) from the TMR pin to GND. The timer cycle time span (t_{EOC}) is determined by C_{TIMER} in the equation:

$$C_{TIMER} = t_{EOC} \bullet 2.27 \bullet 10^{-7}\ (\text{Hours})$$

When charging at a 1C rate, t_{EOC} is commonly set to three hours, which requires a 0.68µF capacitor.

The $\overline{CHRG}$ status pin continues to signal charging, regardless of which termination scheme is used. When timer termination is used, the $\overline{CHRG}$ status pin is pulled low during a charge cycle until the charge current falls below the C/10 threshold. The charger continues to top off the battery until timer EOC, when the LTM8061 terminates the charge cycle and enters standby mode.

APPLICATIONS INFORMATION

Termination at the end of the timer cycle only occurs if the charge cycle was successful. A successful charge cycle occurs when the battery is charged to within 2.5% of the full-charge float voltage. If a charge cycle is not successful at EOC, the timer cycle resets and charging continues for another full timer cycle. When V_{BAT} drops 2.5% from the full-charge float voltage, whether by battery loading or replacement of the battery, the charger automatically resets and starts charging.

Preconditioning and Bad-Battery Fault

The LTM8061 has a precondition mode, in which charge current is limited to 15% of the maximum charge current, roughly 300mA. Precondition mode is engaged if the voltage on the BAT pin is below the precondition threshold, or approximately 70% of the float voltage. Once the BAT voltage rises above the precondition threshold, normal full-current charging can commence. The LTM8061 incorporates 90mV hysteresis to avoid spurious mode transitions.

Bad-battery detection is engaged when using timer termination. This fault detection feature is designed to identify failed cells. A bad-battery fault is triggered when the voltage on BAT remains below the precondition threshold for greater than one-eighth of a full timer cycle (one-eighth EOC). A bad-battery fault is also triggered if a normally charging battery re-enters precondition mode after one-eighth EOC.

When a bad-battery fault is triggered, the charge cycle is suspended, and the $\overline{CHRG}$ status pin becomes high impedance. The $\overline{FAULT}$ pin is pulled low to signal that a fault has been detected. The RNG/SS pin is also pulled low during this fault to accommodate a graceful restart in the event that a soft-start function is incorporated (see the RNG/SS: Soft-Start section).

Cycling the charger's power or shutdown function initiates a new charge cycle, but the LTM8061 charger does not require a manual reset. Once a bad-battery fault is detected, a new timer charge cycle initiates if the BAT pin exceeds the precondition threshold voltage. During a bad-battery fault, a small current is sourced from the charger; removing the failed battery allows the charger output voltage to rise above the preconditioning threshold voltage and initiate a charge cycle reset. A new charge cycle is started by connecting another battery to the charger output.

Battery Temperature Fault: NTC

The LTM8061 can accommodate battery temperature monitoring by using an NTC (negative temperature coefficient) thermistor close to the battery pack. The temperature monitoring function is enabled by connecting a 10kΩ, β = 3380 NTC thermistor from the NTC pin to ground. If the NTC function is not desired, leave the pin unconnected. The NTC pin sources 50µA, and monitors the voltage dropped across the 10kΩ thermistor. When the voltage on this pin is above 1.36V (0°C) or below 0.29V (40°C), the battery temperature is out of range, and the LTM8061 triggers an NTC fault. The NTC fault condition remains until the voltage on the NTC pin corresponds to a temperature within the 0°C to 40°C range. Both hot and cold thresholds incorporate 20% hysteresis, which equates to about 5°C. If higher operational charging temperatures are desired, the temperature range can be expanded by adding series resistance to the 10k NTC resistor. Adding a 909Ω resistor will increase the effective temperature threshold to 45°C, for example.

During an NTC fault, charging is halted and both status pins are pulled low. If timer termination is enabled, the timer count is suspended and held until the fault condition is cleared. The RNG/SS pin is also pulled low during this fault to accommodate a graceful restart in the event that a soft-start function is being incorporated (see the RNG/SS: Soft-Start section).

Thermal Foldback

The LTM8061 contains a thermal foldback protection feature that reduces charge current as the internal temperature approaches 125°C. In most cases, internal temperatures servo such that any overtemperature conditions are relieved with only slight reductions in maximum charge current. In some cases, the thermal foldback protection feature can reduce charge currents below the C/10 threshold. In applications that use C/10 termination (TMR = 0V), the LTM8061 will suspend charging and enter standby mode until the overtemperature condition is relieved.

PCB Layout

APPLICATIONS INFORMATION

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of LTM8061 integration. The LTM8061 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 8 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

1. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8061.
2. If used, place the C_{BAT} capacitor as close as possible to the BAT and GND connection of the LTM8061.
3. Place the C_{IN} and C_{BAT} (if used) capacitors such that their ground current flows directly adjacent or underneath the LTM8061.
4. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8061.
5. For good heat sinking, use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 8. The LTM8061 can benefit from the heat-sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8061. However, these capacitors can cause problems if the LTM8061 is plugged into a live input supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8061 can ring to more than twice the nominal

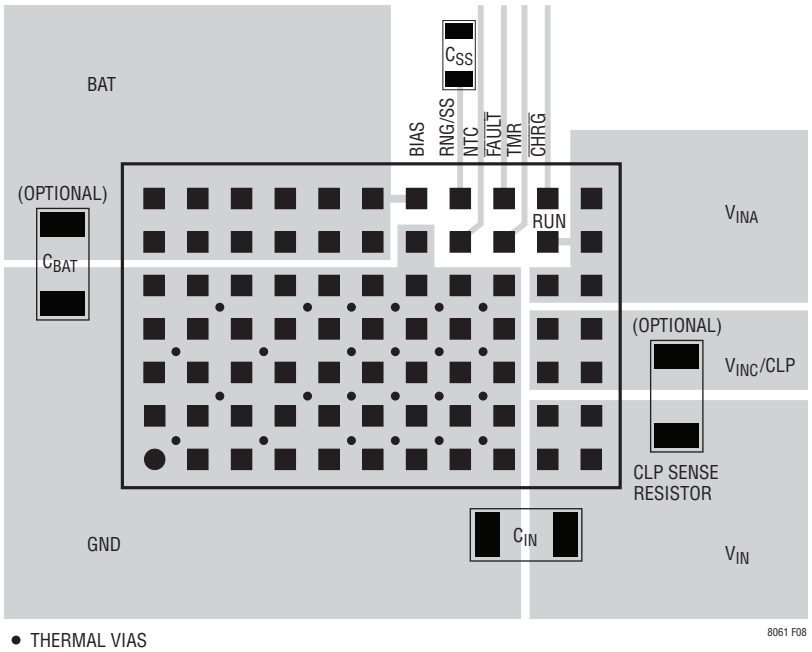


Figure 8. Layout Showing Suggested External Components, Power Planes and Thermal Vias

APPLICATIONS INFORMATION

input voltage, possibly exceeding the LTM8061's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8061 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is physically large.

Thermal Considerations

The temperature rise curves given in the Typical Performance Characteristics section gives the thermal performance of the LTM8061. These curves were generated by the LTM8061 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The junction to air and junction to board thermal resistances given in the Pin Configuration diagram may also be used to estimate the LTM8061 internal temperature. These thermal coefficients are determined for maximum output power per JESD 51-9, "JEDEC Standard, Test Boards for Area Array Surface Mount Package Thermal Measurements" through analysis and physical correlation. Bear in mind that the actual thermal resistance of the LTM8061 to the printed circuit board depends upon the design of the circuit board.

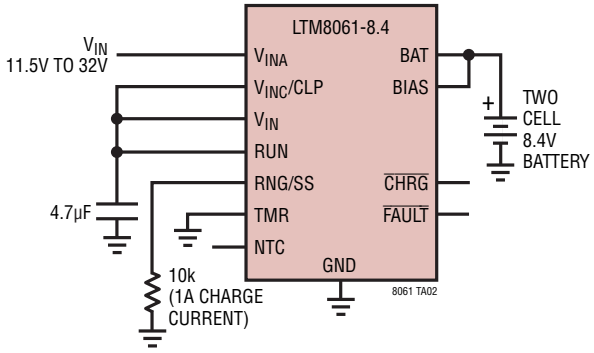
The internal temperature of the LTM8061 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8061. The bulk of the heat flow out of the LTM8061 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

The LTM8061 is equipped with a thermal foldback that reduces the charge current as the internal temperature approaches 125°C. This does not mean that it is impossible to exceed the 125°C maximum internal temperature rating. The ambient operating condition and other factors may result in high internal temperatures.

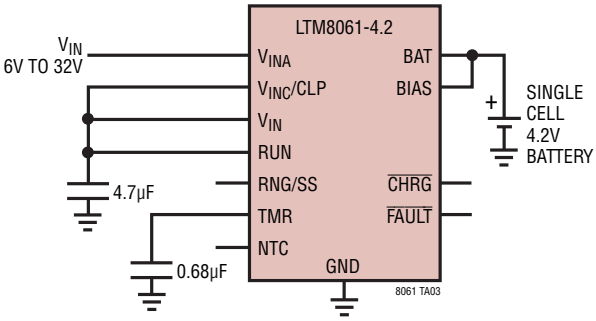
Finally, be aware that at high ambient temperatures the internal Schottky diode will have significant leakage current increasing the quiescent current of the LTM8061.

TYPICAL APPLICATIONS

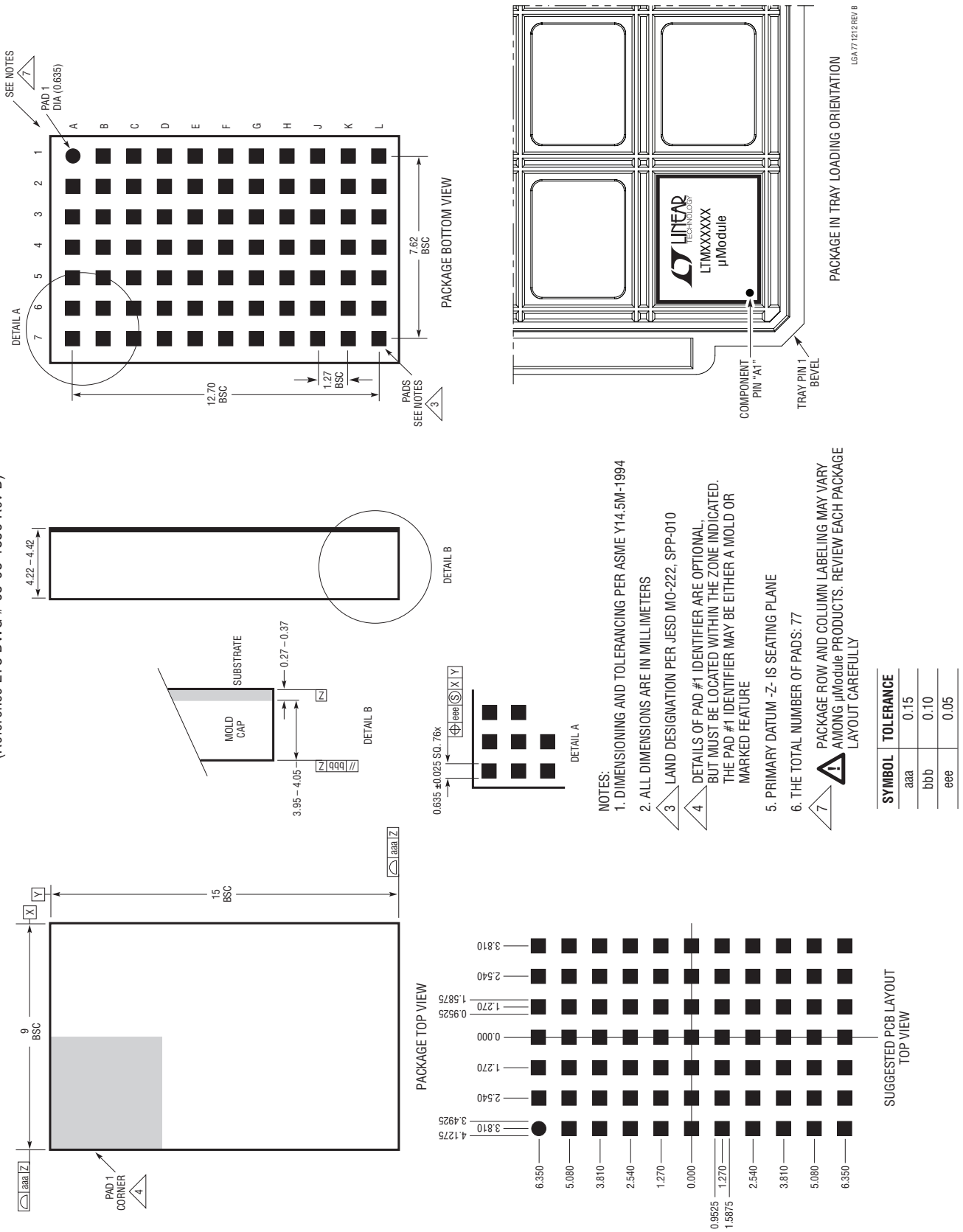
Two Cell 1A Li-Ion Battery Charger with C/10 Termination and Reverse Input Protection



Single Cell 2A Li-Ion Battery Charger with 3 Hour Timer Termination and Reverse Input Protection



PACKAGE DESCRIPTION



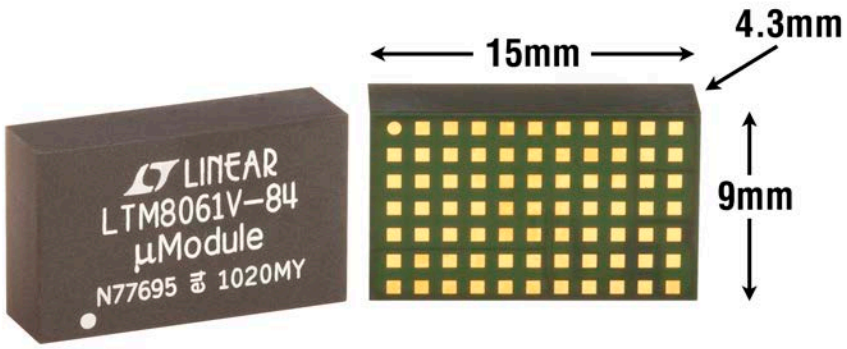
PACKAGE DESCRIPTION

Table 3. Pin Assignment Table (Arranged by Pin Number)

PIN NUMBER		PIN NUMBER		PIN NUMBER		PIN NUMBER		PIN NUMBER		PIN NUMBER	
A1	GND	B1	GND	C1	GND	D1	GND	E1	GND	F1	GND
A2	GND	B2	GND	C2	GND	D2	GND	E2	GND	F2	GND
A3	GND	B3	GND	C3	GND	D3	GND	E3	GND	F3	GND
A4	GND	B4	GND	C4	GND	D4	GND	E4	GND	F4	GND
A5	GND	B5	GND	C5	GND	D5	GND	E5	GND	F5	GND
A6	BAT	B6	BAT	C6	BAT	D6	BAT	E6	BAT	F6	BAT
A7	BAT	B7	BAT	C7	BAT	D7	BAT	E7	BAT	F7	BAT

PIN NUMBER		PIN NUMBER		PIN NUMBER		PIN NUMBER		PIN NUMBER	
G1	GND	H1	GND	J1	GND	K1	V_{IN}	L1	V_{IN}
G2	GND	H2	GND	J2	GND	K2	V_{IN}	L2	V_{IN}
G3	GND	H3	GND	J3	GND	K3	V_{INC}/CLP	L3	V_{INC}/CLP
G4	GND	H4	GND	J4	GND	K4	V_{INC}/CLP	L4	V_{INC}/CLP
G5	GND	H5	GND	J5	GND	K5	V_{INA}	L5	V_{INA}
G6	GND	H6	NTC	J6	TMR	K6	RUN	L6	V_{INA}
G7	BIAS	H7	RNG/SS	J7	$\overline{FAULT}$	K7	$\overline{CHRG}$	L7	V_{INA}

PACKAGE PHOTOGRAPH

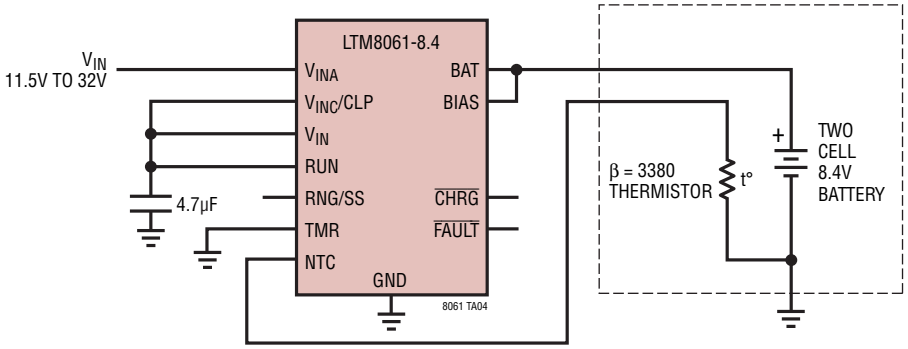


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/14	Input Supply Current; Condition; added Not Switching	3

TYPICAL APPLICATION

Two Cell 2A Li-Ion Battery Charger with Thermistor, C/10 Termination and Reverse Input Protection



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4600	10A DC/DC µModule Regulator	Basic 10A DC/DC µModule, 15mm × 15mm × 2.8mm LGA
LTM4600HVMPV	Military Plastic 10A DC/DC µModule Regulator	–55°C to 125°C Operation, 15mm × 15mm × 2.8mm LGA
LTM4601/ LTM4601A	12A DC/DC µModule Regulator with PLL, Output Tracking/Margining and Remote V_{OUT} Sensing	Synchronizable, PolyPhase® Operation, LTM4601-1 Version Has No Remote Sensing
LTM4602	6A DC/DC µModule Regulator	Pin Compatible with the LTM4600
LTM4603	6A DC/DC µModule Regulator with PLL and Output Tracking/Margining and Remote V_{OUT} Sensing	Synchronizable, PolyPhase Operation, LTM4603-1 Version Has No Remote Sensing, Pin Compatible with the LTM4601
LTM4604	4A Low V_{IN} DC/DC µModule Regulator	2.375V ≤ V_{IN} ≤ 5V, 0.8V ≤ V_{OUT} ≤ 5V, 9mm × 15mm × 2.3mm LGA
LTM4608	8A Low V_{IN} DC/DC µModule Regulator	2.375V ≤ V_{IN} ≤ 5V, 0.8V ≤ V_{OUT} ≤ 5V, 9mm × 15mm × 2.8mm LGA
LTM8020	200mA, 36V DC/DC µModule Regulator	Fixed 450kHz Frequency, 1.25V ≤ V_{OUT} ≤ 5V, 6.25mm × 6.25mm × 2.32mm LGA
LTM8022	1A, 36V DC/DC µModule Regulator	Adjustable Frequency, 0.8V ≤ V_{OUT} ≤ 5V, 9mm × 11.25mm × 2.82mm LGA, Pin Compatible to the LTM8023
LTM8023	2A, 36V DC/DC µModule Regulator	Adjustable Frequency, 0.8V ≤ V_{OUT} ≤ 5V, 9mm × 11.25mm × 2.82mm LGA, Pin Compatible to the LTM8022
LTM8025	3A, 36V DC/DC µModule Regulator	0.8V ≤ V_{OUT} ≤ 24V, 9mm × 15mm × 4.32mm LGA

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LT 0214 REV A • PRINTED IN USA