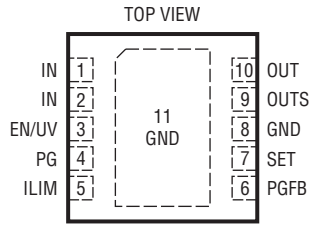
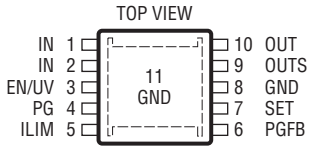
ABSOLUTE MAXIMUM RATINGS (Note 1)

IN Pin Voltage ..... ±22V
EN/UV Pin Voltage ..... ±22V
IN-to-EN/UV Differential ..... ±22V
PG Pin Voltage (Note 10) ..... –0.3V, 22V
ILIM Pin Voltage (Note 10) ..... –0.3V, 1V
PGFB Pin Voltage (Note 10) ..... –0.3V, 22V
SET Pin Voltage (Note 10) ..... –0.3V, 16V
SET Pin Current (Note 7) ..... ±20mA
OUTS Pin Voltage (Note 10) ..... –0.3V, 16V
OUTS Pin Current (Note 7) ..... ±20mA
OUT Pin Voltage (Note 10) ..... –0.3V, 16V
OUT-to-OUTS Differential (Note 14) ..... ±1.2V
IN-to-OUT Differential ..... ±22V
IN-to-OUTS Differential ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Note 9)
E-, I-Grade ..... –40°C to 125°C
H-Grade ..... –40°C to 150°C
MP-Grade ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 Sec)
MSE Package ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 33°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LT3042#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3042EDD#PBF	LT3042EDD#TRPBF	LGSJ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3042IDD#PBF	LT3042IDD#TRPBF	LGSJ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3042HDD#PBF	LT3042HDD#TRPBF	LGSJ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 150°C
LT3042MPDD#PBF	LT3042MPDD#TRPBF	LGSJ	10-Lead (3mm × 3mm) Plastic DFN	–55°C to 150°C
LT3042EMSE#PBF	LT3042EMSE#TRPBF	LTGSH	10-Lead Plastic MSOP	–40°C to 125°C
LT3042IMSE#PBF	LT3042IMSE#TRPBF	LTGSH	10-Lead Plastic MSOP	–40°C to 125°C
LT3042HMSE#PBF	LT3042HMSE#TRPBF	LTGSH	10-Lead Plastic MSOP	–40°C to 150°C
LT3042MPMSE#PBF	LT3042MPMSE#TRPBF	LTGSH	10-Lead Plastic MSOP	–55°C to 150°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult ADI Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum IN Pin Voltage (Note 2)	I_{LOAD} = 200mA, V_{IN} UVLO Rising	●		1.78	2	V
	V_{IN} UVLO Hysteresis			75		mV
SET Pin Current (I_{SET})	V_{IN} = 2V, I_{LOAD} = 1mA, V_{OUT} = 1.3V		99	100	101	µA
	2V < V_{IN} < 20V, 0V < V_{OUT} < 15V, 1mA < I_{LOAD} < 200mA (Note 3)	●	98	100	102	µA
Fast Start-Up Set Pin Current	V_{PGFB} = 289mV, V_{IN} = 2.8V, V_{SET} = 1.3V			2		mA
Output Offset Voltage V_{OS} (V_{OUT} – V_{SET}) (Note 4)	V_{IN} = 2V, I_{LOAD} = 1mA, V_{OUT} = 1.3V		–1		1	mV
	2V < V_{IN} < 20V, 0V < V_{OUT} < 15V, 1mA < I_{LOAD} < 200mA (Note 3)	●	–2		2	mV
Line Regulation: ΔI_{SET}	V_{IN} = 2V to 20V, I_{LOAD} = 1mA, V_{OUT} = 1.3V	●		0.5	±2	nA/V
Line Regulation: ΔV_{OS}	V_{IN} = 2V to 20V, I_{LOAD} = 1mA, V_{OUT} = 1.3V (Note 4)	●		0.5	±3	µV/V
Load Regulation: ΔI_{SET}	I_{LOAD} = 1mA to 200mA, V_{IN} = 2V, V_{OUT} = 1.3V			3		nA
Load Regulation: ΔV_{OS}	I_{LOAD} = 1mA to 200mA, V_{IN} = 2V, V_{OUT} = 1.3V (Note 4)	●		0.1	0.5	mV
Change in I_{SET} with V_{SET}	V_{SET} = 1.3V to 15V, V_{IN} = 20V, I_{LOAD} = 1mA	●		30	400	nA
Change in V_{OS} with V_{SET}	V_{SET} = 1.3V to 15V, V_{IN} = 20V, I_{LOAD} = 1mA (Note 4)	●		0.03	0.6	mV
Change in I_{SET} with V_{SET}	V_{SET} = 0V to 1.3V, V_{IN} = 20V, I_{LOAD} = 1mA	●		150	600	nA
Change in V_{OS} with V_{SET}	V_{SET} = 0V to 1.3V, V_{IN} = 20V, I_{LOAD} = 1mA (Note 4)	●		0.3	2	mV
Dropout Voltage	I_{LOAD} = 1mA, 50mA			220	270	mV
		●			300	mV
	I_{LOAD} = 150mA (Note 5)			270		mV
	I_{LOAD} = 200mA (Note 5)			350		mV
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$ (Note 6)	I_{LOAD} = 10µA			1.9		mA
	I_{LOAD} = 1mA	●		2	3.5	mA
	I_{LOAD} = 50mA	●		3.2	5	mA
	I_{LOAD} = 100mA	●		4.5	7	mA
	I_{LOAD} = 200mA	●		7.6	13	mA
Output Noise Spectral Density (Notes 4, 8)	I_{LOAD} = 200mA, Frequency = 10Hz, C_{OUT} = 4.7µF, C_{SET} = 0.47µF, V_{OUT} = 3.3V			300		nV/√Hz
	I_{LOAD} = 200mA, Frequency = 10Hz, C_{OUT} = 4.7µF, C_{SET} = 4.7µF, 1.3V ≤ V_{OUT} ≤ 15V			60		nV/√Hz
	I_{LOAD} = 200mA, Frequency = 10kHz, C_{OUT} = 4.7µF, C_{SET} = 0.47µF, 1.3V ≤ V_{OUT} ≤ 15V			2		nV/√Hz
	I_{LOAD} = 200mA, Frequency = 10kHz, C_{OUT} = 4.7µF, C_{SET} = 0.47µF, 0V ≤ V_{OUT} < 1.3V			5		nV/√Hz
Output RMS Noise (Notes 4, 8)	I_{LOAD} = 200mA, BW = 10Hz to 100kHz, C_{OUT} = 4.7µF, C_{SET} = 0.47µF, V_{OUT} = 3.3V			1.9		μV_{RMS}
	I_{LOAD} = 200mA, BW = 10Hz to 100kHz, C_{OUT} = 4.7µF, C_{SET} = 4.7µF, 1.3V ≤ V_{OUT} ≤ 15V			0.8		μV_{RMS}
	I_{LOAD} = 200mA, BW = 10Hz to 100kHz, C_{OUT} = 4.7µF, C_{SET} = 4.7µF, 0V ≤ V_{OUT} < 1.3V			1.6		μV_{RMS}
Reference Current RMS Output Noise (Notes 4, 8)	BW = 10Hz to 100kHz			6		nA_{RMS}
Ripple Rejection 1.3V ≤ V_{OUT} ≤ 15V V_{IN} – V_{OUT} = 2V (Avg) (Notes 4, 15)	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 4.7µF		95	117		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF			91		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF			78		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF			79		dB
	V_{RIPPLE} = 80mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF			56		dB
Ripple Rejection 0V ≤ V_{OUT} < 1.3V V_{IN} – V_{OUT} = 2V (Avg) (Notes 4, 8)	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF			104		dB
	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF			85		dB
	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF			73		dB
	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF			72		dB
	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF			57		dB
EN/UV Pin Threshold	EN/UV Trip Point Rising (Turn-On), V_{IN} = 2V	●	1.18	1.24	1.32	V
EN/UV Pin Hysteresis	EN/UV Trip Point Hysteresis, V_{IN} = 2V			170		mV
EN/UV Pin Current	$V_{EN/UV}$ = 0V, V_{IN} = 20V	●			±1	µA
	$V_{EN/UV}$ = 1.24V, V_{IN} = 20V			0.2		µA
	$V_{EN/UV}$ = 20V, V_{IN} = 0V	●		8	15	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current in Shutdown ($V_{EN/UV}$ = 0V)	V_{IN} = 6V	 ●		0.3	1 10	µA µA
Internal Current Limit (Note 12)	V_{IN} = 2V, V_{OUT} = 0V V_{IN} = 12V, V_{OUT} = 0V V_{IN} = 20V, V_{OUT} = 0V	● ●	220 130	270 300 180	320 250	mA mA mA
Programmable Current Limit	Programming Scale Factor: 2V< V_{IN} < 20V (Note 11) V_{IN} = 2V, V_{OUT} = 0V, R_{ILIM} = 625Ω V_{IN} = 2V, V_{OUT} = 0V, R_{ILIM} = 2.5kΩ	 ● ●	 180 45	125 200 50	 220 55	mA • kΩ mA mA
PGFB Trip Point	PGFB Trip Point Rising	●	291	300	309	mV
PGFB Hysteresis	PGFB Trip Point Hysteresis			7		mV
PGFB Pin Current	V_{IN} = 2V, V_{PGFB} = 300mV			25		nA
PG Output Low Voltage	I_{PG} = 100µA	●		30	100	mV
PG Leakage Current	V_{PG} = 20V	●			1	µA
Reverse Input Current	V_{IN} = –20V, $V_{EN/UV}$ = 0V, V_{OUT} = 0V, V_{SET} = 0V	●			50	µA
Reverse Output Current	V_{IN} = 0, V_{OUT} = 5V, SET = Open			2	5	µA
Minimum Load Required (Note 13)	V_{OUT} < 1V	●	10			µA
Thermal Shutdown	T_J Rising Hysteresis			162 8		°C °C
Start-Up Time	$V_{OUT(NOM)}$ = 5V, I_{LOAD} = 200mA, C_{SET} = 0.47µF, V_{IN} = 6V, V_{PGFB} = 6V $V_{OUT(NOM)}$ = 5V, I_{LOAD} = 200mA, C_{SET} = 4.7µF, V_{IN} = 6V, V_{PGFB} = 6V $V_{OUT(NOM)}$ = 5V, I_{LOAD} = 200mA, C_{SET} = 4.7µF, V_{IN} = 6V, R_{PG1} = 50kΩ, R_{PG2} = 700kΩ (with Fast Start-Up to 90% of V_{OUT})			55 550 10		ms ms ms
Thermal Regulation	10ms Pulse			–0.01		%/W

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The EN/UV pin threshold must be met to ensure device operation.

Note 3: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current, especially due to the internal current limit foldback which starts to decrease current limit at $V_{IN} – V_{OUT}$ > 12V. If operating at maximum output current, limit the input voltage range. If operating at the maximum input voltage, limit the output current range.

Note 4: OUTS ties directly to OUT.

Note 5: Dropout voltage is the minimum input-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout — which is measured when $V_{IN} = V_{OUT(NOMINAL)}$. For lower output voltages, below 1.5V, dropout voltage is limited by the minimum input voltage specification. **Linear Technology is unable to guarantee maximum dropout voltage specifications at high currents due to production test limitations with Kelvin-sensing the package pins.** Please consult the Typical Performance Characteristics for curves of dropout voltage as a function of output load current and temperature measured in a typical application circuit.

Note 6: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ and a current source load. Therefore, the device is tested while operating in dropout. This is the worst-case GND pin current. GND pin current decreases at higher input voltages. Note that GND pin current does not include SET pin or ILIM pin current but Quiescent current does include them.

Note 7: SET and OUTS pins are clamped using diodes and two 25Ω series resistors. For less than 5ms transients, this clamp circuitry can carry more than the rated current. Refer to Applications Information for more information.

Note 8: Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise as well as the reference current's noise. The output noise then equals the error amplifier noise. Use of a SET pin bypass capacitor also increases start-up time.

Note 9: The LT3042 is tested and specified under pulsed load conditions such that $T_J \approx T_A$. The LT3042E is 100% tested at 25°C and performance is guaranteed from 0°C to 125°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3042I is guaranteed over the full –40°C to 125°C operating temperature range. The LT3042MP is 100% tested and guaranteed over the full –55°C to 150°C operating temperature range. The LT3042H is 100% tested at the 150°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

ELECTRICAL CHARACTERISTICS

Note 10: Parasitic diodes exist internally between the ILIM, PG, PGFB, SET, OUTS, and OUT pins and the GND pin. Do not drive these pins more than 0.3V below the GND pin during a fault condition. These pins must remain at a voltage more positive than GND during normal operation.

Note 11: The current limit programming scale factor is specified while the internal backup current limit is not active. Note that the internal current limit has foldback protection for $V_{IN} – V_{OUT}$ differentials greater than 12V.

Note 12: The internal back-up current limit circuitry incorporates foldback protection that decreases current limit for $V_{IN} – V_{OUT} > 12V$. Some level of output current is provided at all $V_{IN} – V_{OUT}$ differential voltages. Consult the Typical Performance Characteristics graph for current limit vs $V_{IN} – V_{OUT}$.

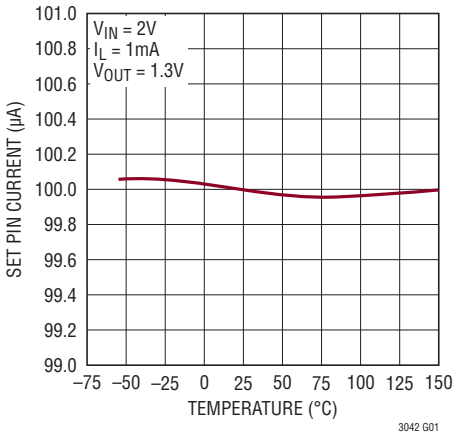
Note 13: For output voltages less than 1V, the LT3042 requires a 10µA minimum load current for stability.

Note 14: Maximum OUT-to-OUTS differential is guaranteed by design.

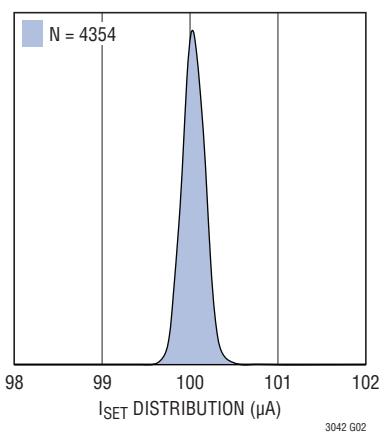
Note 15: The PSRR at 120Hz is guaranteed by design, characterization, and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

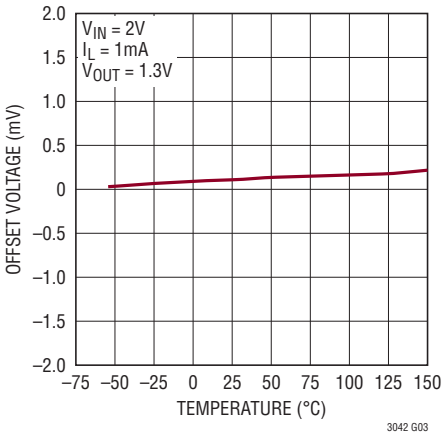
SET Pin Current



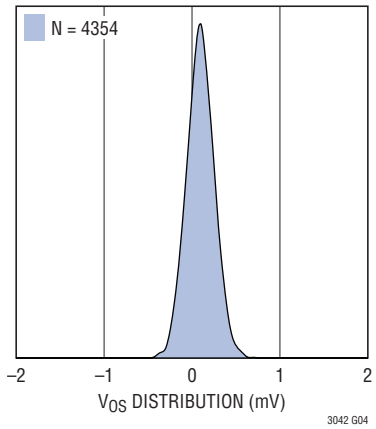
SET Pin Current



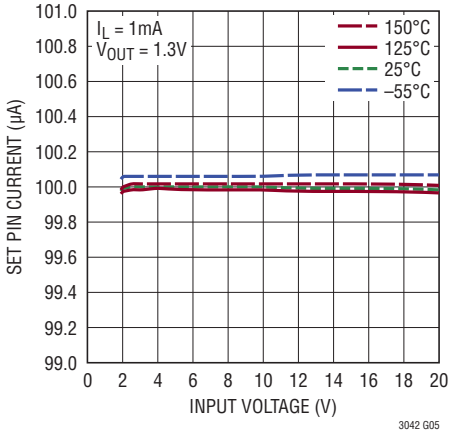
Offset Voltage ($V_{OUT} – V_{SET}$)



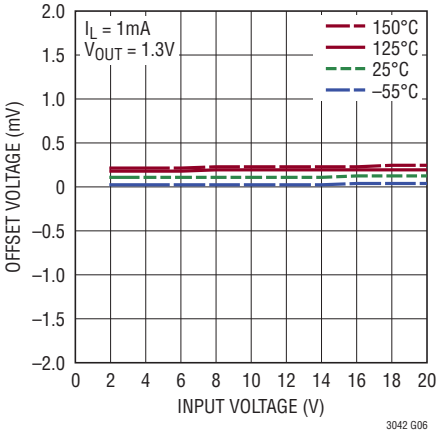
Offset Voltage



SET Pin Current

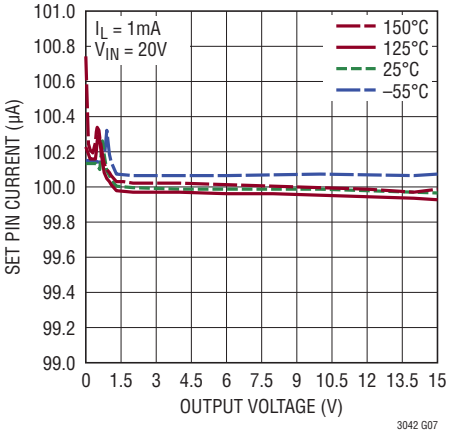


Offset Voltage ($V_{OUT} – V_{SET}$)

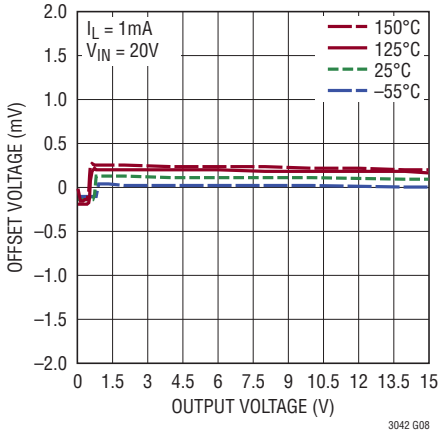


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

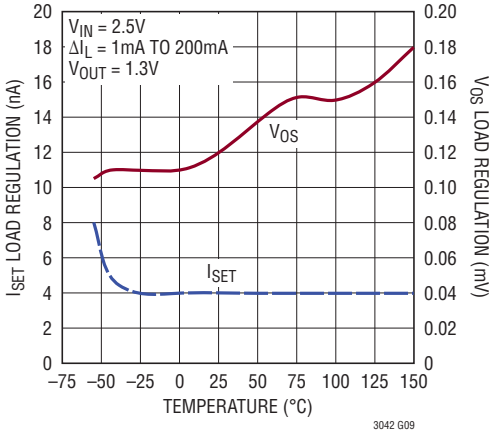
SET Pin Current



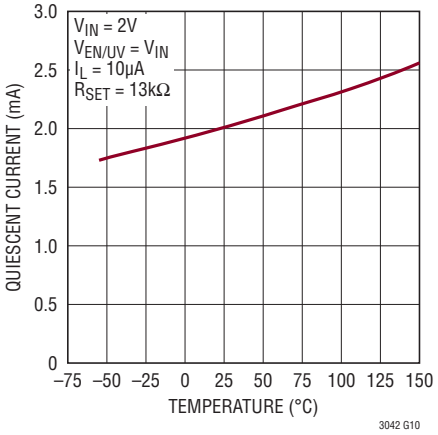
Offset Voltage (V_{OUT} – V_{SET})



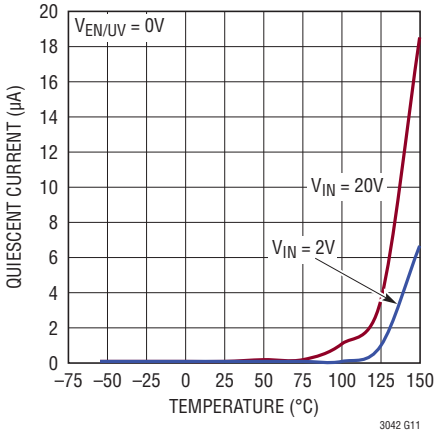
Load Regulation



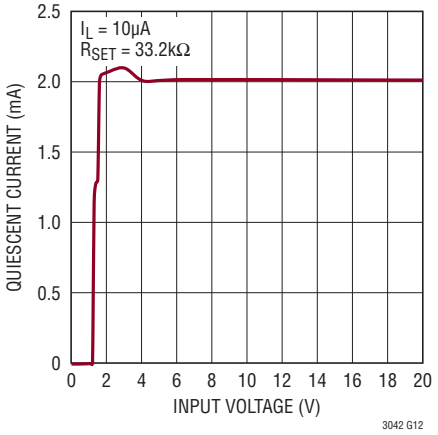
Quiescent Current



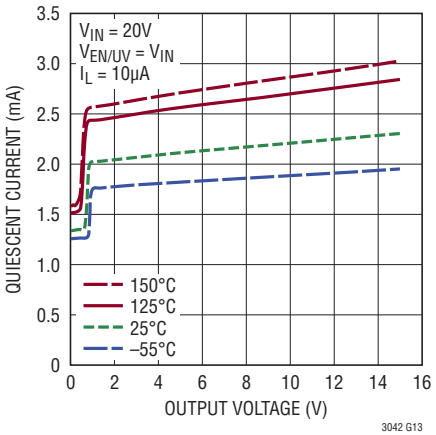
Quiescent Current in Shutdown



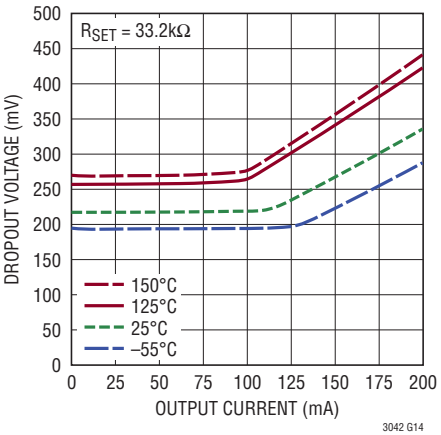
Quiescent Current



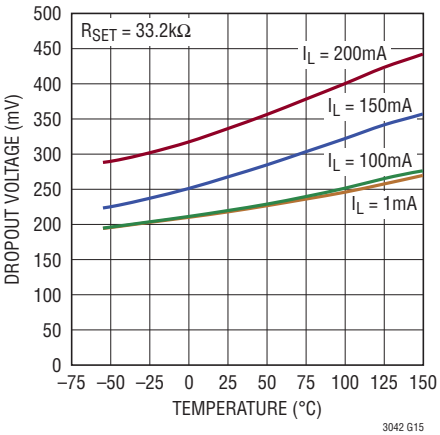
Quiescent Current



Typical Dropout Voltage

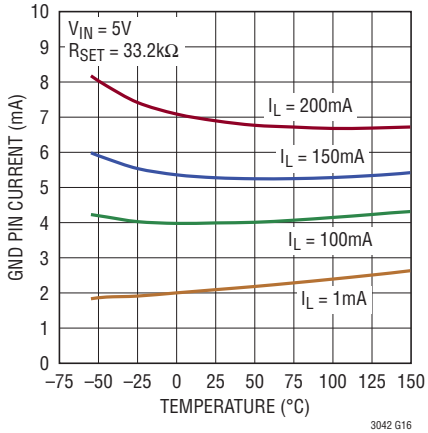


Dropout Voltage

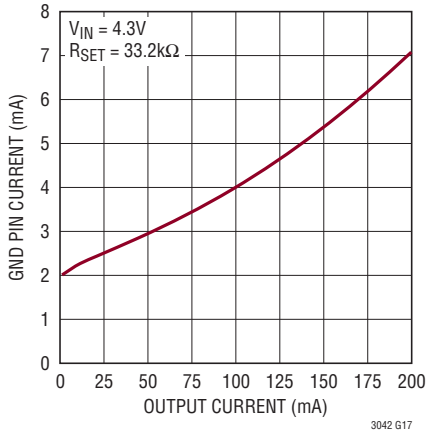


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

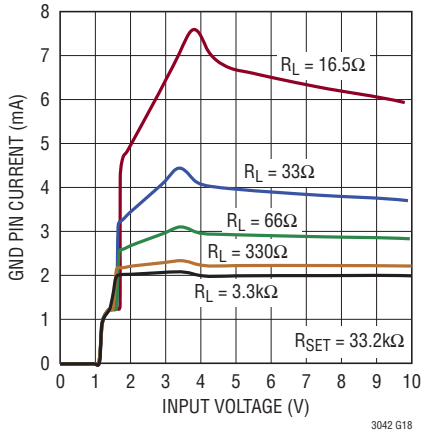
GND Pin Current



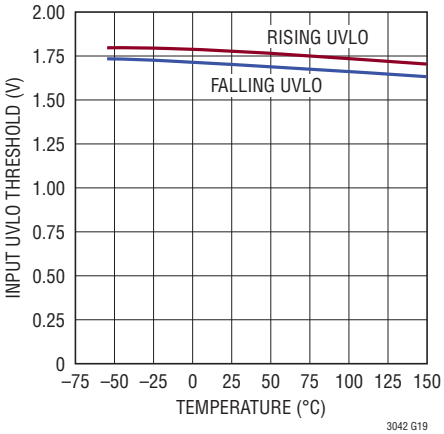
GND Pin Current



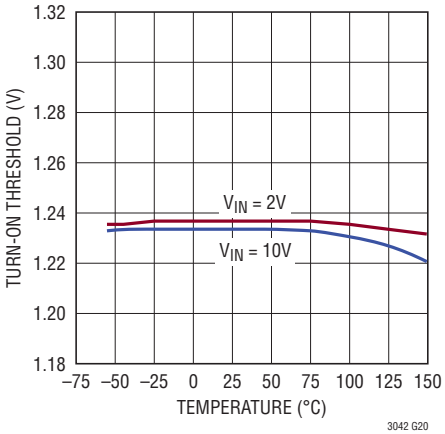
GND Pin Current



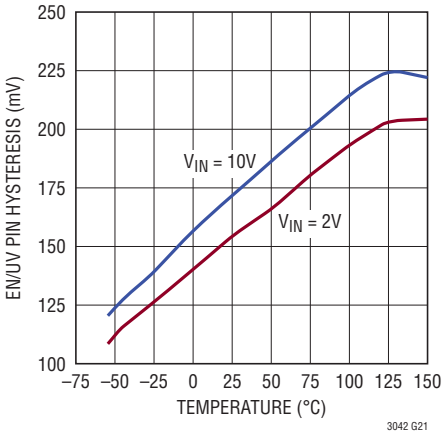
Minimum Input Voltage



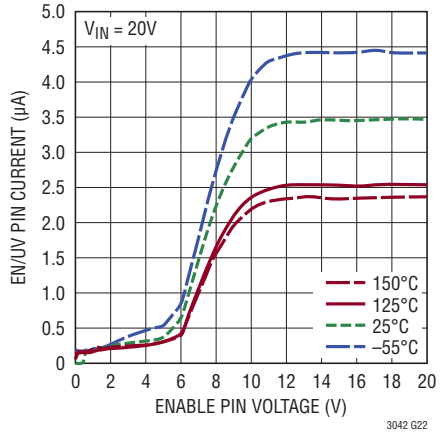
EN/UV Turn-On Threshold



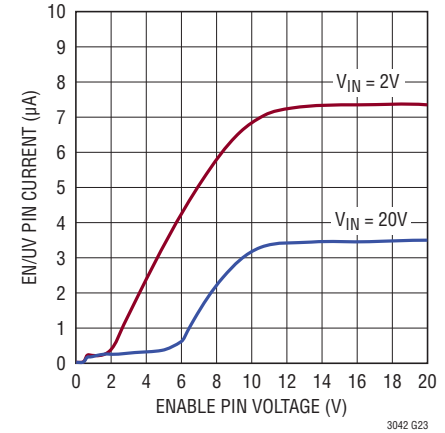
EN/UV Pin Hysteresis



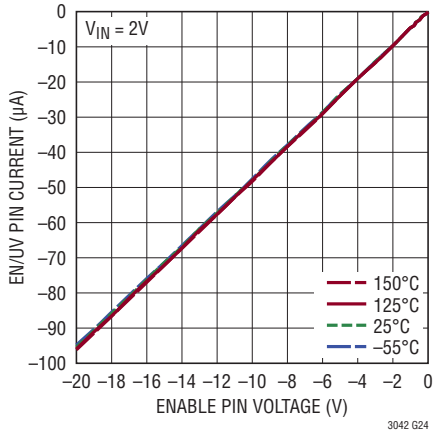
Enable Pin Input Current



Enable Pin Current

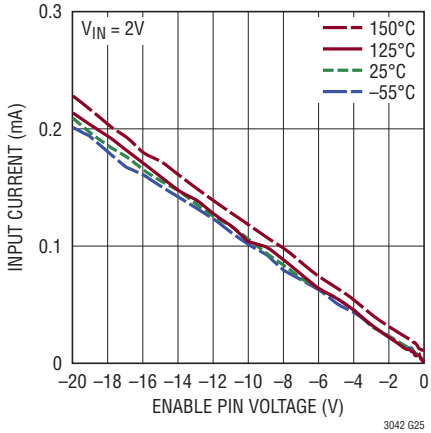


Negative Enable Pin Current

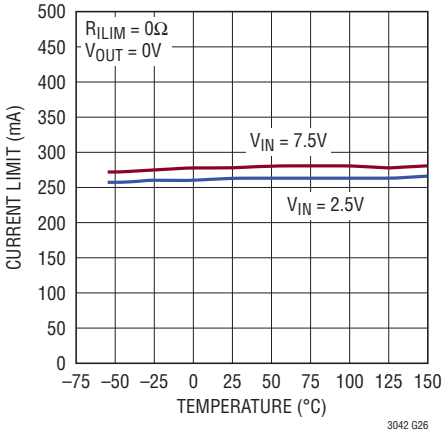


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

Input Pin Current



Internal Current Limit



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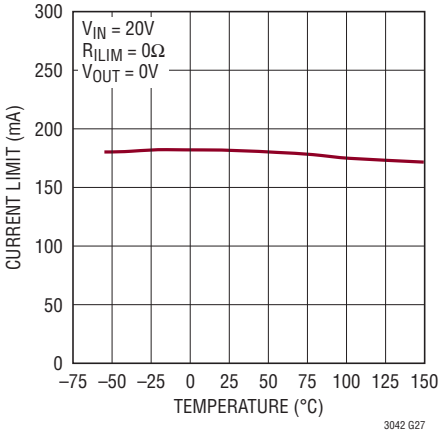

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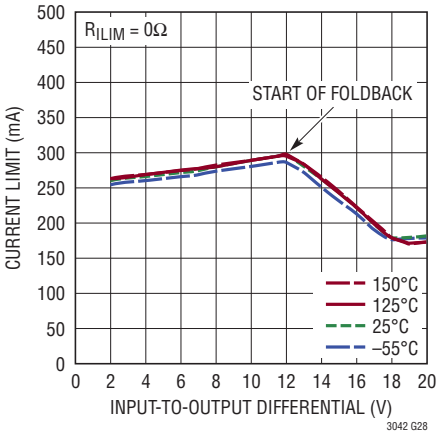
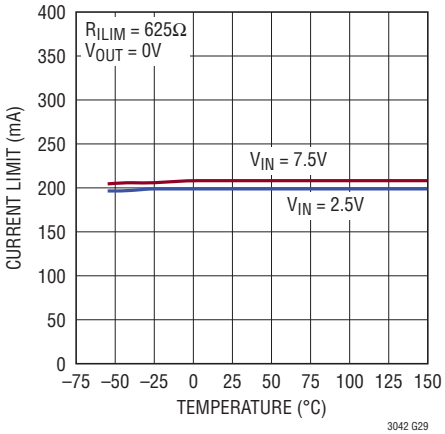
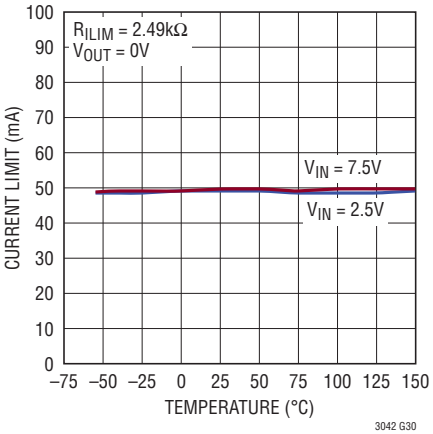


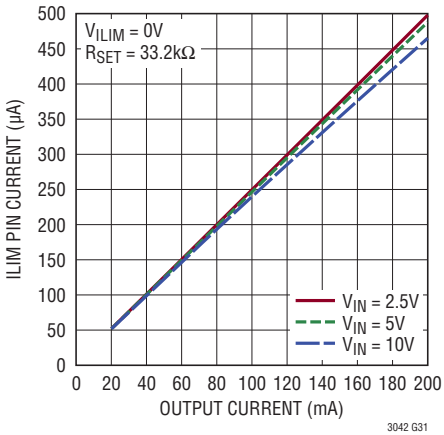
Programmable Current Limit



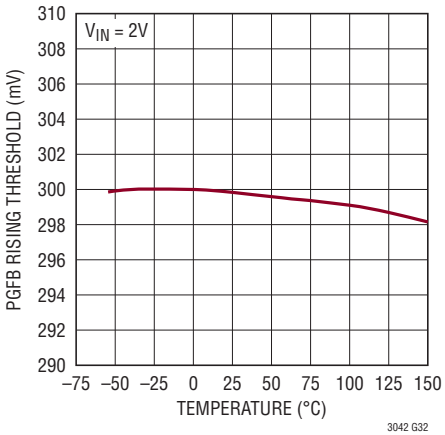
Programmable Current Limit



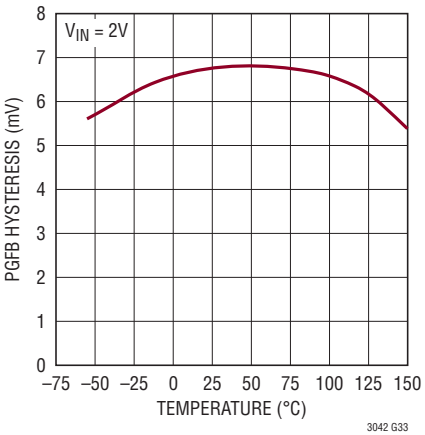
ILIM Pin Current



PGFB Rising Threshold

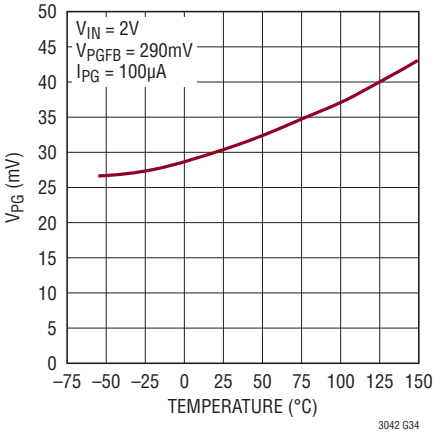


PGFB Hysteresis

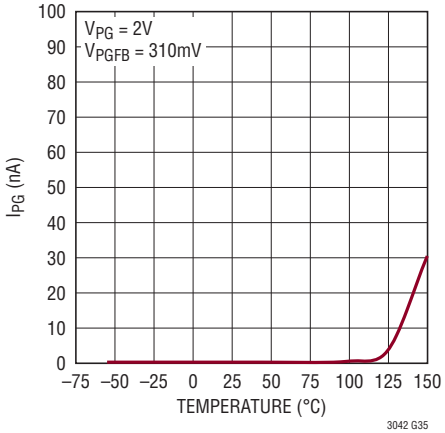


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

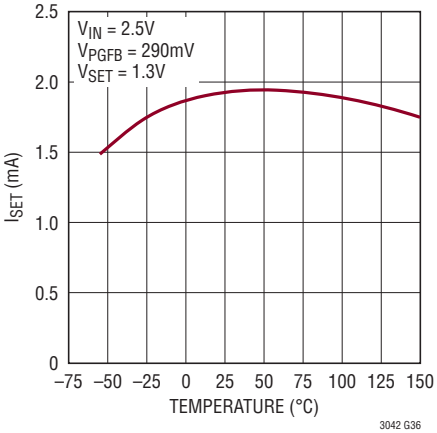
PG Output Low Voltage



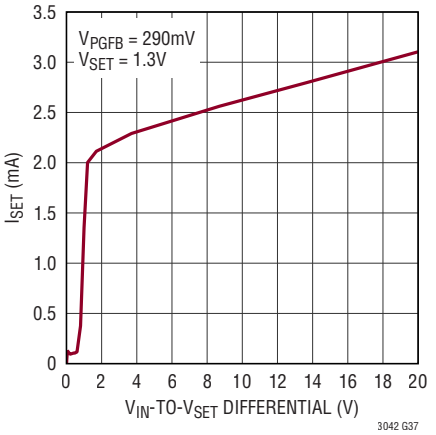
PG Pin Leakage Current



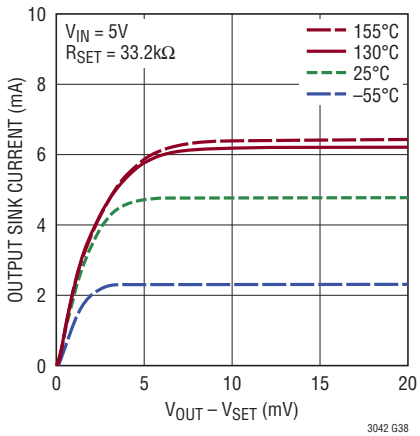
I_{SET} During Start-Up with Fast Start-Up Enabled



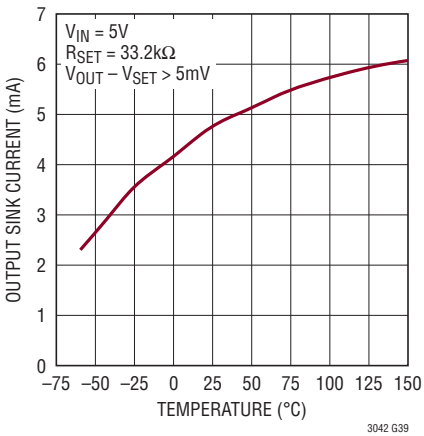
I_{SET} During Start-Up with Fast Start-Up Enabled



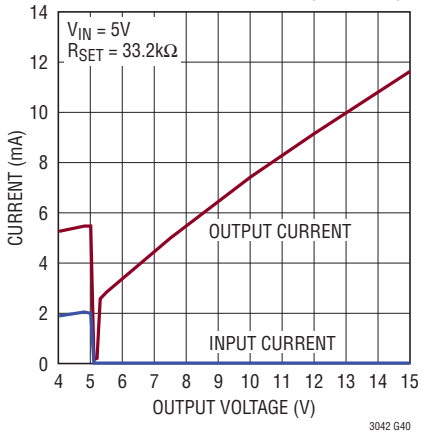
Output Overshoot Recovery Current Sink



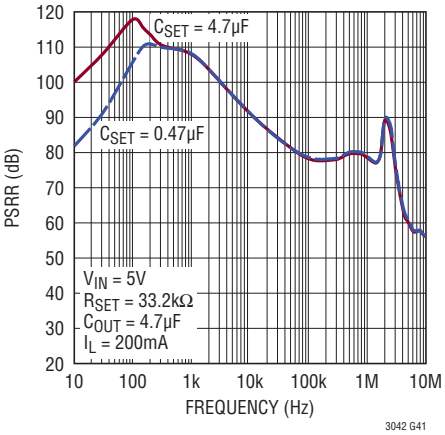
Output Overshoot Recovery Current Sink



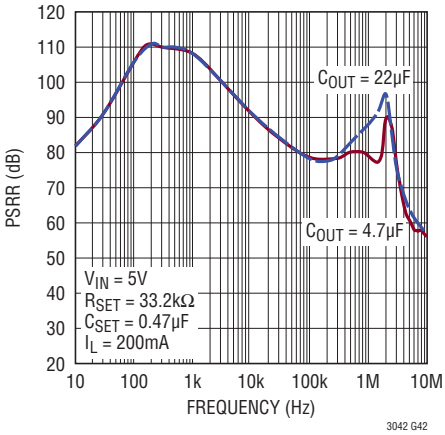
V_{OUT} Forced Above $V_{OUT(NOMINAL)}$



Power Supply Ripple Rejection

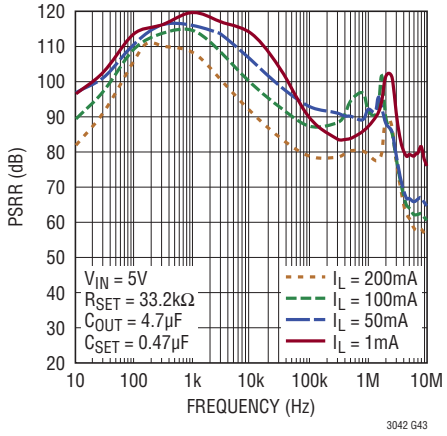


Power Supply Ripple Rejection

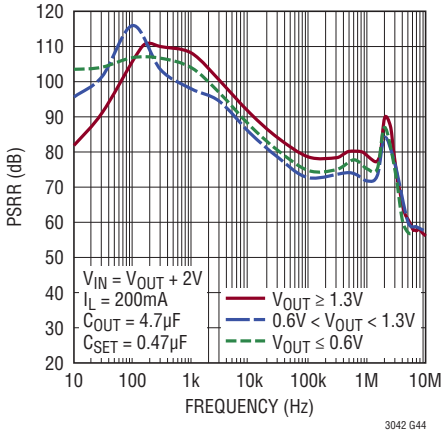


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

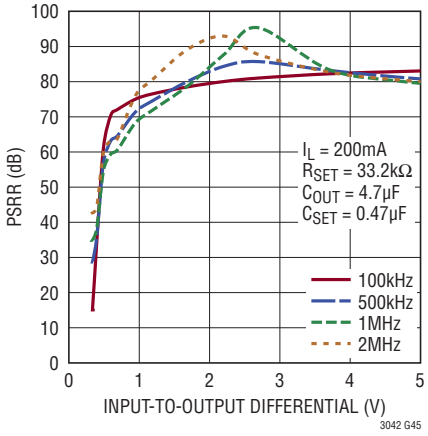
Power Supply Ripple Rejection



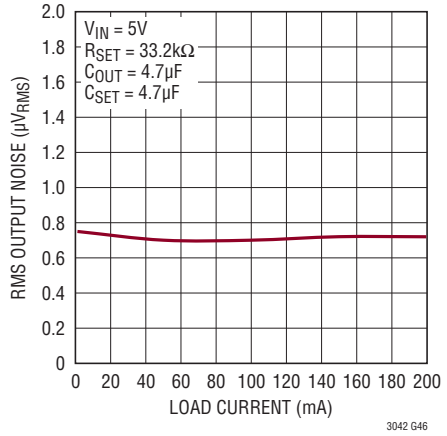
Power Supply Ripple Rejection as a Function of Error Amplifier Input Pair



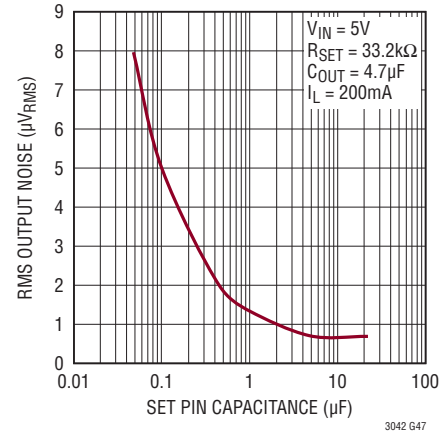
Power Supply Ripple Rejection



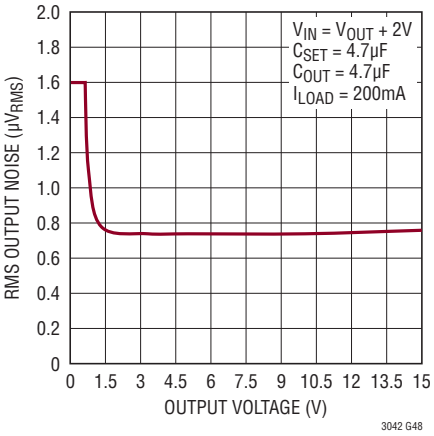
Integrated RMS Output Noise (10Hz to 100kHz)



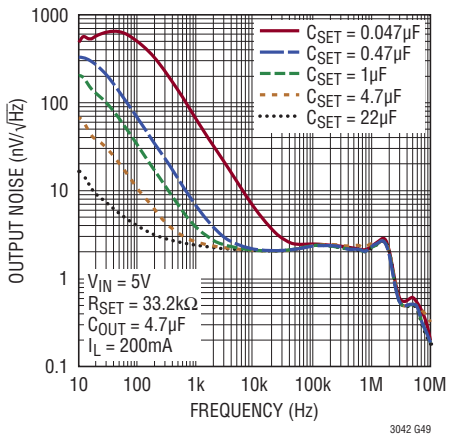
Integrated RMS Output Noise (10Hz to 100kHz)



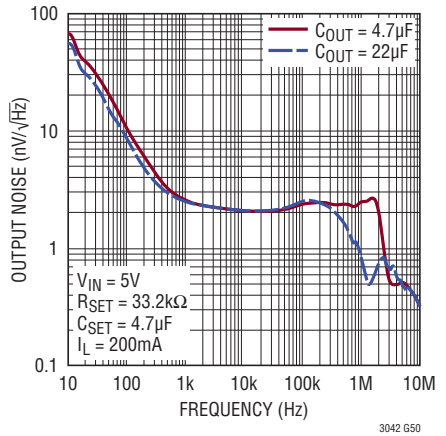
Integrated RMS Output Noise (10Hz to 100kHz)



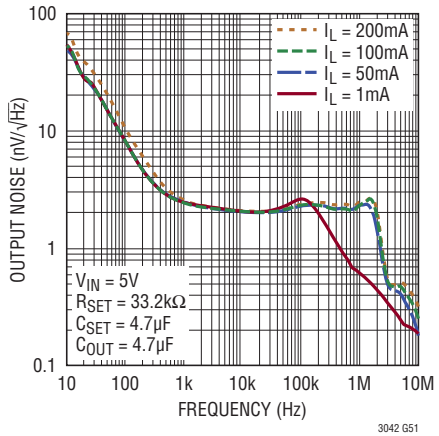
Noise Spectral Density



Noise Spectral Density

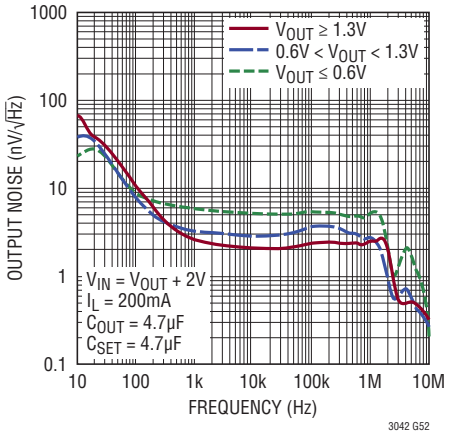


Noise Spectral Density

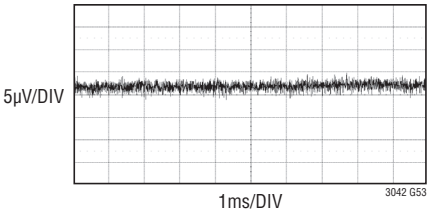


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

Noise Spectral Density as a Function of Error Amplifier Input Pair

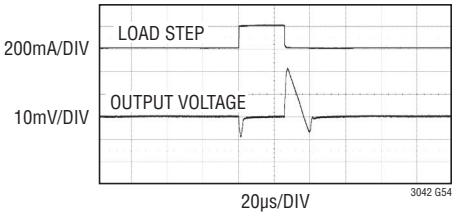


Output Noise: 10Hz to 100kHz



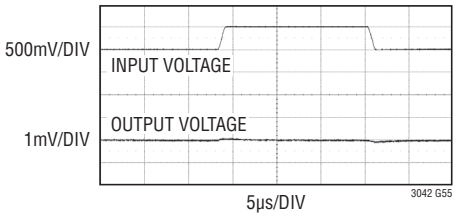
V_{IN} = 5V
R_{SET} = 33.2kΩ
C_{OUT} = 4.7µF
C_{SET} = 4.7µF
I_L = 200mA

Load Transient Response



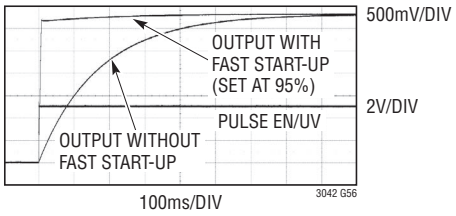
V_{IN} = 5V
R_{SET} = 33.2kΩ
C_{OUT} = 4.7µF
C_{SET} = 0.47µF
LOAD STEP = 10mA TO 200mA

Line Transient Response



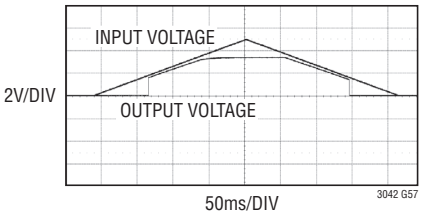
V_{IN} = 4V TO 4.5V
R_{SET} = 33.2kΩ
C_{OUT} = 4.7µF
C_{SET} = 0.47µF
I_L = 200mA

Start-Up Time with and without Fast Start-Up Circuitry for Large C_{SET}



V_{IN} = 5V
R_{SET} = 33.2kΩ
C_{OUT} = 4.7µF
C_{SET} = 4.7µF
R_L = 16.5Ω

Input Supply Ramp-Up and Ramp-Down



V_{IN} = 0V TO 5V
R_{SET} = 33.2kΩ
C_{OUT} = 4.7µF
C_{SET} = 0.47µF
R_L = 16.5Ω

PIN FUNCTIONS

IN (Pins 1, 2): Input. These pins supply power to the regulator. The LT3042 requires a bypass capacitor at the IN pin. In general, a battery's output impedance rises with frequency, so include a bypass capacitor in battery-powered applications. While a 4.7µF input bypass capacitor generally suffices, applications with large load transients may require higher input capacitance to prevent input supply droop. Consult the Applications Information section on the proper use of an input capacitor and its effect on circuit performance, in particular PSRR. The LT3042 withstands reverse voltages on IN with respect to GND, OUTS and OUT. In the case of a reversed input, which occurs if a battery is plugged-in backwards, the LT3042 acts as if a diode is in series with its input. Hence, no reverse current flows into the LT3042 and no negative voltage appears at the load. The device protects itself and the load.

EN/UV (Pin 3): Enable/UVLO. Pulling the LT3042's EN/UV pin low places the part in shutdown. Quiescent current in shutdown drops to less than 1µA and the output voltage turns off. Alternatively, the EN/UV pin can set an input supply undervoltage lockout (UVLO) threshold using a resistor divider between IN, EN/UV and GND. The LT3042 typically turns on when the EN/UV voltage exceeds 1.24V on its rising edge, with a 170mV hysteresis on its falling edge. The EN/UV pin can be driven above the input voltage and maintain proper functionality. If unused, tie EN/UV to IN. Do not float the EN/UV pin.

PG (Pin 4): Power Good. PG is an open-collector flag that indicates output voltage regulation. PG pulls low if PGFB is below 300mV. If the power good functionality is not needed, float the PG pin. A parasitic substrate diode exists between PG and GND pins of the LT3042; do not drive PG more than 0.3V below GND during normal operation or during a fault condition.

ILIM (Pin 5): Current Limit Programming Pin. Connecting a resistor between ILIM and GND programs the current limit. For best accuracy, Kelvin connect this resistor directly to the LT3042's GND pin. The programming scale factor is nominally 125mA•kΩ. The ILIM pin sources current proportional (1:400) to output current; therefore, it also serves as a current monitoring pin with a 0V to 300mV range. If the programmable current limit functionality is not needed, tie ILIM to GND. A parasitic substrate diode exists between ILIM and GND pins of the LT3042; do not drive ILIM more than 0.3V below GND during normal operation or during a fault condition.

PGFB (Pin 6): Power Good Feedback. The PG pin pulls high if PGFB increases beyond 300mV on its rising edge, with 7mV hysteresis on its falling edge. Connecting an external resistor divider between OUT, PGFB and GND sets the programmable power good threshold with the following transfer function: $0.3V \bullet (1 + R_{PG2}/R_{PG1})$. As discussed in the Applications Information section, PGFB also activates the fast start-up circuitry. Tie PGFB to IN if power good and fast start-up functionalities are not needed, and if reverse input protection is additionally required, tie the anode of a 1N4148 diode to IN and its cathode to PGFB. See the Typical Applications section for details. A parasitic substrate diode exists between PGFB and GND pins of the LT3042; do not drive PGFB more than 0.3V below GND during normal operation or during a fault condition.

SET (Pin 7): SET. This pin is the inverting input of the error amplifier and the regulation set-point for the LT3042. SET sources a precision 100µA current that flows through an external resistor connected between SET and GND. The LT3042's output voltage is determined by $V_{SET} = I_{SET} \bullet R_{SET}$. Output voltage range is from zero to 15V. Adding a capacitor from SET to GND improves noise, PSRR and transient response at the expense of increased start-up time. For optimum load regulation, Kelvin connect the ground side of the SET pin resistor directly to the load. A parasitic substrate diode exists between SET and GND pins of the LT3042; do not drive SET more than 0.3V below GND during normal operation or during a fault condition.

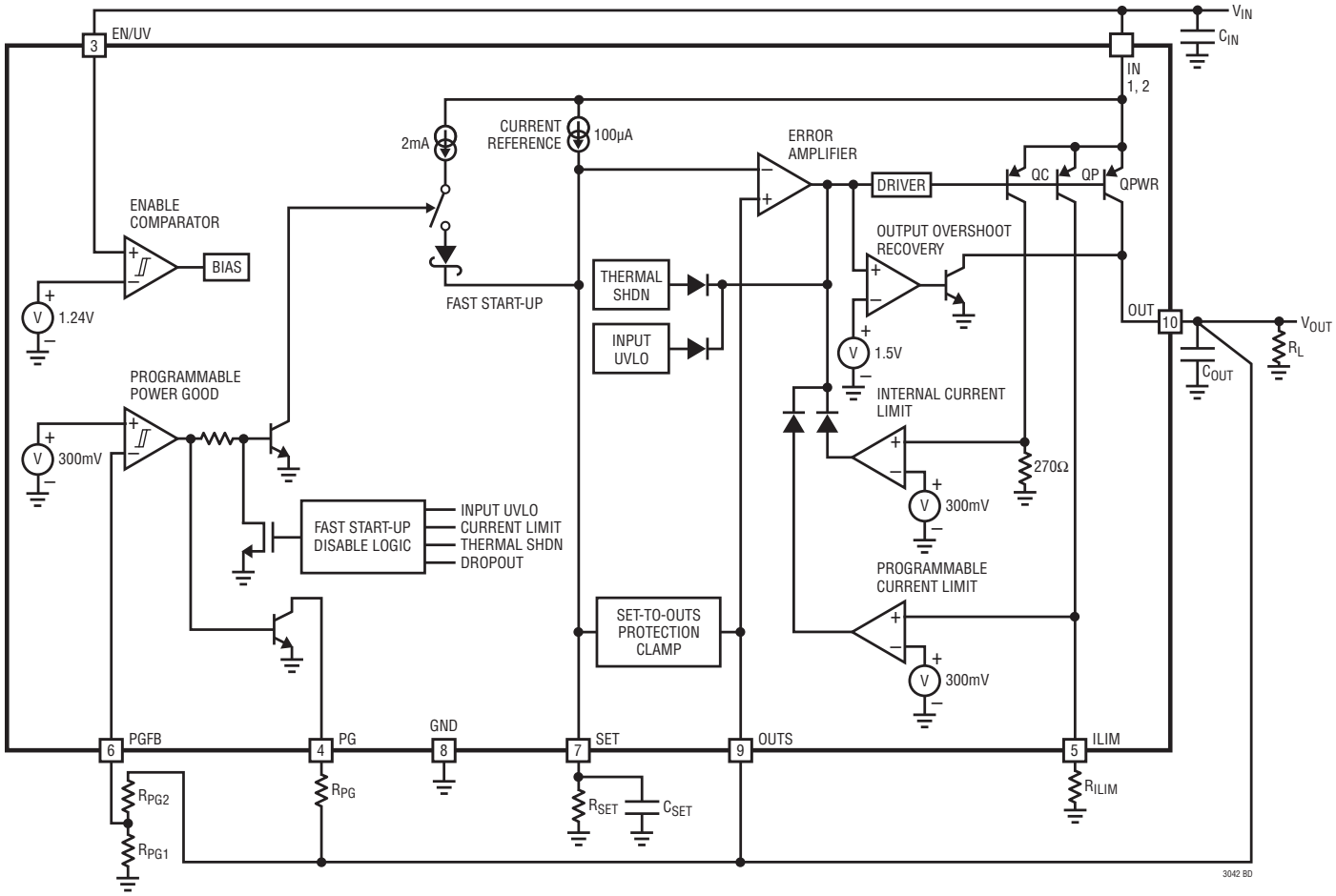
GND (Pin 8, Exposed Pad Pin 11): Ground. The exposed backside is an electrical connection to GND. To ensure proper electrical and thermal performance, solder the exposed backside to the PCB ground and tie it directly to the GND pin.

PIN FUNCTIONS

OUTS (Pin 9): Output Sense. This pin is the noninverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. Also, tie the GND connections of the output capacitor and the SET pin capacitor directly together. Moreover, place the input and output capacitors (and their GND connections) very close together. A parasitic substrate diode exists between OUTS and GND pins of the LT3042; do not drive OUTS more than 0.3V below GND during normal operation or during a fault condition.

OUT (Pin 10): Output. This pin supplies power to the load. For stability, use a minimum 4.7µF output capacitor with an ESR below 50mΩ and an ESL below 2nH. Large load transients require larger output capacitance to limit peak voltage transients. Refer to the Applications Information section for more information on output capacitance. A parasitic substrate diode exists between OUT and GND pins of the LT3042; do not drive OUT more than 0.3V below GND during normal operation or during a fault condition.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT3042 is a high performance low dropout linear regulator featuring LTC's ultralow noise (2nV/√Hz at 10kHz) and ultrahigh PSRR (79dB at 1MHz) architecture for powering noise sensitive applications. Designed as a precision current source followed by a high performance rail-to-rail voltage buffer, the LT3042 can be easily paralleled to further reduce noise, increase output current and spread heat on the PCB. The device additionally features programmable current limit, fast start-up capability and programmable power good.

The LT3042 is easy to use and incorporates all of the protection features expected in high performance regulators. Included are short-circuit protection, safe operating area protection, reverse battery protection, reverse current protection, and thermal shutdown with hysteresis.

Output Voltage

The LT3042 incorporates a precision 100µA current source flowing out of the SET pin, which also ties to the error amplifier's inverting input. Figure 1 illustrates that connecting a resistor from SET to ground generates a reference voltage for the error amplifier. This reference voltage is simply the product of the SET pin current and the SET pin resistor. The error amplifier's unity-gain configuration produces a low impedance version of this voltage on its noninverting input, i.e. the OUTS pin, which is externally tied to the OUT pin.

The LT3042's rail-to-rail error amplifier and current reference allows for a wide output voltage range from 0V (using a 0Ω resistor) to V_{IN} minus dropout — up to 15V. A PNP-based input pair is active for 0V to 0.6V output and an NPN-based input pair is active for output voltages greater than 1.3V, with a smooth transition between the two input pairs from 0.6V to 1.3V output. While the NPN-based input pair is designed to offer the best overall performance, refer to the Electrical Characteristics Table for details on offset voltage, SET pin current, output noise and PSRR variation with the error amp input pair. Table 1 lists many common output voltages and their corresponding 1% R_{SET} resistors.

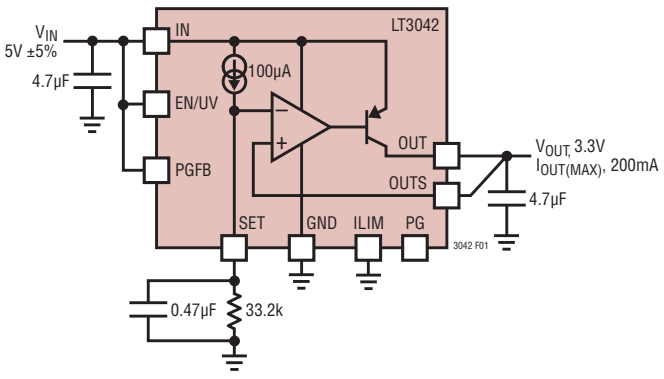


Figure 1. Basic Adjustable Regulator

Table 1. 1% Resistor for Common Output Voltages

V_{OUT} (V)	R_{SET} (kΩ)
2.5	24.9
3.3	33.2
5	49.9
12	121
15	150

The benefit of using a current reference compared with a voltage reference as used in conventional regulators is that the regulator always operates in unity gain configuration, independent of the programmed output voltage. This allows the LT3042 to have loop gain, frequency response and bandwidth independent of the output voltage. As a result, noise, PSRR and transient performance do not change with output voltage. Moreover, since none of the error amp gain is needed to amplify the SET pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds of microvolts range and not as a fixed percentage of the output voltage.

Since the zero TC current source is highly accurate, the SET pin resistor can become the limiting factor in achieving high accuracy. Hence, it should be a precision resistor. Additionally, any leakage paths to or from the SET pin create errors in the output voltage. If necessary, use high quality insulation (e.g., Teflon, Kel-F); moreover, cleaning of all insulating surfaces to remove fluxes and other residues may be required. High humidity environments may require a surface coating at the SET pin to provide a moisture barrier.

Minimize board leakage by encircling the SET pin with a guard ring operated at a potential close to itself — ideally tied to the OUT pin. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard ring width. Leakages of 100nA into or out of

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the SET pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over wide operating temperature range. Figure 2illustrates a typical guard ring layout technique.

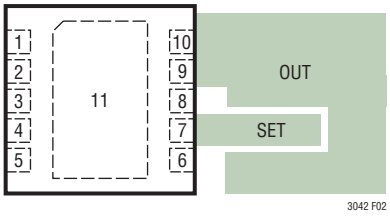

Figure 2. Guard Ring Layout

Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the SET pin with a small capacitance to ground resolves this issue — 10nF is sufficient.

For applications requiring higher accuracy or an adjustable output voltage, the SET pin may be actively driven by an external voltage source capable of sinking 100µA. Connecting a precision voltage reference to the SET pin eliminates any errors present in the output voltage due to the reference current and SET pin resistor tolerances.

Output Sensing and Stability

The LT3042's OUTS pin provides a Kelvin sense connection to the output. The SET pin resistor's GND side provides a Kelvin sense connection to the load's GND side.

Additionally, for ultrahigh PSRR, the LT3042 bandwidth is made quite high (~1MHz), making it close to a typical 4.7µF (1206 case size) ceramic output capacitor's self-resonance frequency (~2.3MHz). Therefore, it is very important to avoid adding extra impedance (ESR and ESL) outside the feedback loop. To that end, as shown in Figure 3, minimize the effects of PCB trace and solder inductance by tying the OUTS pin directly to C_{OUT} and the GND side of CSET directly to the GND side of C_{OUT}, as well as keep the GND sides of C_{IN} and C_{OUT} reasonably close. Refer to the LT3042 demo board manual for more information on the recommended layout that meets these

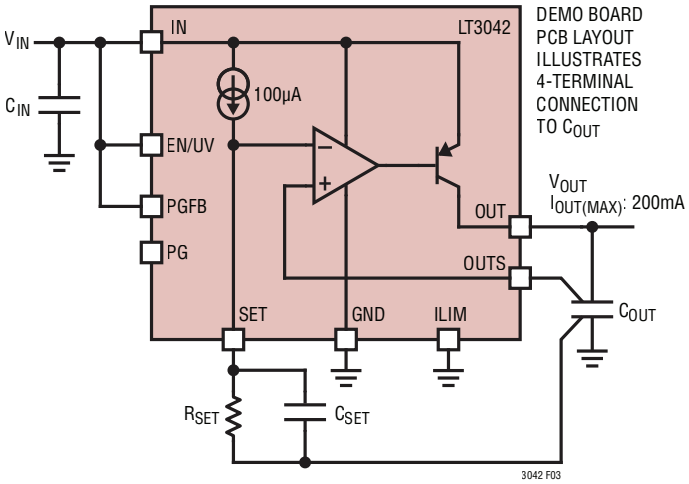

Figure 3. C_{OUT} and C_{SET} Connections for Stability

requirements. While the LT3042 is robust enough not to oscillate if the recommended layout is not followed, depending on the actual layout, phase/gain margin, noise and PSRR performance may degrade.

Stability and Output Capacitance

The LT3042 requires an output capacitor for stability. Given its high bandwidth, LTC recommends low ESR and ESL ceramic capacitors. A minimum 4.7µF output capacitor with an ESR below 50mΩ and an ESL below 2nH is required for stability.

Given the high PSRR and low noise performance attained using a single 4.7µF ceramic output capacitor, larger values of output capacitor only marginally improves the performance because the regulator bandwidth decreases with increasing output capacitance — hence, there is little to be gained by using larger than the minimum 4.7µF output capacitor. Nonetheless, larger values of output capacitance do decrease peak output deviations during a load transient. Note that bypass capacitors used to decouple individual components powered by the LT3042 increase the effective output capacitance.

Give extra consideration to the type of ceramic capacitors used. They are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V,

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X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in the small packages, but they tend to have stronger voltage and temperature coefficients as shown in Figure 4 and Figure 5. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied over the operating temperature range.

X5R and X7R dielectrics result in more stable characteristics and are thus more suitable for LT3042. The X7R dielectric has better stability across temperature, while the X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and the maximum capacitance change over temperature. While capacitance change due to DC bias for X5R and X7R is better than Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance below sufficient levels. As shown in Figure 6, capacitor DC bias characteristics tend to improve as component case size increases, **but verification of expected capacitance at the operating voltage is highly recommended.**

High Vibration Environments

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress upon it, similar to how a piezoelectric microphone works. For a ceramic capacitor, this stress can be induced by mechanical vibrations within the system or due to thermal transients.

LT3042 applications in high vibration environments have three distinct piezoelectric noise generators: ceramic output, input, and SET pin capacitors. However, due to LT3042's very low output impedance over a wide frequency range, negligible output noise is generated using a ceramic output capacitor. Similarly, due to LT3042's ultrahigh PSRR, negligible output noise is generated using a ceramic input capacitor. Nonetheless, given the high SET pin impedance, any piezoelectric response from a ceramic SET pin capacitor generates significant output noise – peak-to-peak excursions of hundreds of µVs. However, due to the SET pin capacitor's high ESR

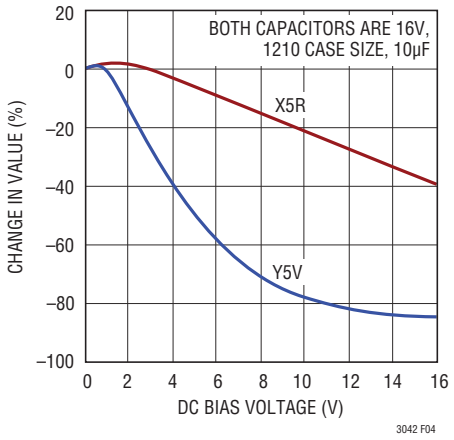

Figure 4. Ceramic Capacitor DC Bias Characteristics

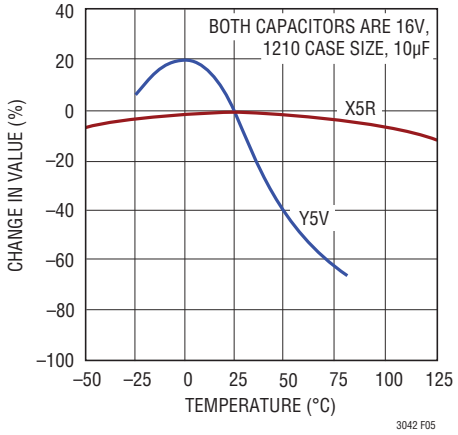

Figure 5. Ceramic Capacitor Temperature Characteristics

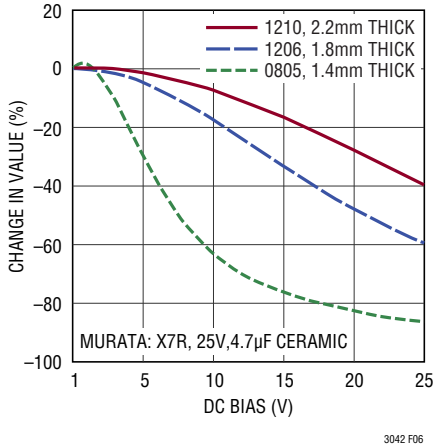

Figure 6. Capacitor Voltage Coefficient for Different Case Sizes

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and ESL tolerance, any non-piezoelectrically responsive (tantalum, electrolytic, or film) capacitor can be used at the SET pin – although electrolytic capacitors tend to have high 1/f noise. In any case, use of surface mount capacitor is highly recommended.

Stability and Input Capacitance

The LT3042 is stable with a minimum 4.7µF IN pin capacitor. LTC recommends using low ESR ceramic capacitors. In cases where long wires connect the power supply to the LT3042's input and ground terminals, the use of low value input capacitors combined with a large load current can result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause and not because of LT3042's instability.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. The wire diameter, however, has less influence on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce a wire's self-inductance. One method divides the current flowing towards the LT3042 between two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connect two equal inductors in parallel. However, when placed in close proximity to each other, their mutual inductance adds to the overall self inductance of the wires — therefore a 50% reduction is not possible in such cases. The second and more effective technique to reduce the overall inductance is to place the forward and return current conductors (the input and ground wires) in close proximity. Two 30-AWG wires separated by 0.02" reduce the overall inductance to about one-fifth of a single wire.

If a battery mounted in close proximity powers the LT3042, a 4.7µF input capacitor suffices for stability. However, if a distantly located supply powers the LT3042, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 4.7µF minimum) per 8" of wire length. The minimum input capacitance needed to stabilize the application also varies with the output capacitance as well as the load current. Placing additional capacitance on the LT3042's output helps. However, this requires significantly more capacitance compared to additional input bypassing. Series resistance between the supply and the LT3042 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use a higher ESR tantalum or electrolytic capacitor at the LT3042 input in parallel with a 4.7µF ceramic capacitor.

PSRR and Input Capacitance

For applications utilizing the LT3042 for post-regulating switching converters, placing a capacitor directly at the LT3042 input results in ac current (at the switching frequency) to flow near the LT3042. This relatively high frequency switching current generates a magnetic field that couples to the LT3042 output, thereby degrading its effective PSRR. While highly dependent on the PCB, the switching pre-regulator, the input capacitance, amongst other factors, the PSRR degradation can be easily over 30dB at 1MHz. This degradation is present even if the LT3042 is de-soldered from the board, because it effectively degrades the PSRR of the PC board itself. While negligible for conventional low PSRR LDOs, LT3042's ultrahigh PSRR requires careful attention to higher order parasitics in order to extract the full performance offered by the regulator.

To mitigate the flow of high-frequency switching current near the LT3042, the LT3042 input capacitor can be entirely removed—as long as the switching converter's output capacitor is located more than an inch away from the LT3042. Magnetic coupling rapidly decreases with increasing distance. Nonetheless, if the switching pre-regulator is placed too far away (conservatively more than a couple inches) from the LT3042, with no input capacitor present, as with any regulator, the LT3042 input will oscillate at the parasitic LC resonance frequency. Besides, it is generally a very common (and a preferred) practice to bypass regulator input with some capacitance. So this option is fairly limited in its scope and not the most palatable solution.

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To that end, LTC recommends using the LT3042 demo board (DC2246B) layout for achieving the best possible PSRR performance. The LT3042 demo board layout utilizes magnetic field cancellation techniques to prevent PSRR degradation caused by this high-frequency current flow—while utilizing the input capacitor.

Filtering High Frequency Spikes

For applications where the LT3042 is used to post-regulate a switching converter, its high PSRR effectively suppresses any "noise" present at the switcher's switching frequency — typically 100kHz to 4MHz. However, the very high frequency (100s of MHz) "spikes" — beyond the LT3042's bandwidth — associated with the switcher's power switch transition times will almost directly pass through the LT3042. While the output capacitor is partly intended to absorb these spikes, its ESL will limit its ability at these frequencies. A ferrite bead or even the inductance associated with a short (e.g. 0.5") PCB trace between the switcher's output and the LT3042's input can serve as an LC-filter to suppress these very high frequency spikes.

Output Noise

The LT3042 offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a traditional regulator are its voltage reference, error amplifier, noise from the resistor divider network used for setting output voltage and the noise gain created by this resistor divider. Many low noise regulators pin out their voltage reference to allow for noise reduction by bypassing the reference voltage.

Unlike most linear regulators, the LT3042 does not use a voltage reference; instead, it uses a 100µA current reference. The current reference operates with typical noise current level of $20pA/\sqrt{Hz}$ ($6nA_{RMS}$ over a 10Hz to 100kHz bandwidth). The resultant voltage noise equals the current noise multiplied by the resistor value, which in turn is RMS summed with the error amplifier's noise and the resistor's own noise of $\sqrt{4kTR}$ — whereby k = Boltzmann's constant $1.38 \cdot 10^{-23}$J/K and T is the absolute temperature.

One problem that conventional linear regulators face is that the resistor divider setting the output voltage gains up the reference noise. In contrast, the LT3042's unity-gain follower architecture presents no gain from the SET pin to the output. Therefore, if a capacitor bypasses the SET pin resistor, then the output noise is independent of the programmed output voltage. The resultant output noise is then set just by the error amplifier's noise — typically $2nV/\sqrt{Hz}$ from 10kHz to 1MHz and $0.8\mu V_{RMS}$ in a 10Hz to 100kHz bandwidth using a 4.7µF SET pin capacitor. Paralleling multiple LT3042s further reduces noise by $\sqrt{N}$, for N parallel regulators.

Refer to the Typical Performance Characteristics section for noise spectral density and RMS integrated noise over various load currents and SET pin capacitances.

Set Pin (Bypass) Capacitance: Noise, PSRR, Transient Response and Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor also improves PSRR and transient performance. Note that any bypass capacitor leakage deteriorates the LT3042's DC regulation. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, LTC recommends the use of a good quality low leakage ceramic capacitor.

Using a SET pin bypass capacitor also soft-starts the output and limits inrush current. The RC time constant, formed by the SET pin resistor and capacitor, controls soft-start time. Ramp-up rate from 0 to 90% of nominal V_{OUT} is:

$$t_{SS} \approx 2.3 \bullet R_{SET} \bullet C_{SET} \text{ (fast start-up disabled)}$$

Fast Start-Up

For ultralow noise applications that require low 1/f noise (i.e. at frequencies below 100Hz), a larger value SET pin capacitor is required, up to 22µF. While normally this would significantly increase the regulator's start-up time, the LT3042 incorporates fast start-up circuitry that increases the SET pin current to about 2mA during start-up.

As shown in the Block Diagram, the 2mA current source remains engaged while PGFB is below 300mV, unless the regulator is in current limit, dropout, thermal shutdown or input voltage is below minimum V_{IN}.

If fast start-up capability is not used, tie PGFB to IN or to OUT for output voltages above 300mV. Note that doing so also disables power good functionality.

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ENABLE/UVLO

The EN/UV pin is used to put the regulator into a micropower shutdown state. The LT3042 has an accurate 1.24V turn-on threshold on the EN/UV pin with 170mV of hysteresis. This threshold can be used in conjunction with a resistor divider from the input supply to define an accurate undervoltage lockout (UVLO) threshold for the regulator. The EN/UV pin current (I_{EN}) at the threshold from the Electrical Characteristics table needs to be considered when calculating the resistor divider network:

$$V_{IN(UVLO)} = 1.24V \bullet \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + I_{EN} \bullet R_{EN2}$$

The EN/UV pin current (I_{EN}) can be ignored if R_{EN1} is less than 100k. If unused, tie EN/UV pin to IN.

Programmable Power Good

As illustrated in the Block Diagram, power good threshold is user programmable using the ratio of two external resistors, R_{PG2} and R_{PG1}:

$$V_{OUT(PG\_THRESHOLD)} = 0.3V \bullet \left(1 + \frac{R_{PG2}}{R_{PG1}}\right) + I_{PGFB} \bullet R_{PG2}$$

If the PGFB pin increases above 300mV, the open-collector PG pin de-asserts and becomes high impedance. The power good comparator has 7mV hysteresis and 5µs of deglitching. The PGFB pin current (I_{PGFB}) from the Electrical Characteristics table must be considered when determining the resistor divider network. The PGFB pin current (I_{PGFB}) can be ignored if R_{PG1} is less than 30k. If power good functionality is not used, float the PG pin. Please note that programmable power good and fast start-up capabilities are disabled for output voltages below 300mV or when the device is in shutdown.

Externally Programmable Current Limit

The ILIM pin's current limit threshold is 300mV. Connecting a resistor from ILIM to GND sets the maximum current flowing out of the ILIM pin, which in turn programs the LT3042's current limit. With a 125mA • kΩ programming scale factor, the current limit can be calculated as follows:

$$\text{Current Limit} = 125mA \bullet k\Omega / R_{ILIM}$$

For example, a 1kΩ resistor programs the current limit to 125mA and a 2kΩ resistor programs the current limit to 62.5mA. For good accuracy, Kelvin connect this resistor to the LT3042's GND pin.

In cases where IN-to-OUT differential is greater than 12V, the LT3042's foldback circuitry decreases the internal current limit. As a result, internal current limit may override the externally programmed current limit level to keep the LT3042 within its safe-operating-area (SOA). See the Internal Current Limit vs Input-to-Output Differential graph in the Typical Performance Characteristics section.

As shown in the Block Diagram, the ILIM pin sources current proportional (1:400) to output current; therefore, it also serves as a current monitoring pin with a 0V to 300mV range. If external current limit or current monitoring is not used, tie ILIM to GND.

Output Overshoot Recovery

During a load step from full load to no load (or light load), the output voltage overshoots before the regulator responds to turn the power transistor OFF. Given that there is no load (or very light load) present at the output, it takes a long time to discharge the output capacitor.

As illustrated in the Block Diagram, the LT3042 incorporates an overshoot recovery circuitry that turns on a current sink to discharge the output capacitor in the event OUTS is higher than SET. This current is typically about 4mA. No load recovery is disabled for input voltages less than 2.5V or output voltages less than 1.5V.

If OUTS is externally held above SET, the current sink turns ON in an attempt to restore OUTS to its programmed voltage. The current sink remains ON until the external circuitry releases OUTS.

Direct Paralleling for Higher Current

Higher output current is obtained by paralleling multiple LT3042s. Tie all SET pins together and all IN pins together. Connect the OUT pins together using small pieces of PCB trace (used as a ballast resistor) to equalize currents in the LT3042s. PCB trace resistance in milliohms/inch is shown in Table 2.

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Table 2. PC Board Trace Resistance

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in.

The small worst-case offset of 2mV for each paralleled LT3042 minimizes the required ballast resistor value. Figure 7 illustrates that two LT3042s, each using a 50mΩ PCB trace ballast resistor, provide better than 20% accurate output current sharing at full load. The two 50mΩ external resistors only add 10mV of output regulation drop with a 400mA maximum current. With a 3.3V output, this only adds 0.3% to the regulation accuracy. As has been discussed previously, tie the OUTS pin directly to the output capacitor.

More than two LT3042s can also be paralleled for even higher output current and lower output noise. Paralleling multiple LT3042s is also useful for distributing heat on the PCB. For applications with high input-to-output voltage differential, an input series resistor or resistor in parallel with the LT3042 can also be used to spread heat.

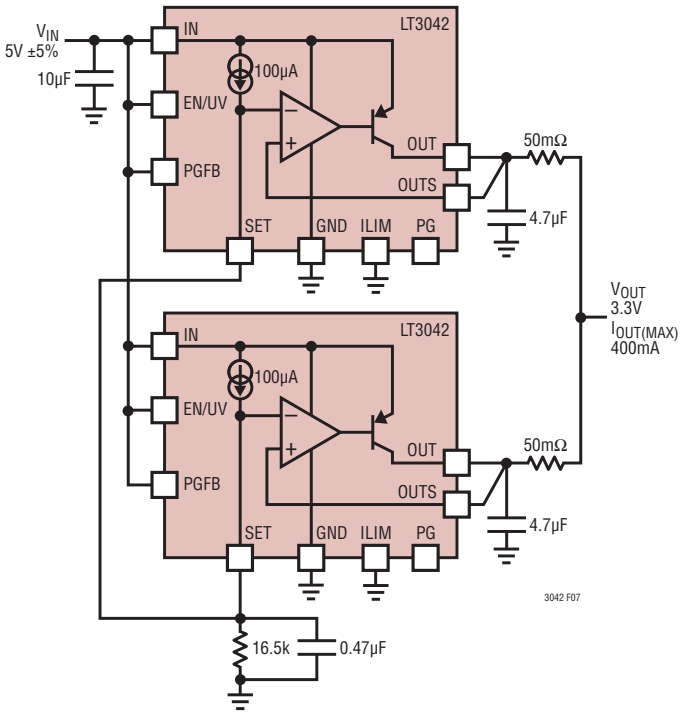

Figure 7. Parallel Devices

PCB Layout Considerations

Given the LT3042's high bandwidth and ultrahigh PSRR, careful PCB layout must be employed to achieve full device performance. Figure 8 shows an example layout that delivers full performance of the regulator. Refer to the LT3042's DC2246B demo board manual for further details.

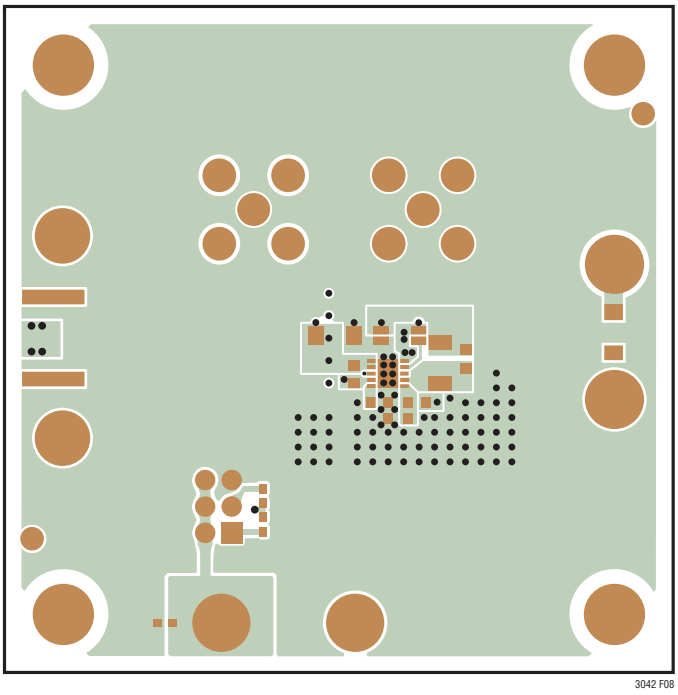

Figure 8. Example DFN Layout

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Thermal Considerations

The LT3042 has internal power and thermal limiting circuits that protect the device under overload conditions. The thermal shutdown temperature is nominally 162°C with about 8°C of hysteresis. For continuous normal load conditions, do not exceed the maximum junction temperature, (125°C for E-, I-grades and 150°C for H-, MP-grades). It is important to consider all sources of thermal resistance from junction to ambient. This includes junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient as the application dictates. Additionally, consider all heat sources in close proximity to the LT3042.

The undersides of the DFN and MSOP packages have exposed metal from the lead frame to the die attachment. Both packages allow heat to directly transfer from the die junction to the PCB metal to limit maximum operating junction temperature. The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by the regulator.

Tables 3 and 4 list thermal resistance as a function of copper area on a fixed board size. All measurements were taken in still air on a 4 layer FR-4 board with 1oz solid internal planes and 2oz top/bottom planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-7 and JESD51-12. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

Table 3. Measured Thermal Resistance for DFN Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE
TOP SIDE*	BOTTOM SIDE		
2500mm^2	2500mm^2	2500mm^2	34°C/W
1000mm^2	2500mm^2	2500mm^2	34°C/W
225mm^2	2500mm^2	2500mm^2	35°C/W
100mm^2	2500mm^2	2500mm^2	36°C/W

*Device is mounted on topside

Table 4. Measured Thermal Resistance for MSOP Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE
TOP SIDE*	BOTTOM SIDE		
2500mm^2	2500mm^2	2500mm^2	33°C/W
1000mm^2	2500mm^2	2500mm^2	33°C/W
225mm^2	2500mm^2	2500mm^2	34°C/W
100mm^2	2500mm^2	2500mm^2	35°C/W

*Device is mounted on topside

Calculating Junction Temperature

Example: Given an output voltage of 2.5V and input voltage of 5V ± 5%, output current range from 1mA to 200mA, and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The LT3042's power dissipation is:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet V_{IN(MAX)}$$

where:

$I_{OUT(MAX)} = 200mA$

$V_{IN(MAX)} = 5.25V$

I_{GND} (at $I_{OUT} = 200mA$ and $V_{IN} = 5.25V$) = 7.2mA

thus:

$$P_{DISS} = 0.2A \bullet (5.25V - 2.5V) + 7.2mA \bullet 5.25V = 0.59W$$

Using a DFN package, the thermal resistance is in the range of 34°C/W to 36°C/W depending on the copper area. Therefore, the junction temperature rise above ambient approximately equals:

$0.59W \bullet 35°C/W = 20.7°C$

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The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient:

T_{JMAX} = 85°C + 20.7°C = 105.7°C

Overload Recovery

Like many IC power regulators, the LT3042 incorporates safe-operating-area (SOA) protection. The SOA protection activates at input-to-output differential voltages greater than 12V. The SOA protection decreases the current limit as the input-to-output differential increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltages up to the LT3042's absolute maximum ratings. The LT3042 provides some level of output current for all values of input-to-output differentials. Refer to the Current Limit curves in the Typical Performance Characteristics section. When power is first applied and input voltage rises, the output follows the input and keeps the input-to-output differential low to allow the regulator to supply large output current and start-up into high current loads.

Due to current limit foldback, however, at high input voltages a problem can occur if the output voltage is low and the load current is high. Such situations occur after the removal of a short-circuit or if the EN/UV pin is pulled high after the input voltage has already turned ON. The load line in such cases intersects the output current profile at two points. The regulator now has two stable operating points. With this double intersection, the input power supply may need to be cycled down to zero and brought back up again to make the output recover. Other linear regulators with foldback current limit protection (such as the LT1965 and LT1963A, etc.) also exhibit this phenomenon, so it is not unique to the LT3042.

Protection Features

The LT3042 incorporates several protection features for battery-powered applications. Precision current limit and thermal overload protection protect the LT3042 against overload and fault conditions at the device's output. For normal operation, do not allow the junction temperature to exceed 125°C (E-, I-grade) or 150°C (H-, MP-grade).

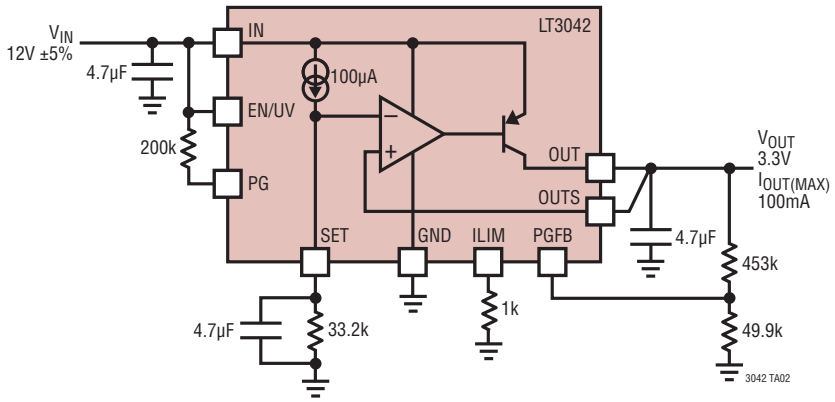
To protect the LT3042's low noise error amplifier, the SET-to-OUTS protection clamp limits the maximum voltage between SET and OUTS with a maximum DC current of 20mA through the clamp. So for applications where SET is actively driven by a voltage source, the voltage source must be current limited to 20mA or less. Moreover, to limit the transient current flowing through these clamps during a transient fault condition, limit the maximum value of the SET pin capacitor (C_{SET}) to 22µF.

The LT3042 also incorporates reverse input protection whereby the IN pin withstands reverse voltages of up to –20V without causing any input current flow and without developing negative voltages at the OUT pin. The regulator protects both itself and the load against batteries that are plugged-in backwards.

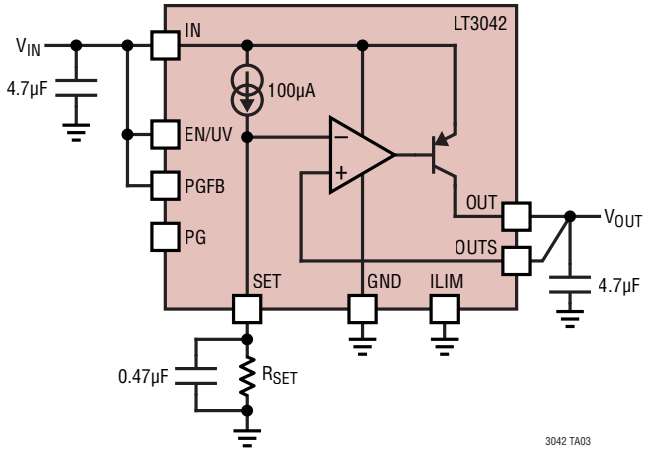
In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to GND, pulled to some intermediate voltage, or left open-circuit. In all of these cases, the reverse current protection circuitry prevents current flow from output to the input. Nonetheless, due to the OUTS-to-SET clamp, unless the SET pin is floating, current can flow to GND through the SET pin resistor as well as up to 15mA to GND through the output overshoot recovery circuitry. This current flow through the output overshoot recovery circuitry can be significantly reduced by placing a Schottky diode between OUTS and SET pins, with its anode at the OUTS pin.

TYPICAL APPLICATIONS

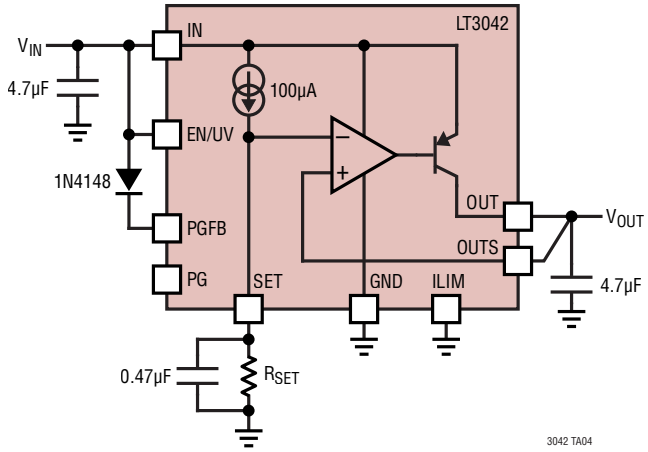
$12V_{IN}$ to $3.3V_{OUT}$ with $0.8\mu V_{RMS}$ Integrated Noise



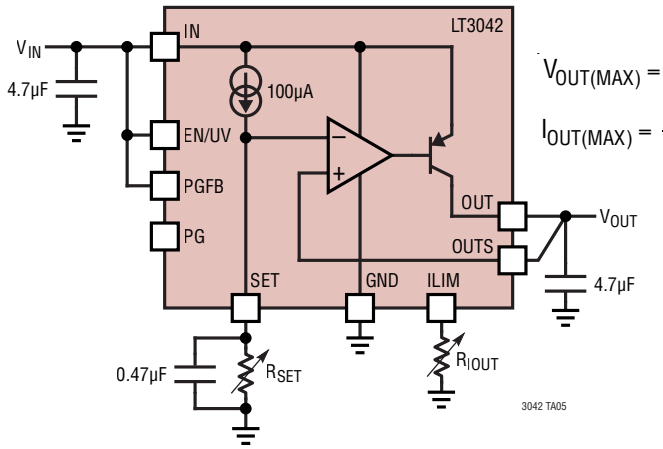
PGFB Disabled without Reverse Input Protection



PGFB Disabled with Reverse Input Protection



Low Noise CC/CV Lab Power Supply

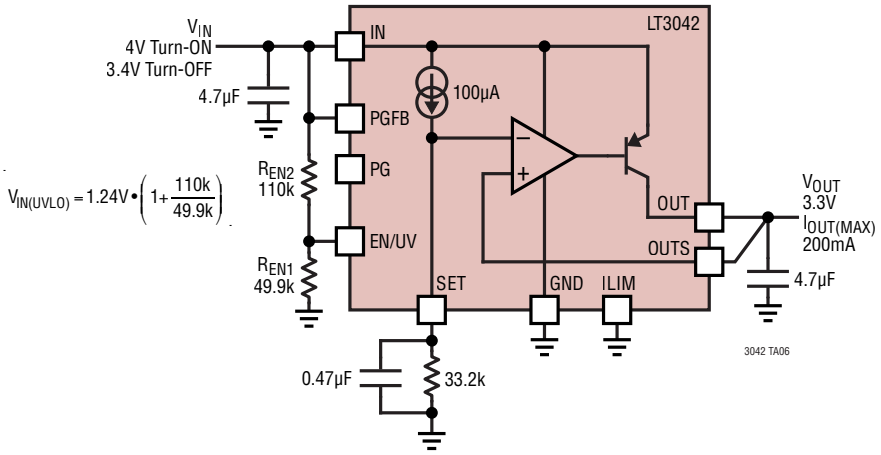


$$V_{OUT(MAX)} = 100\mu A \bullet R_{SET}$$

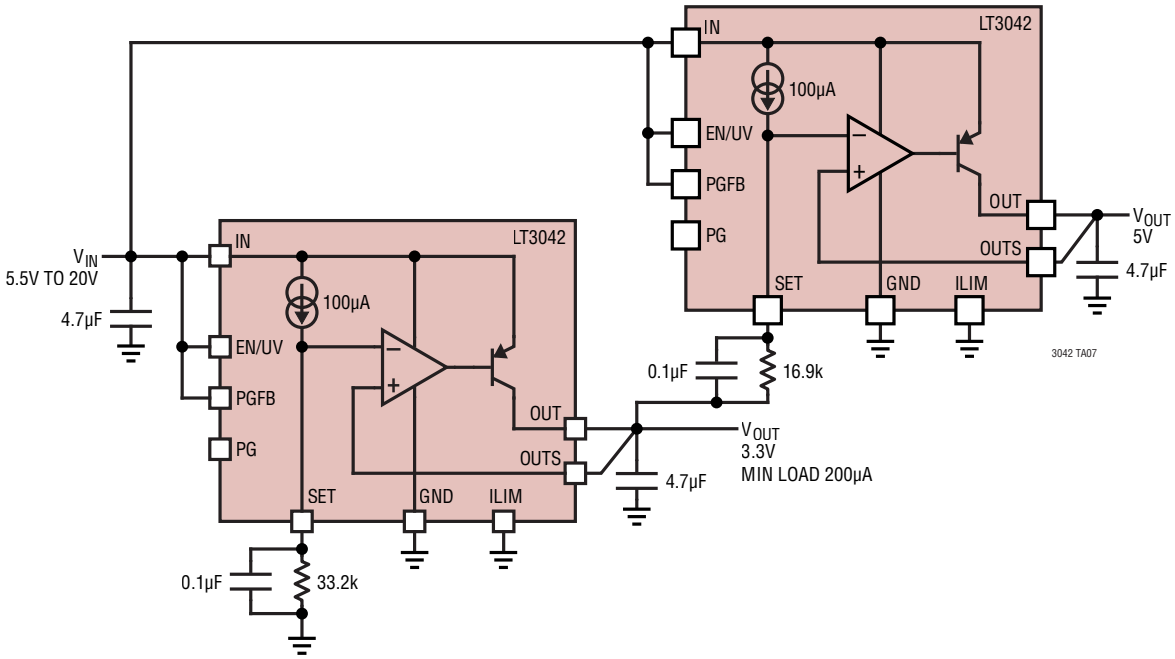
$$I_{OUT(MAX)} = \frac{125mA \bullet k\Omega}{R_{IOUT}}$$

TYPICAL APPLICATIONS

Programming Undervoltage Lockout

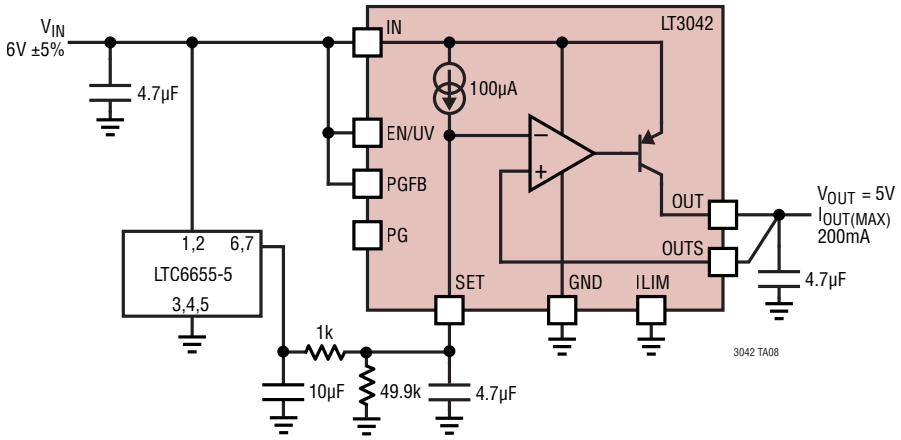


Ratiometric Tracking

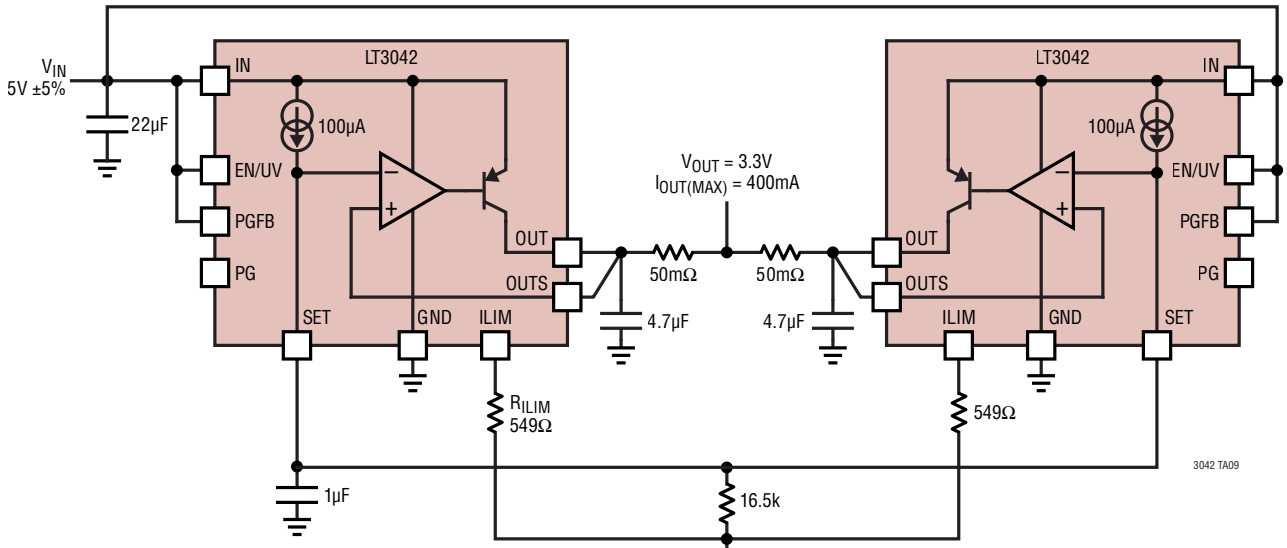


TYPICAL APPLICATIONS

Ultralow 1/f Noise Reference Buffer



Paralleling Multiple Devices Using ILIM (Current Monitor) to Cancel Ballast Resistor Drop



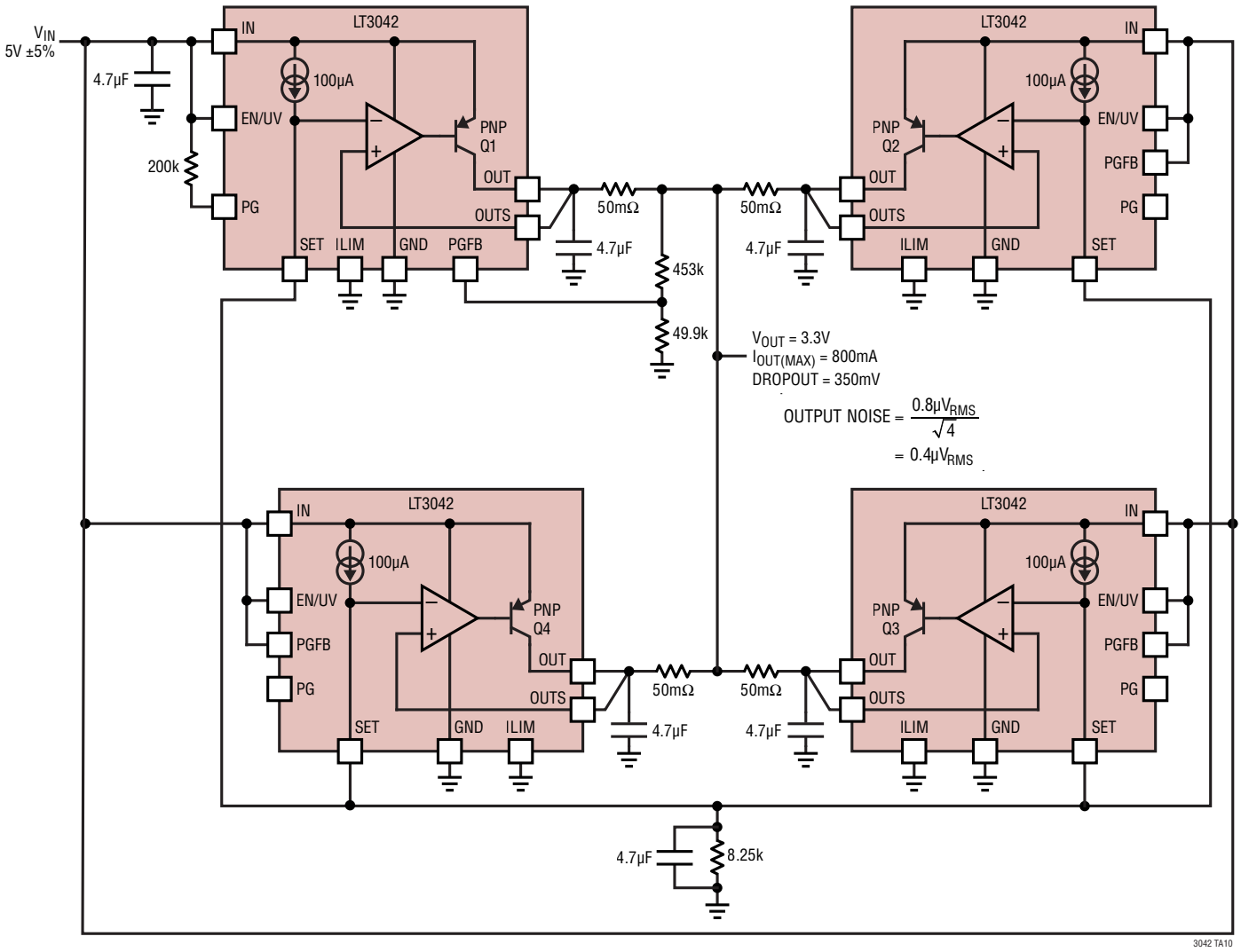
N = NUMBER OF DEVICES IN PARALLEL
R_{CDC} = CABLE (BALLAST RESISTOR) DROP CANCELLATION RESISTOR
R_{ILIM} = CURRENT LIMIT PROGRAMMING RESISTOR
$R_{BALLAST}$ = BALLAST RESISTOR
ILIM = OUTPUT CURRENT LIMIT

R_{ILIM} = 125mA • kΩ/ILIM – R_{CDC} • N
= 549Ω (FOR 200mA ILIM PER REGULATOR)

R_{CDC} = $R_{BALLAST}$ • 400/N
= 10Ω

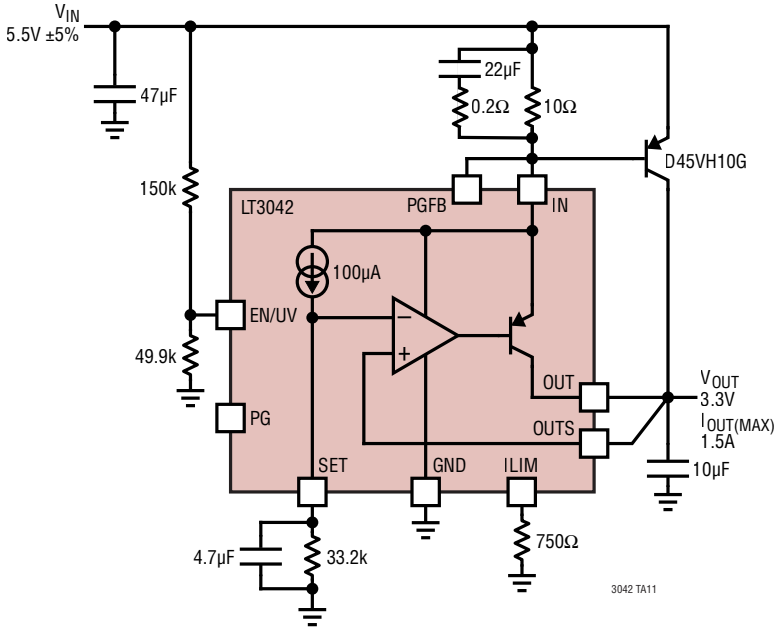
TYPICAL APPLICATIONS

Paralleling Multiple LT3042s for Higher Output Current

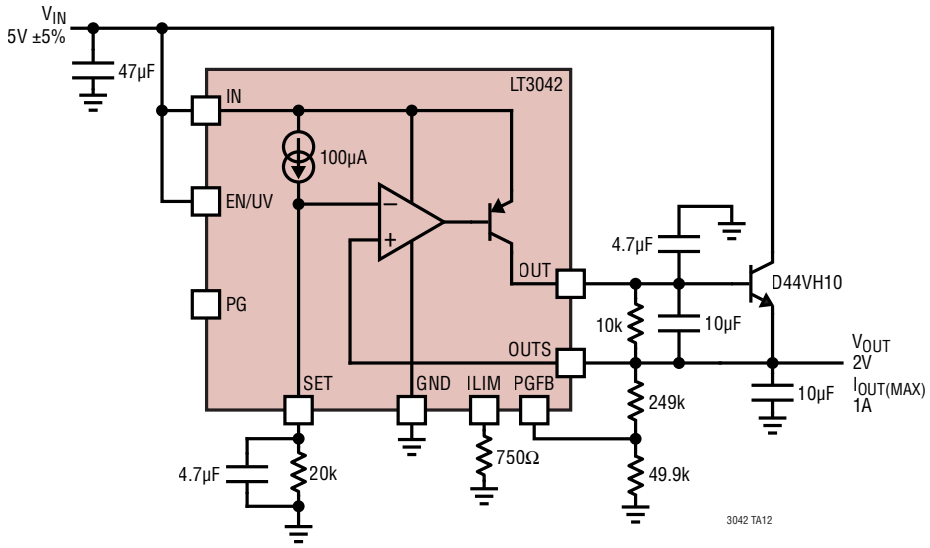


TYPICAL APPLICATIONS

Ultralow Noise Higher Current Regulator with External PNP



Ultralow Noise Higher Current Regulator with External NPN

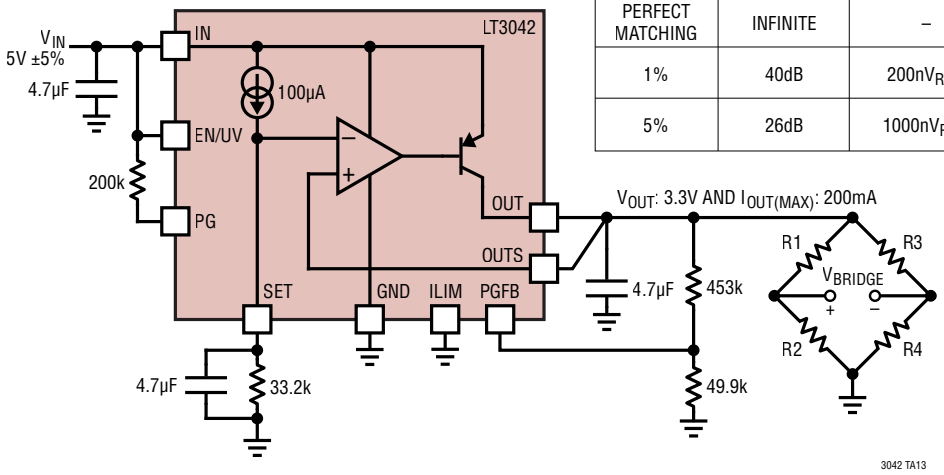


TYPICAL APPLICATIONS

Low Noise Wheatstone Bridge Power Supply

LT1763 NOISE: 20μV_{RMS} (10Hz TO 100kHz)
LT3042 NOISE: 0.8μV_{RMS} (10Hz TO 100kHz)

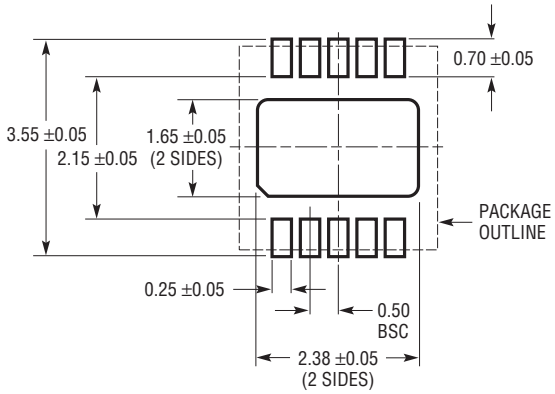
RESISTOR TOLERANCE	BRIDGE PSRR	NOISE AT V_{BRIDGE} USING LT1763	NOISE AT V_{BRIDGE} USING LT3042
PERFECT MATCHING	INFINITE	–	–
1%	40dB	200nV_{RMS}	**8nV_{RMS}**
5%	26dB	1000nV_{RMS}	**42.5nV_{RMS}**



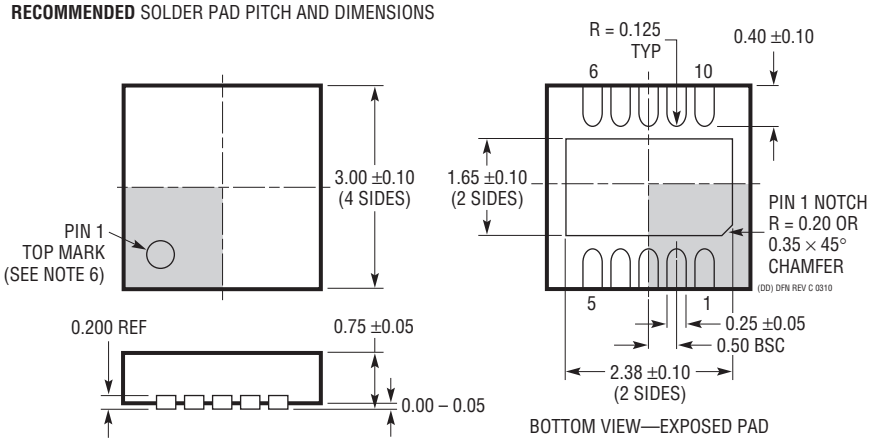
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3042#packaging for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



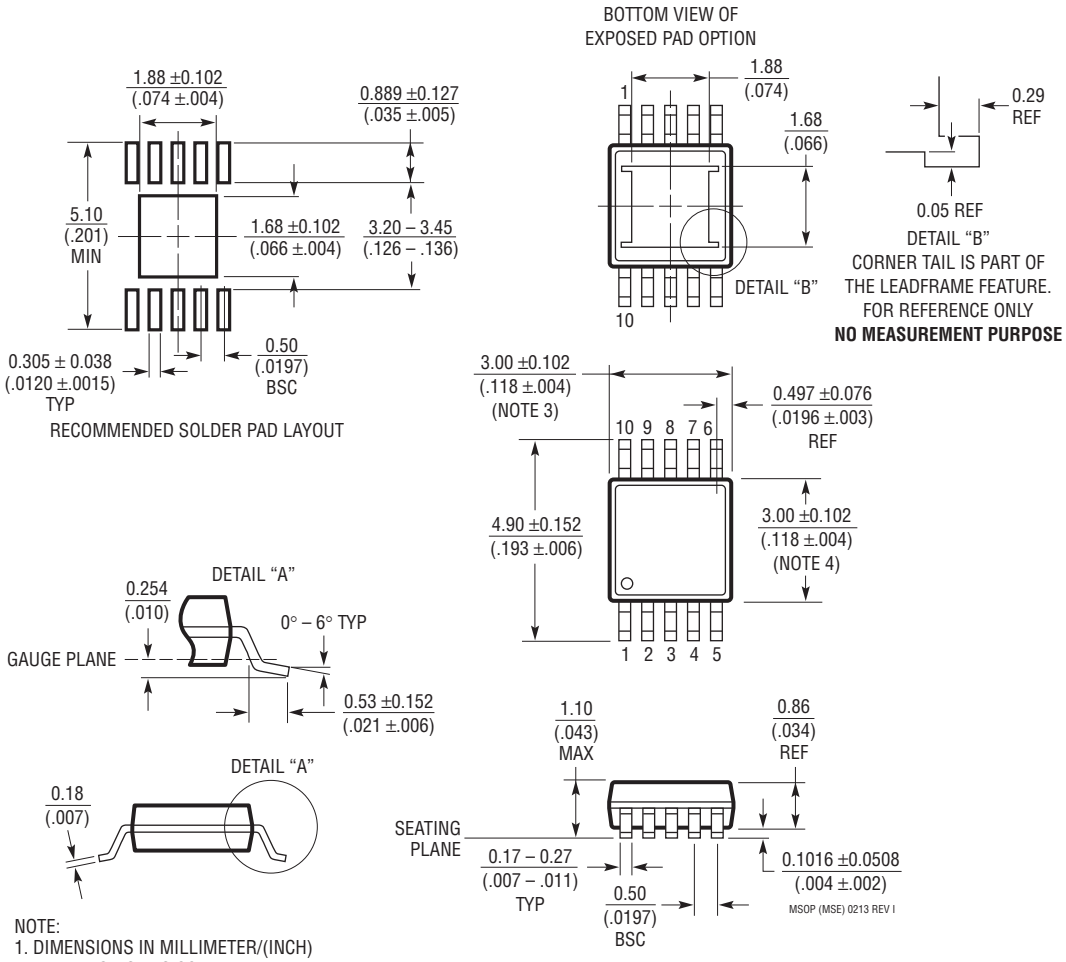
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3042#packaging for the most recent package drawings.

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)



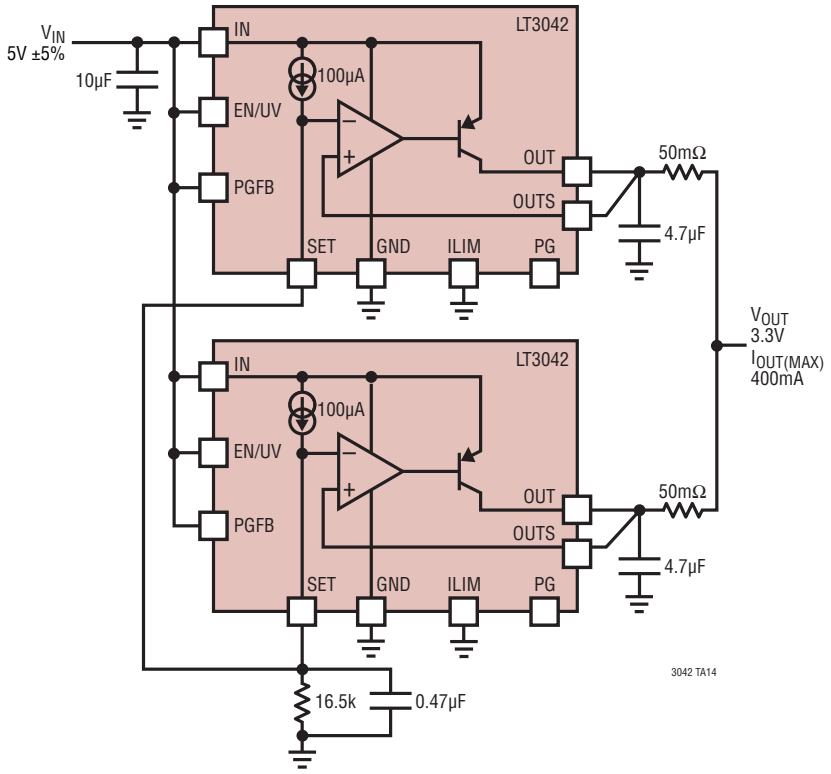
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/15	Updated text in the second paragraph	1
		Updated Line Reg ΔV_{OS}, Change in V_{OS}, Output Noise Spectral Density specs	3
		Updated text to clarify fast start-up test condition	4
		Updated text to clarify Notes 5, 6, and 7	4
		Updated text to clarify Note 10	5
		Updated Graph 10 and Graph 12	6
		Updated conditions on Graph 18 and Graph 24	7
		Updated conditions on Graph 28	8
		Updated title of Graph 40	9
		Updated Output Voltage section	14, 15
		Updated Fast Start-up section	18
		Modified Direct Paralleling for Higher Current section	19
		Updated Typical Application circuit TA02	22
		Added Equation text to the Typical Application circuit TA03	22
		Updated Typical Application circuit TA06 and TA13	24
		Updated text in the Typical Application circuit TA14 and TA07	25
		Updated text in the Typical Application circuit TA08	26
B	11/17	Modified Typical Application schematic.	1
		Removed Ripple Rejection minimum spec in the Electrical Characteristics table.	3
		Modified Start-Up Time conditions in the Electrical Characteristics table.	4
		Revised Graph 37.	9
		Changed scale on Graph 55.	11
		Revised PGFB pin description in the Pin Functions section.	12
		Modified Figure 3, and ‘Output Sensing and Stability’ and ‘Stability and Output Capacitance’ sections.	15
		Added High Vibration Environments section.	16
		Added PSRR + Input Capacitance section.	17
		Revised Externally Programmable Current Limit section.	19
		Revised Figure 8.	20
		Modified Protection Features section.	22

TYPICAL APPLICATION

Parallel Devices



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V
LT1763	500mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, SO-8 Package
LT3050	100mA LDO with Diagnostics and Precision Current Limit	340mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.8V to 45V, 3mm × 2mm DFN and MSOP Packages
LT3060	100mA Low Noise LDO with Soft-Start	300mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.8V to 45V, 2mm × 2mm DFN and ThinSOT Packages
LT3080	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; TO-220, DD-Pak, SOT-223, MSOP and 3mm × 3mm DFN-8 Packages; LT3080-1 Version Has Integrated Internal Ballast Resistor
LT3082	200mA, Parallelable, Low Noise LDO	Outputs May Be Paralleled for Higher Output Current or Heat Spreading, Wide Input Voltage Range: 1.2V to 40V, Low Value Input/Output Capacitors Required: 2.2µF, Single Resistor Sets Output Voltage, 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; MS8E and 2mm × 3mm DFN-6 Packages

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