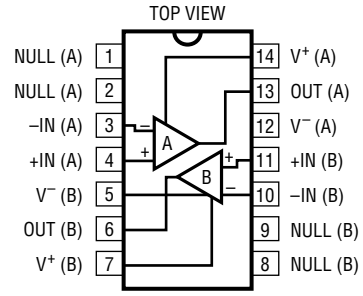
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ..... ±20V
Differential Input Current (Note 2) ..... ±10mA
Input Voltage ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1024AM/LT1024M **(OBSOLETE)**.....–55°C to 125°C
LT1024AC/LT1024C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
14-PIN PDIP
T_{JMAX} = 100°C, θ_{JA} = 100°C/W, θ_{JC} = 60°C/W (N)

NOTE: DEVICE MAY BE OPERATED EVEN IF INSERTION IS REVERSED; THIS IS DUE TO INHERENT SYMMETRY OF PIN LOCATIONS OF AMPLIFIERS A AND B (NOTE 3)

ORDER PART NUMBER
LT1024ACN LT1024CN

D PACKAGE
14-PIN SIDE BRAZED (HERMETIC)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W, θ_{JC} = 60°C/W (D)

ORDER PART NUMBER
LT1024AMD LT1024MD

OBSOLETE PACKAGE
Consider the N14 Package as an Alternate Source

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

Individual Amplifiers. V_S = ±15V, V_{CM} = 0V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M/LT1024C MIN	LT1024M/LT1024C TYP	LT1024M/LT1024C MAX	UNITS
V_{OS}	Input Offset Voltage			15	50		20	100	µV
	Long Term Input Offset Voltage Stability			0.3			0.3		µV/month
I_{OS}	Input Offset Current			20	100		25	180	pA
I_B	Input Bias Current			±25	±120		±30	±200	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μV_{P-P}
e_n	Input Noise Voltage Density	f_O = 10Hz (Note 4) f_O = 1000Hz (Note 4)		17 14	33 24		17 14	33 24	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz		20			20		fA/√Hz
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L ≥ 10kΩ V_{OUT} = ±10V, R_L ≥ 2kΩ	250 150	2000 1000		180 100	2000 1000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = ±13.5V	112	132		108	132		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±20V	112	132		108	132		dB
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
V_{OUT}	Output Voltage Swing	R_L = 10kΩ	±13	±14		±13	±14		V
	Slew Rate		0.1	0.2		0.1	0.2		V/µs
I_S	Supply Current per Amplifier			380	600		380	700	µA

ELECTRICAL CHARACTERISTICS

Matching Specifications. V_S = ±15V, V_{CM} = 0V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M /LT1024C MIN	LT1024M /LT1024C TYP	LT1024M /LT1024C MAX	UNITS
	Input Offset Voltage Match			20	75		25	150	µV
I_B^+	Average Noninverting Bias Current			±30	±150		±40	±250	pA
I_{OS}^+	Noninverting Offset Current			30	150		30	300	pA
ΔCMRR	Common Mode Rejection Ratio Match	V_{CM} = ±13.5V	110	132		106	132		dB
ΔPSRR	Power Supply Rejection Ratio Match	V_S = ±2V to 20V	110	132		106	132		dB
	Channel Separation	f ≤ 10Hz (Note 4)	134	150		134	150		dB

Individual Amplifiers. The ● denotes the specifications which apply over the full operating temperature range of 0°C ≤ T_A = 70°C for the LT1024AC and LT1024C; –55°C ≤ T_A ≤ 125°C for the LT1024AM and LT1024M. V_S = ±15V, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M/LT1024C MIN	LT1024M/LT1024C TYP	LT1024M/LT1024C MAX	UNITS
V_{OS}	Input Offset Voltage	0°C to 70°C –55°C to 125°C	● ●		30 40	120 200		35 50	200 300	µV µV
	Average Temperature Coefficient of Input Offset Voltage		●		0.25	1.5		0.3	2.0	µV/°C
I_{OS}	Input Offset Current	0°C to 70°C –55°C to 125°C	● ●		40 80	250 350		50 100	300 500	pA pA
	Average Temperature Coefficient of Input Offset Current		●		0.5	2.5		0.7	3	pA/°C
I_B	Input Bias Current	0°C to 70°C –55°C to 125°C	● ●		±40 ±100	±250 ±700		±50 ±200	±400 ±1300	pA pA
	Average Temperature Coefficient of Input Bias Current	0°C to 70°C –55°C to 125°C	● ●		0.4 1	3 6		0.5 2	4 12	pA/°C pA/°C
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L ≥ 10kΩ V_{OUT} = ±10V, R_L ≥ 2kΩ	● ●	150 100	1000 600		150 100	1000 600		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = ±13.5V	●	108	128		106	128		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±18V	●	108	128		106	128		dB
	Input Voltage Range		●	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	R_L = 10kΩ	●	±13	±14		±13	±14		V
I_S	Supply Current		●		400	800		400	900	µA

ELECTRICAL CHARACTERISTICS

Matching Specifications. The ● denotes the specifications which apply over the temperature range of 0°C ≤ T_A = 70°C for the LT1024AC and LT1024C; –55°C ≤ T_A ≤ 125°C for the LT1024AM and LT1024M, V_S = ±15V, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M/LT1024C MIN	LT1024M/LT1024C TYP	LT1024M/LT1024C MAX	UNITS
	Input Offset Voltage Match	0°C to 70°C –55°C to 125°C	● ●		35 50	170 280		45 70	300 500	µV µV
	Input Offset Voltage Tracking		●		0.3	2		0.4	3.5	µV/°C
I_B^+	Average Noninverting Bias Current	0°C to 70°C –55°C to 125°C	● ●		±40 ±100	±300 ±800		±50 ±200	±500 ±1400	pA pA
I_{OS}^+	Noninverting Offset Current	0°C to 70°C –55°C to 125°C	● ●		40 80	300 800		50 150	500 1500	pA pA
ΔCMRR	Common Mode Rejection Ratio Match	V_{CM} = ±13.5V	●	106	128		104	128		dB
ΔPSRR	Power Supply Rejection Ratio Match	V_S = ±2.5V to ±18V	●	106	128		104	128		dB

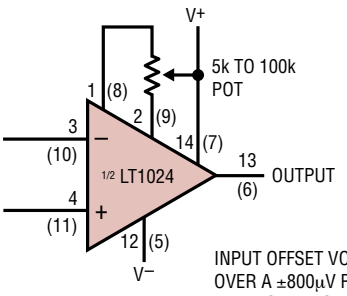
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 3: The V^+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V^- supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V^- pins should be used.

Note 4: This parameter is tested on a sample basis only.

Optional Offset Nulling Circuit

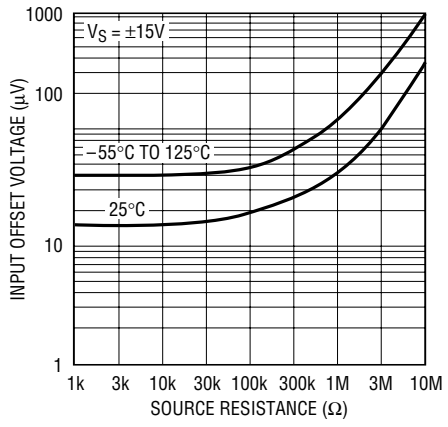


INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±800µV RANGE WITH A 5k TO 100k POTENTIOMETER

LT1024 • EC01

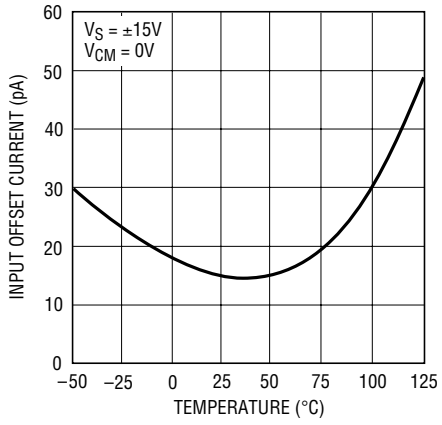
TYPICAL PERFORMANCE CHARACTERISTICS

Offset Voltage vs Source Resistance (Balanced or Unbalanced)



LT1024 • TPC01

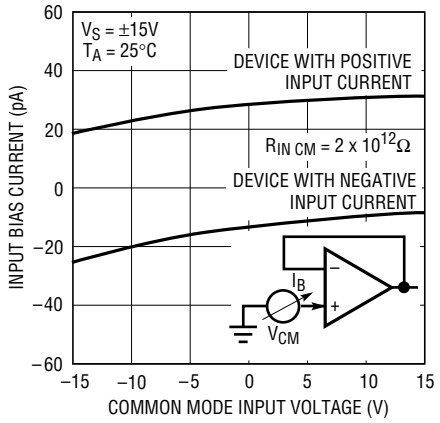
Input Offset Current vs Temperature



LT1024 • TPC02

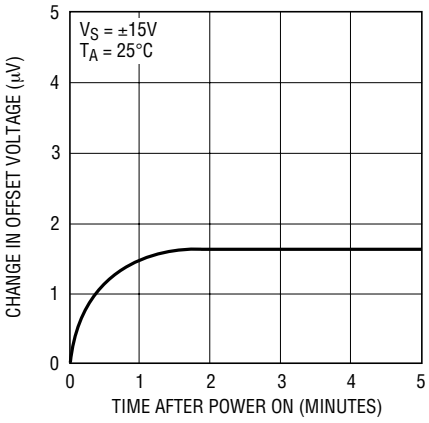
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current Over Common Mode Range



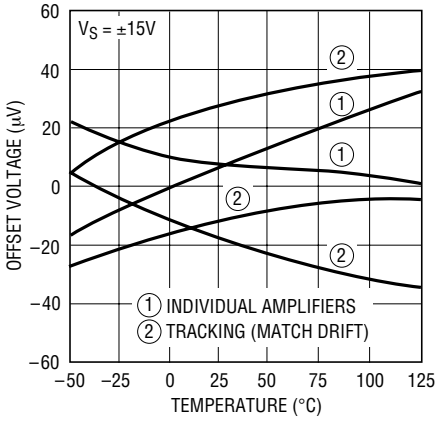
LT1024 • TPC03

Warm-Up Drift



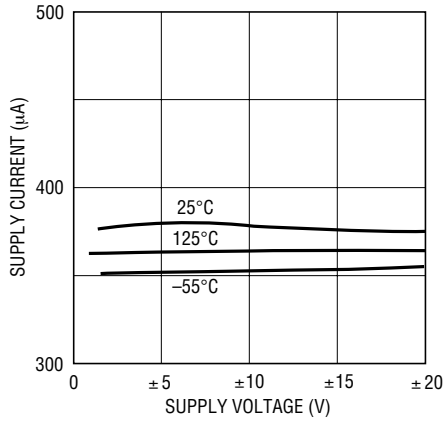
LT1024 • TPC04

Offset Voltage Drift and Tracking with Temperatures of Representative Units



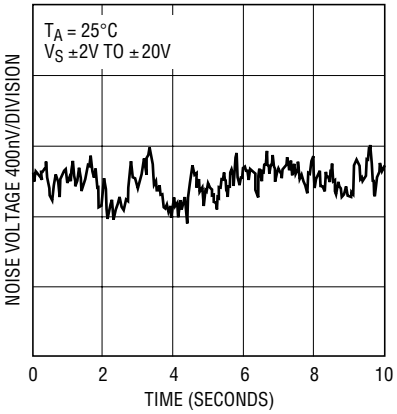
LT1024 • TPC05

Supply Current vs Supply Voltage per Amplifier



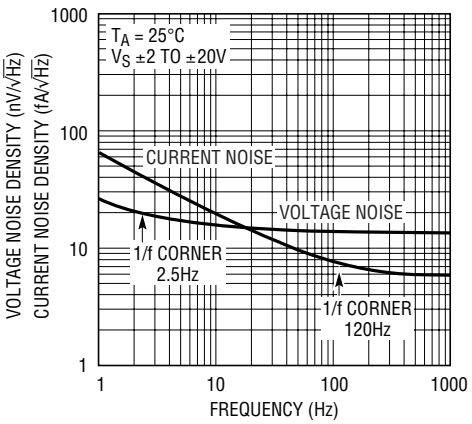
LT1024 • TPC06

0.1Hz to 10Hz Noise



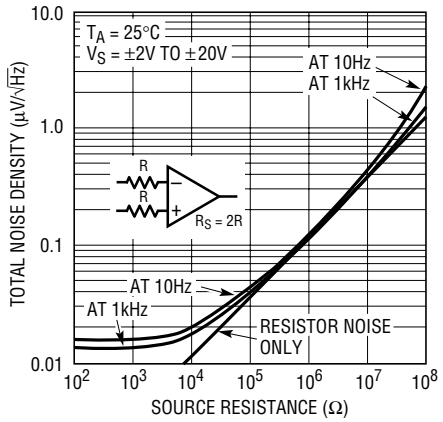
LT1024 • TPC07

Noise Spectrum



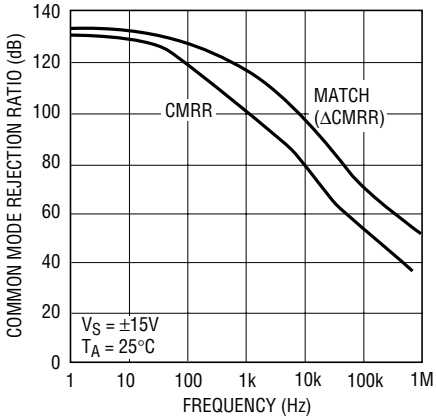
LT1024 • TPC08

Total Noise vs Source Resistance



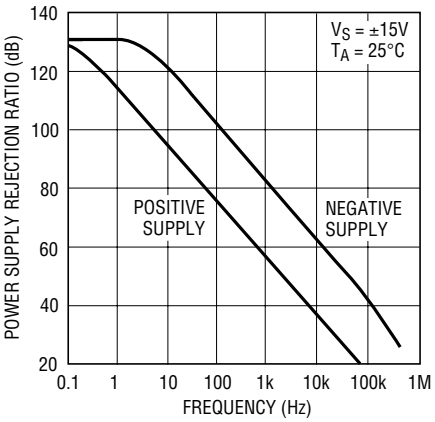
LT1024 • TPC09

Common Mode Rejection and CMRR Match vs Frequency



LT1024 • TPC10

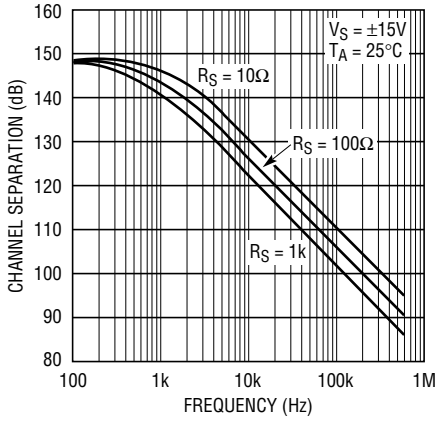
Power Supply Rejection vs Frequency



LT1024 • TPC11

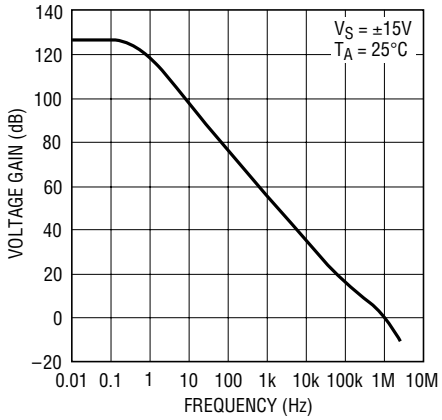
TYPICAL PERFORMANCE CHARACTERISTICS

Channel Separation vs Frequency



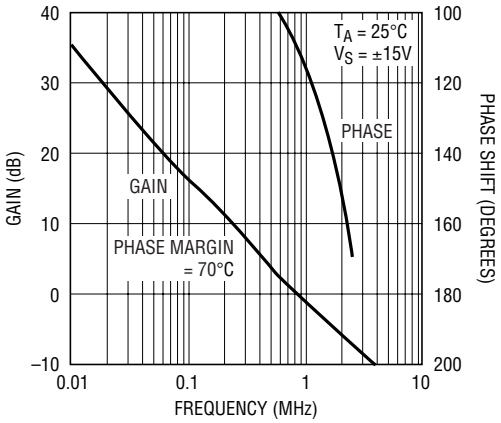
LT1024 • TPC12

Voltage Gain vs Frequency



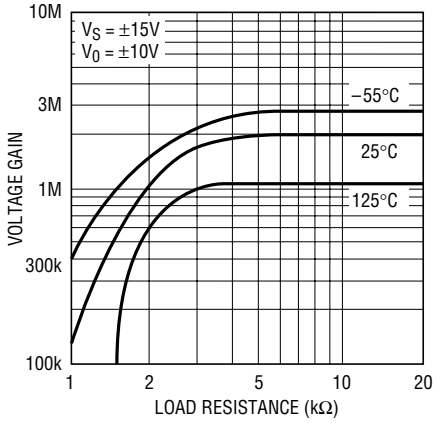
LT1024 • TPC13

Gain, Phase Shift vs Frequency



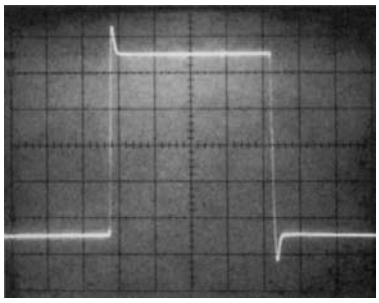
LT1024 • TPC14

Voltage Gain vs Load Resistance



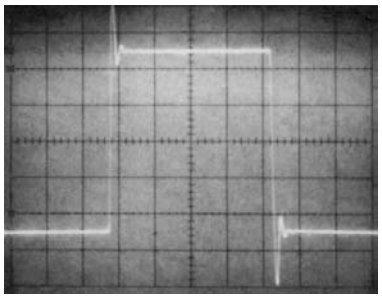
LT1024 • TPC15

Small-Signal Transient Response



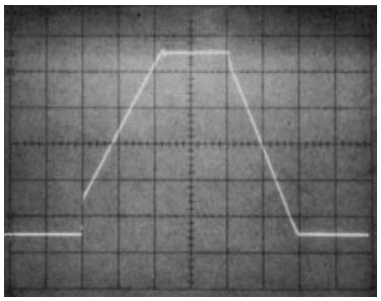
A_V = +1 5µs/DIV
C_{LOAD} = 100pF

Small-Signal Transient Response



A_V = +1 5µs/DIV
C_{LOAD} = 1000pF

Large-Signal Transient Response



A_V = +1 20µs/DIV

APPLICATIONS INFORMATION

The LT1024 may be inserted directly into OP-10, OP-207 or OP227 sockets with or without removal of external nulling components.

The LT1024 is specified over a wide range of power supply voltages from ±2V to ±18V. Operation with lower supplies is possible down to ±1.2V (two NiCad batteries).

Advantages of Matched Dual Op Amps

In many applications, the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references, and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1024. This error cancellation principle holds for a considerable number of input-referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two noninverting input currents (I_B^+). The difference between these two currents (I_{OS}^+) is the offset current of the instrumentation amplifier. Common mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

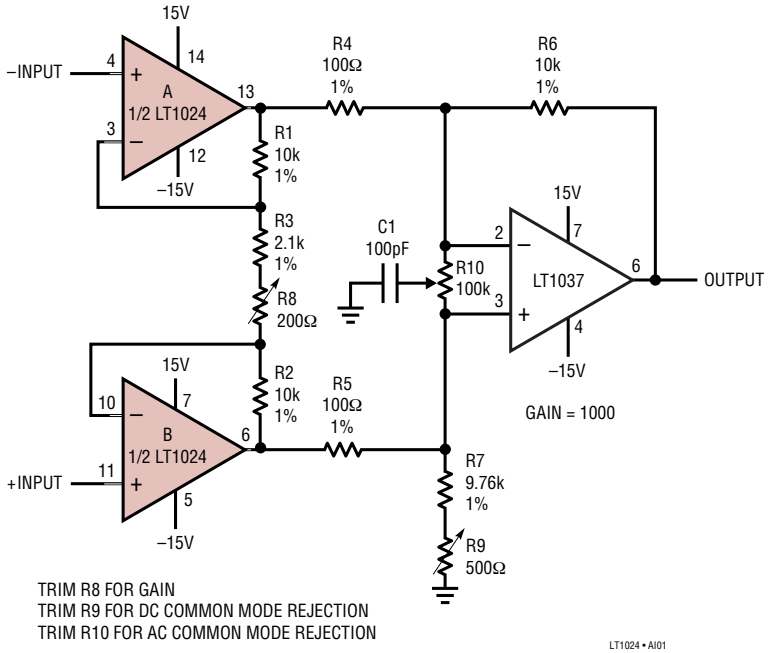
The concepts of common mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $CMRR_A$ = +1.0μV/V or 120dB
and $CMRR_B$ = +0.5μV/V or 126dB,
then ΔCMRR = 0.5μV/V or 126dB
if $CMRR_B$ = −0.5μV/V, which is still 126dB,
then ΔCMRR = 1.5μV/V or 116.5dB.

Typical performance of the instrumentation amplifier:
Input offset voltage = 25μV.
Input bias current = 30pA.
Input resistance = $10^{12}\Omega$.
Input offset current = 30pA.
Input noise = 0.7μV_{P-P}.
Power bandwidth (V_O = ±10V) = 80kHz.

Clearly, the LT1024, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.

Three Op Amp Instrumentation Amplifier



APPLICATIONS INFORMATION

Achieving Picoampere/Microvolt Performance

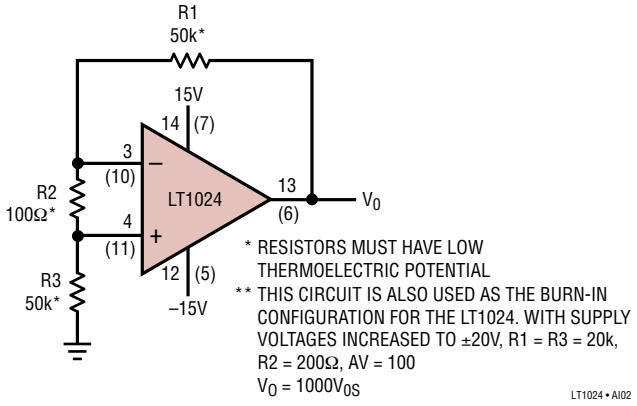
In order to realize the picoampere/microvolt level accuracy of the LT1024, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations, the guard ring should be tied to ground; in noninverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the offset trim terminals can affect offset voltage and drift with temperature.

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

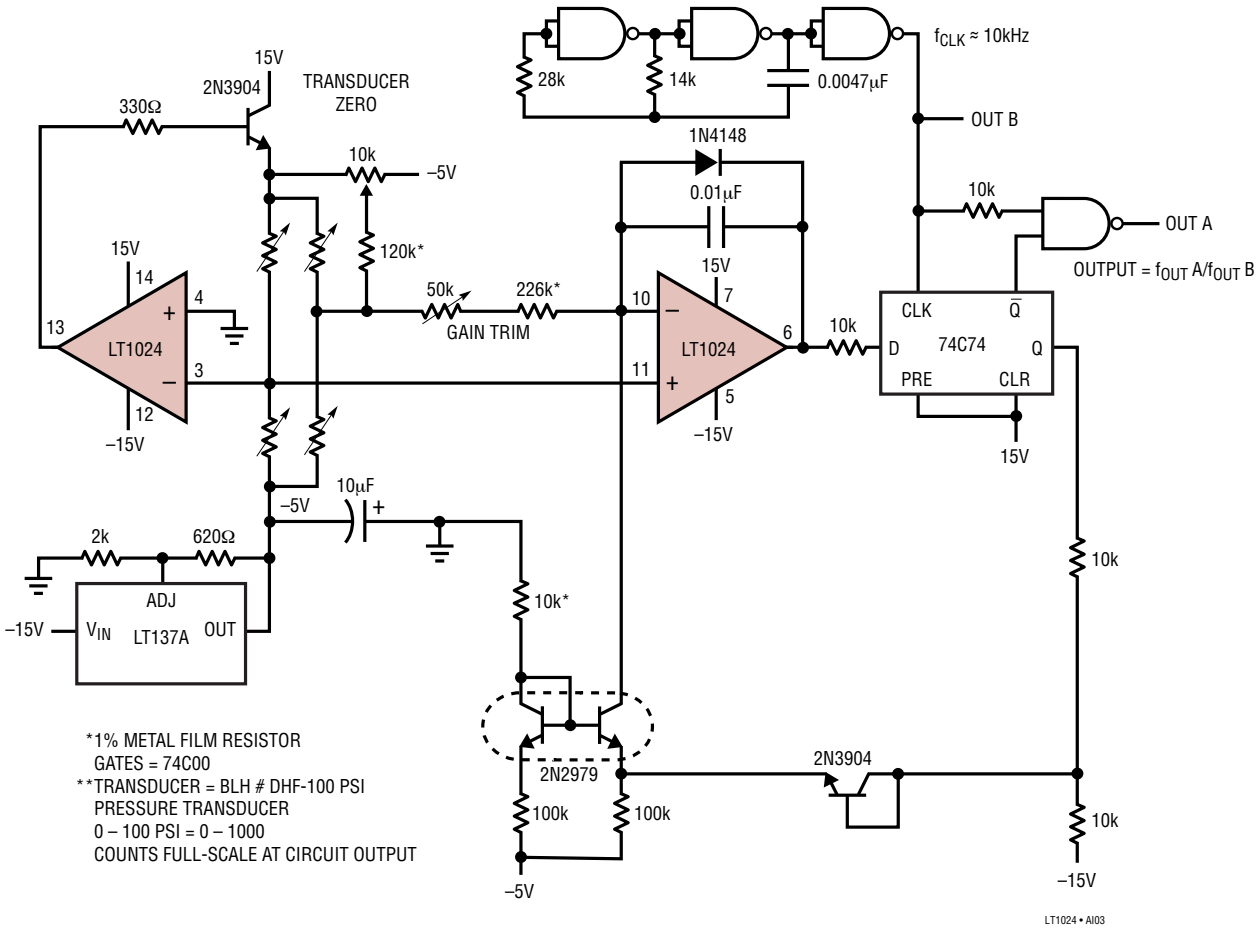
Teflon is a trademark of Dupont.

Test Circuit for Offset Voltage and its Drift with Temperature



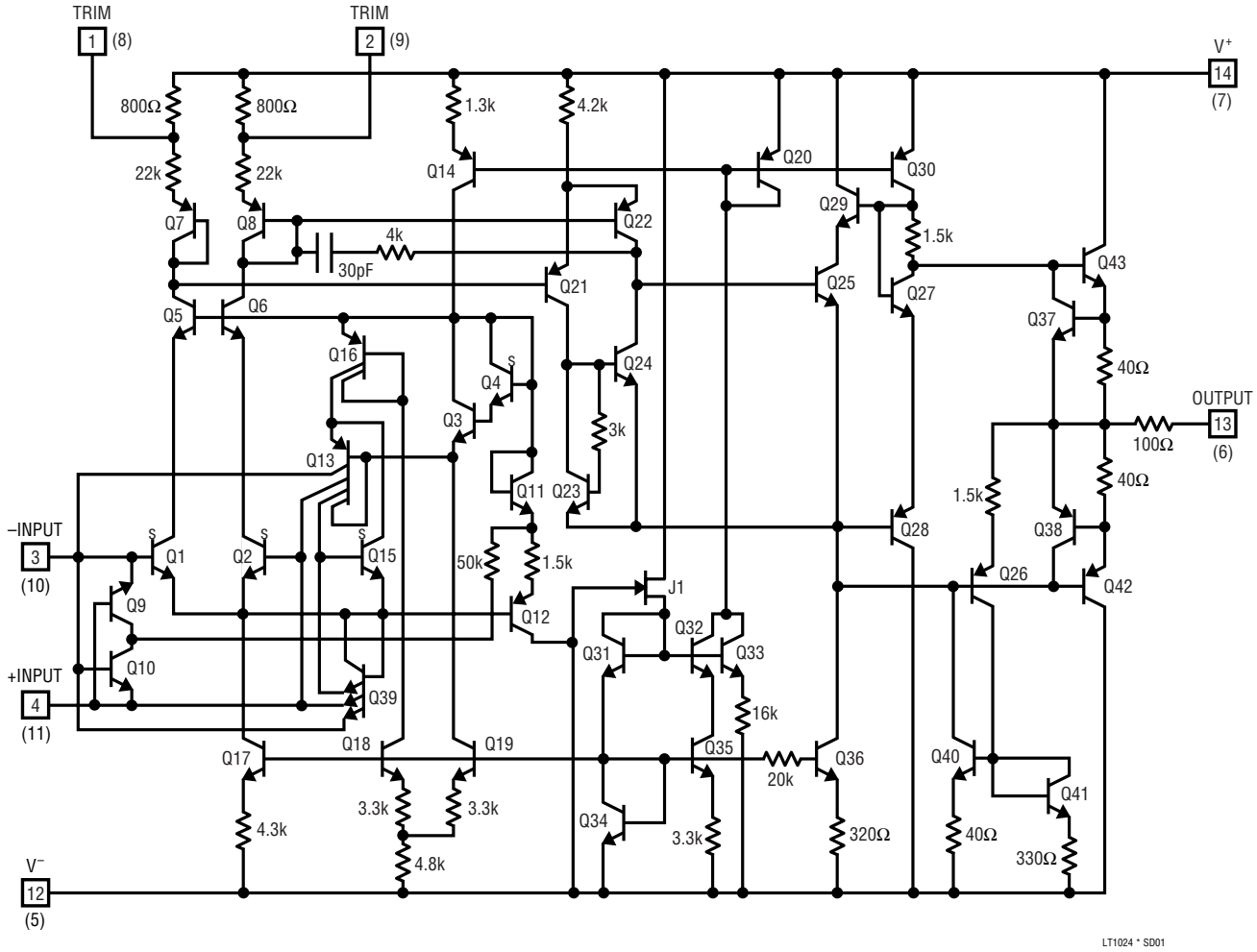
APPLICATIONS INFORMATION

Direct Pressure Transducer to Digital Output Signal Conditioner



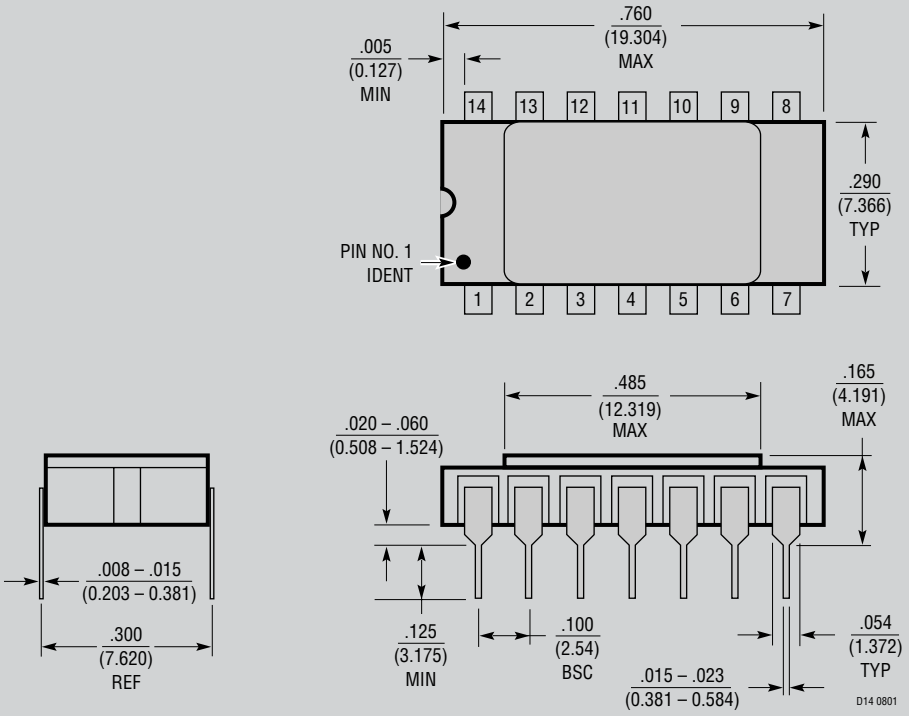
SCHEMATIC DIAGRAM

1/2 LT1024



PACKAGE DESCRIPTION

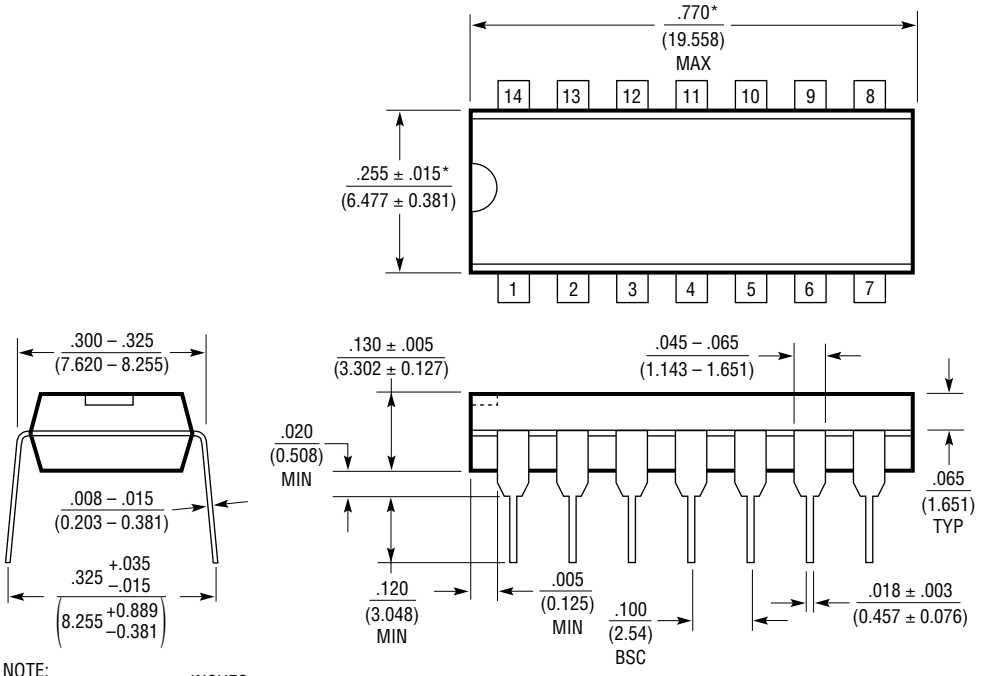
D Package
14-Lead Side Brazed (Hermetic)
(Reference LTC DWG # 05-08-1210)



OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N Package
14-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1884	Picoamp Input, Precision Op Amp	Rail-to-Rail Output

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LW/TP 1002 1K REV A • PRINTED IN USA