

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.13	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.077	Ω	V _{GS} = 10V, I _{D2} = 20A ④
		—	—	0.125		V _{GS} = 10V, I _{D1} = 28A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
G _{fs}	Forward Transconductance	9.1	—	—	S	V _{DS} = 15V, I _{D2} = 20A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	59	nC	I _{D1} = 28A
Q _{GS}	Gate-to-Source Charge	—	—	16		V _{DS} = 50V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	30.7		V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	—	21	ns	V _{DD} = 50V
t _r	Rise Time	—	—	105		I _{D1} = 20A
t _{d(off)}	Turn-Off Delay Time	—	—	64		R _G = 9.1Ω
t _f	Fall Time	—	—	65		V _{GS} = 10V
L _S + L _D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package)
C _{iss}	Input Capacitance	—	1600	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	550	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	120	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	28	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	112		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 28A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	400	ns	T _J = 25°C, I _F = 28A, V _{DD} ≤ 30V
Q _{rr}	Reverse Recovery Charge	—	—	2.9	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	1.0	°C/W
R _{θCS}	Case -to-Sink	—	0.21	—	
R _{θJA}	Junction-to-Ambient (Typical socket mount)	—	—	48	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 25V, starting T_J = 25°C, L = 0.64mH, Peak I_L = 28A, V_{GS} = 10V.
- ③ I_{SD} ≤ 28A, di/dt ≤ 170A/μs, V_{DD} ≤ 100V, T_J ≤ 150°C.
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

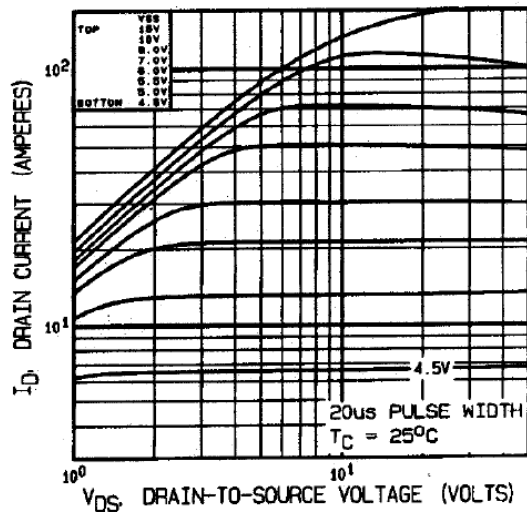


Fig 1. Typical Output Characteristics

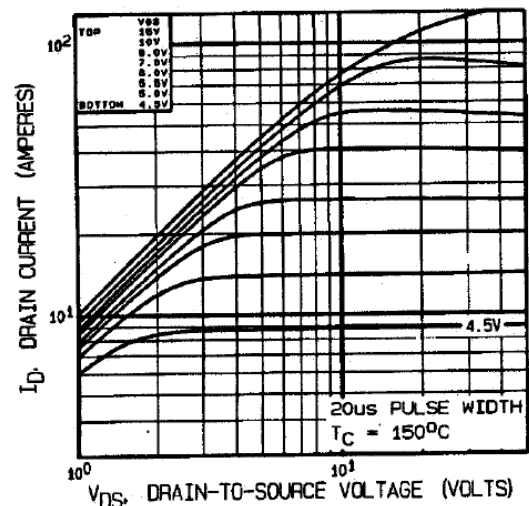


Fig 2. Typical Output Characteristics

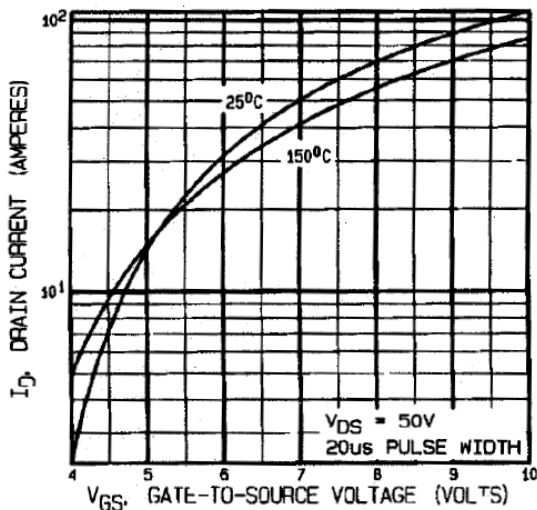


Fig 3. Typical Transfer Characteristics

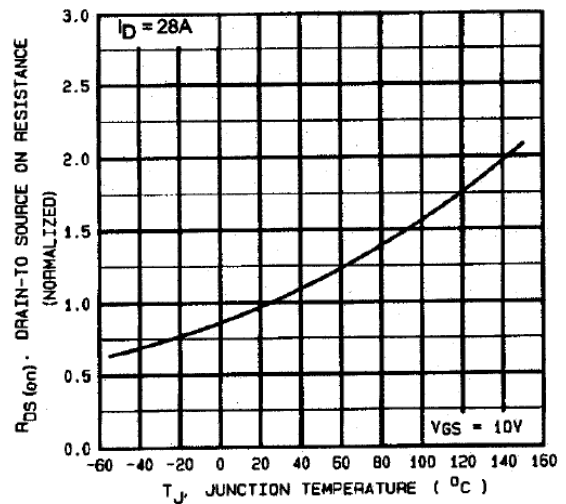


Fig 4. Normalized On-Resistance Vs. Temperature

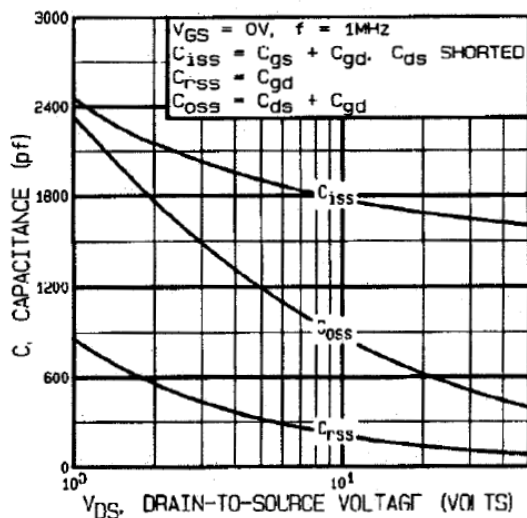


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

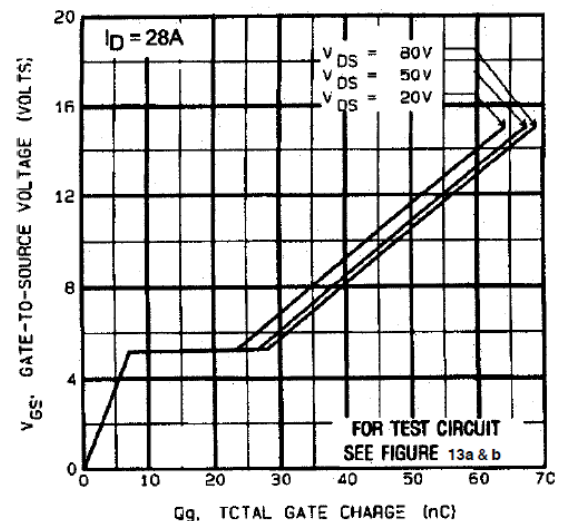


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

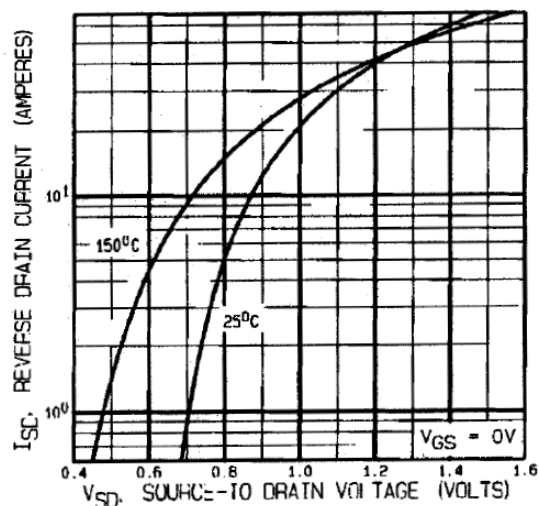


Fig 7. Typical Source-Drain Diode Forward Voltage

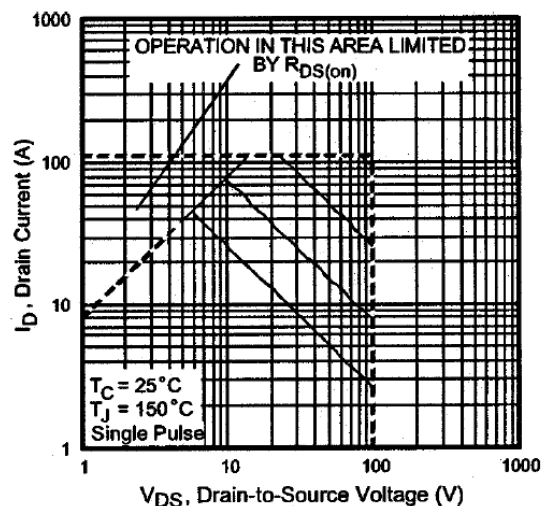


Fig 8. Maximum Safe Operating Area

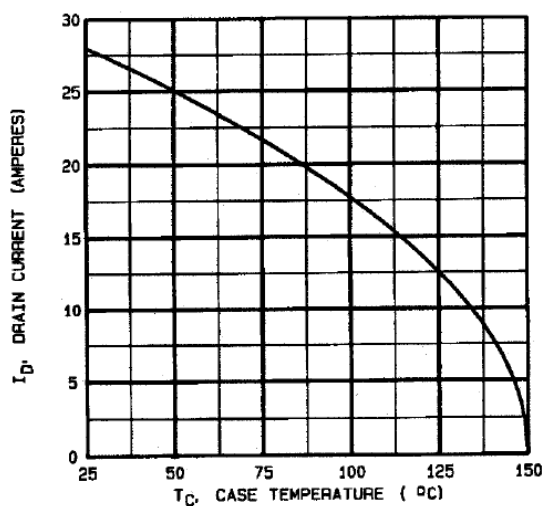


Fig 9. Maximum Drain Current Vs. Case Temperature

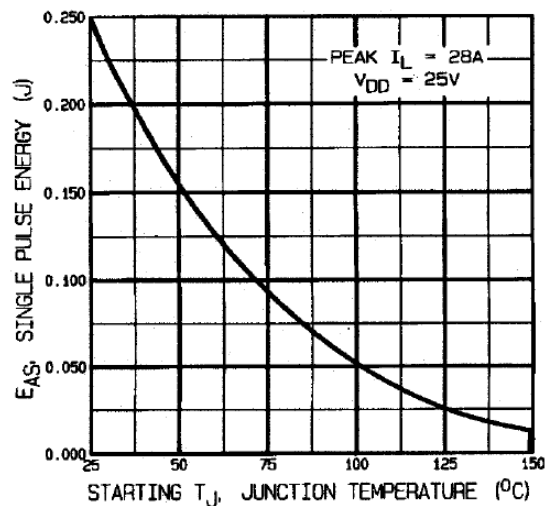


Fig 10. Maximum Avalanche Energy Vs. Drain Current

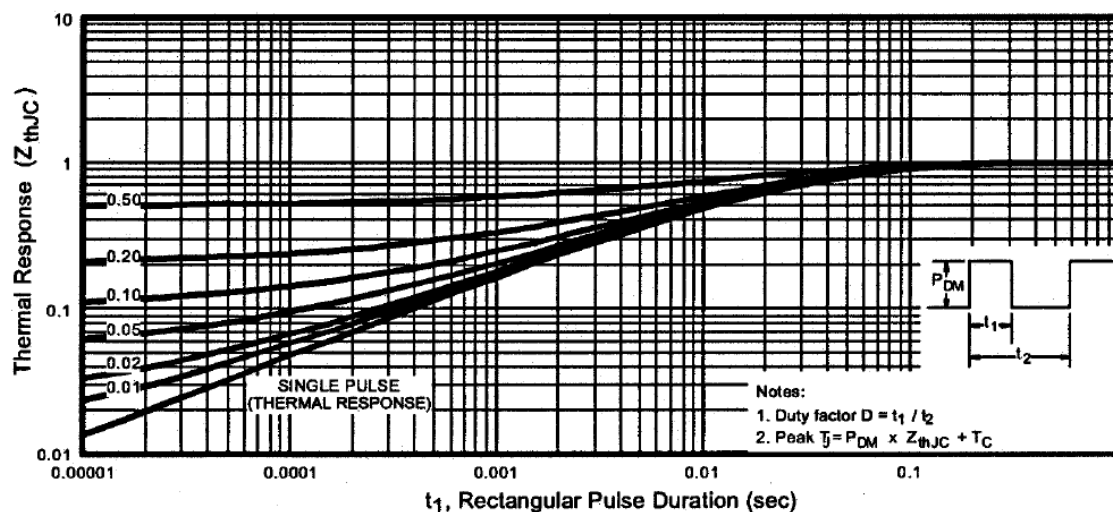


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

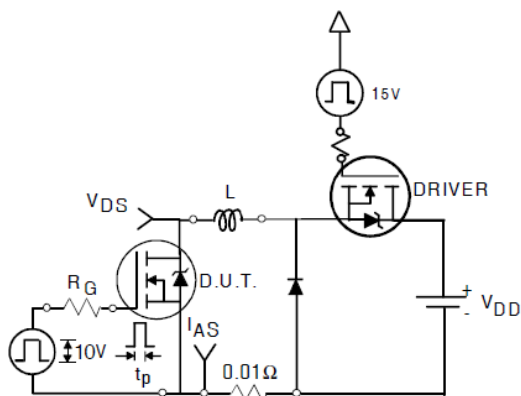


Fig 12a. Unclamped Inductive Test Circuit

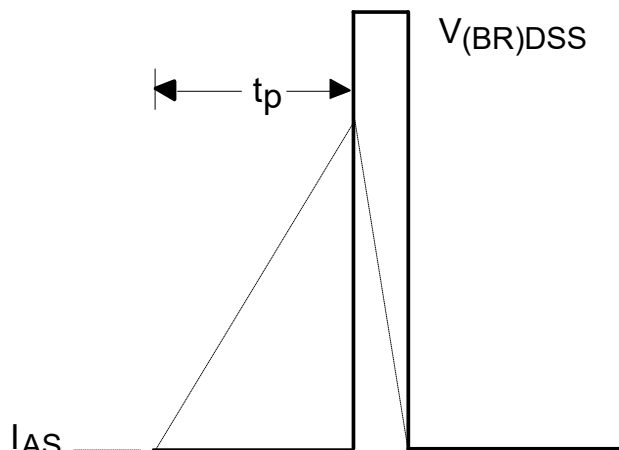


Fig 12b. Unclamped Inductive Waveforms

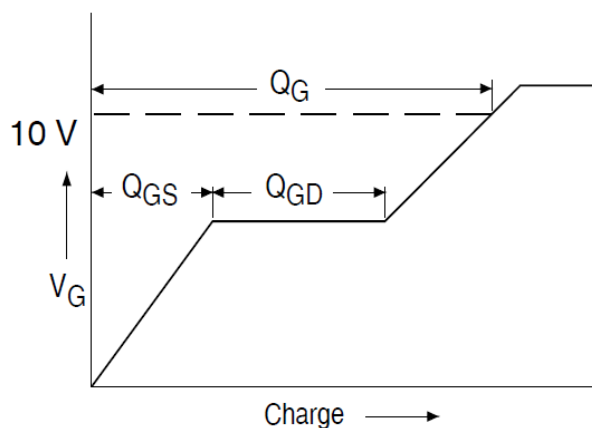


Fig 13a. Gate Charge Waveform

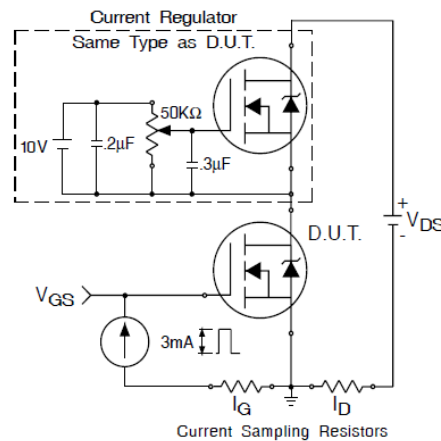


Fig 13b. Gate Charge Test Circuit

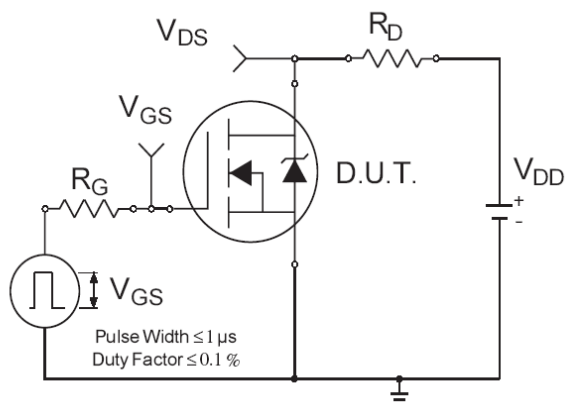


Fig 14a. Switching Time Test Circuit

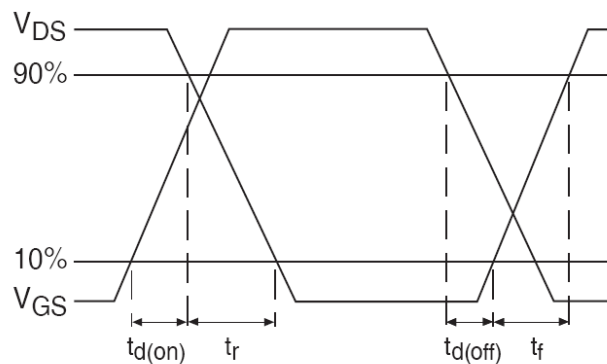
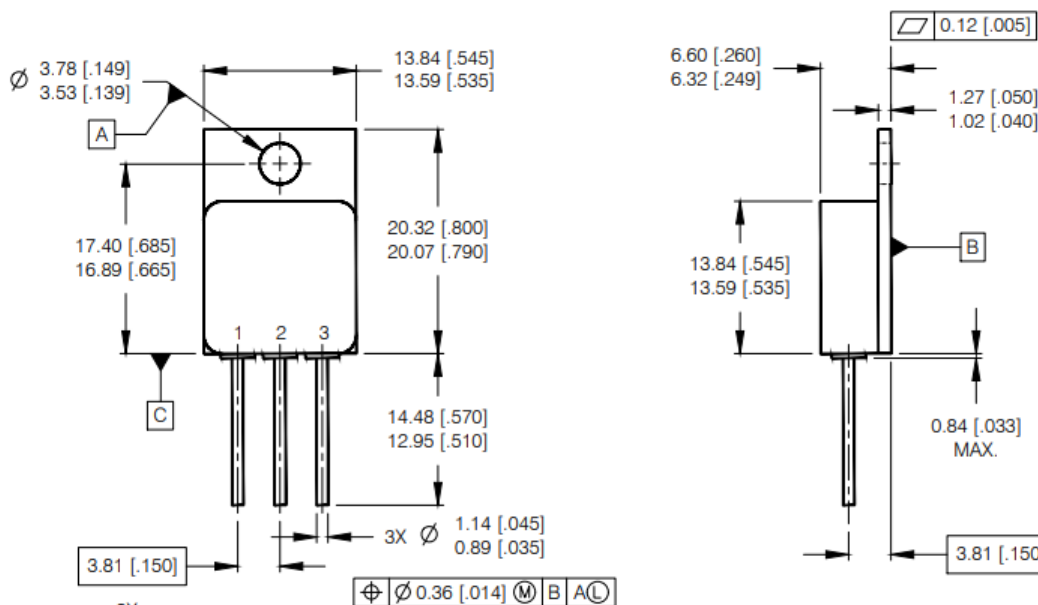


Fig 14b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: TO-254AA

Case Outline and Dimensions - Low-Ohmic TO-254AA

REV.	DESCRIPTION	ECN	DATE
A	INITIAL RELEASE	1120_ER6904	4-3-20



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.
5. FINAL LEAD FINISH IS SOLDER ALLOY 63%Sn 37%Pb.
6. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

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TITLE: TO-254AA PACKAGE OUTLINE (STD & LOW OHMIC)	
DRAWING NO. D100720G-WEB	REV A

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

IR HiRel
An Infineon Technologies Company

www.infineon.com/irhirel

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Data and specifications subject to change without notice.

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