Microprocessor Voltage Monitor with Dual Over/Undervoltage Detection

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1) .....-0.3V to +18V
Output Voltages OUT1 and OUT2
(with respect to GND) (Note 1) .....-0.3V to +18V
Output Voltages HYST1 and HYST2
(with respect to V+) (Note 1) .....+0.3V to -18V
Input Voltages SET1 and SET2
(Note 1).....(GND - 0.3V) to (V+ + 0.3V)
Maximum Sink Output Current
OUT1 and OUT2.....25mA
Maximum Source Output Current
HYST1 and HYST2 .....-25mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW
TO-99 (derate 6.67mW/°C above +70°C) 533mW
Operating Temperature Ranges
ICL7665C_ _.....0°C to +70°C
ICL7665I_ _.....-20°C to +85°C
ICL7665E_ _.....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V+ + 0.3V) or less than (GND - 0.3V) may cause destructive latchup. For this reason, we recommend that inputs from external sources that are not operating from the same power supply **not** be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+	ICL7665	T_A = +25°C		1.6		16	V
			T_A = T_{MIN} to T_{MIN}		1.8		16	
		ICL7665A	T_A = T_{MIN} to T_{MIN}		2.0		16	
		ICL7665B	T_A = +25°C		1.6		10	
			T_A = T_{MIN} to T_{MIN}		1.8		10	
Supply Current	I+	GND ≤ V_{SET1}, V_{SET2} ≤ V+, all outputs open circuit	ICL7665, T_A = +25°C; ICL7665A, T_A = T_{MIN} to T_{MAX}	V+ = 2V		2.5	10	µA
				V+ = 9V		2.6	10	
				V+ = 15V		2.9	15	
			ICL7665B, T_A = +25°C	V+ = 2V		2.5	10	
				V+ = 9V		2.6	10	
Input Trip Voltage	V_{SET}	ICL7665, ICL7665B, T_A = +25°C		V_{SET1}	1.150	1.300	1.450	V
				V_{SET2}	1.200	1.300	1.400	
		ICL7665A, T_A = +25°C		V_{SET1}	1.275	1.300	1.325	
				V_{SET2}	1.225	1.300	1.375	
		ICL7665A, T_A = T_{MIN} to T_{MAX}		V_{SET1}	1.250	1.300	1.350	
				V_{SET2}	1.215	1.300	1.385	
V_{SET} Tempco						100		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}		R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1MΩ				0.004		%/V

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, T_A = +25°C, unless otherwise noted.)

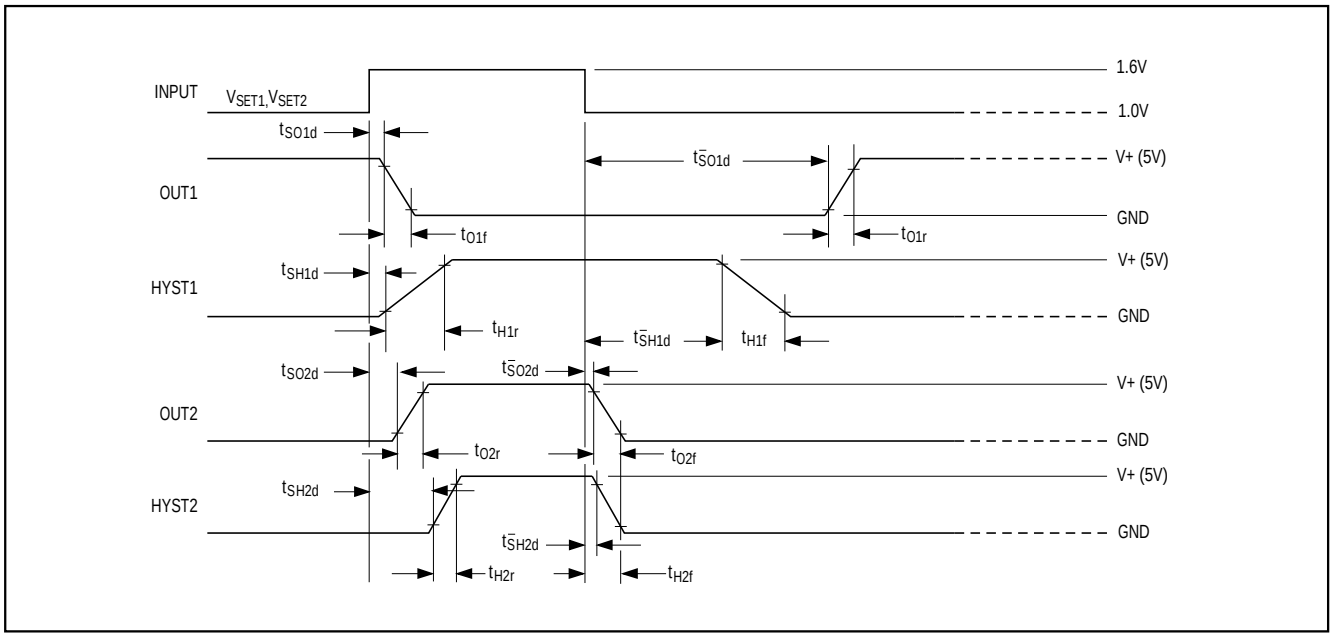
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Leakage Current	I_{OLK}, I_{HLK}	All grades, V_{SET} = 0V or $V_{SET} \geq$ 2V, T_A = +25°C	OUT1, OUT2		10	200	nA
			HYST1, HSYT2		-10	-100	
		ICL7665, ICL7665A, V+ = 15V, $T_A = T_{MIN}$ to T_{MAX}	OUT1, OUT2			2000	
			HYST1, HSYT2			-500	
		ICL7665B, V+ = 9V, $T_A = T_{MIN}$ to T_{MAX}	OUT1, OUT2			2000	
			HYST1, HSYT2			-500	
V_{OUT1} Saturation Voltage		V_{SET1} = 2V, I_{OUT1} = 2mA	ICL7665, ICL7665B: V+ = 2V		0.20	0.50	V
			ICL7665A: V+ = 2V		0.20		
			All grades: V+ = 5V		0.10	0.30	
			ICL7665, ICL7665A: V+ = 15V		0.06	0.20	
			ICL7665B: V+ = 9V		0.06	0.25	
V_{HYST1} Saturation Voltage		V_{SET1} = 2V, I_{HYST1} = -0.5mA	All grades: V+ = 2V		-0.15	-0.30	V
			All grades: V+ = 5V		-0.05	-0.15	
			ICL7665, ICL665A: V+ = 15V		-0.02	-0.10	
			ICL7665B: V+ = 9V		-0.02	-0.15	
V_{OUT2} Saturation Voltage		V_{SET2} = 0V, I_{OUT2} = 2mA	All grades: V+ = 2V		0.20	0.50	V
			All grades: V+ = 5V		0.15	0.30	
			ICL7665, ICL665A: V+ = 15V		0.11	0.25	
			ICL7665B: V+ = 9V		0.11	0.30	
V_{HYST2} Saturation Voltage		V_{SET2} = 2V, I_{HYST2} = -0.2mA	All grades: V+ = 2V		-0.25	-0.80	V
		V_{SET2} = 2V, I_{HYST2} = -0.5mA	All grades: V+ = 5V		-0.43	-1.00	
			ICL7665: V+ = 15V		-0.35	-0.80	
			ICL7665A: V+ = 15V		-0.35	-1.00	
			ICL7665B: V+ = 9V		-0.35	-1.00	
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V+			±0.01	±10	nA
V_{SET} Input Change for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ, V_{OUT}LO = 1% V+, V_{OUT}HI = 99% V+			0.1		mV
Difference in Trip Voltage	V_{SET1}– V_{SET2}	R_{OUT}, R_{HYST} = 1MΩ			±5	±50	mV
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1MΩ			±0.1		mV

AC OPERATING CHARACTERISTICS

(V+ = 5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Delay Time, Input Going High	t_{SO1d}	V_{SET} switched from 1.0V to 1.6V, R_{OUT} = 4.7kΩ, C_L = 12pF, R_{HYST} = 20kΩ		85		µs
	t_{SH1d}			90		
	t_{SO2d}			55		
	t_{SH2d}			55		
Output Delay Time, Input Going Low	$t_{\overline{SO}1d}$	V_{SET} switched from 1.6V to 1.0V, R_{OUT} = 4.7kΩ, C_L = 12pF, R_{HYST} = 20kΩ		75		µs
	$t_{\overline{SH}1d}$			80		
	$t_{\overline{SO}2d}$			60		
	$t_{\overline{SH}2d}$			60		
Output Rise Times	t_{O1r}	V_{SET} switched between 1.0V and 1.6V, R_{OUT} = 4.7kΩ, C_L = 12pF, R_{HYST} = 20kΩ		0.6		µs
	t_{O2r}			0.8		
	t_{H1r}			7.5		
	t_{H2r}			0.7		
Output Fall Times	t_{O1f}	V_{SET} switched between 1.0V and 1.6V, R_{OUT} = 4.7kΩ, C_L = 12pF, R_{HYST} = 20kΩ		0.6		µs
	t_{O2f}			0.7		
	t_{H1f}			4.0		
	t_{H2f}			1.8		

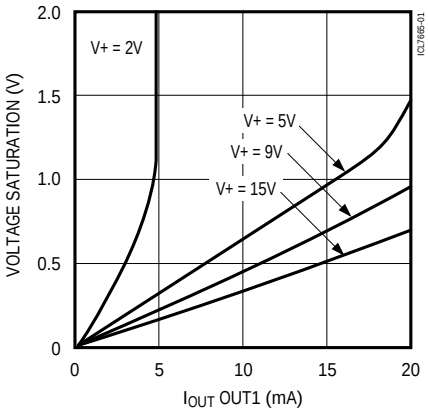
Switching Waveforms



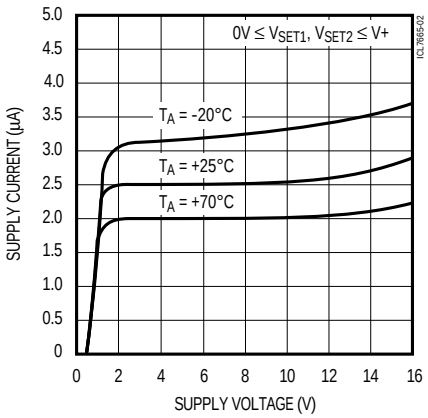
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

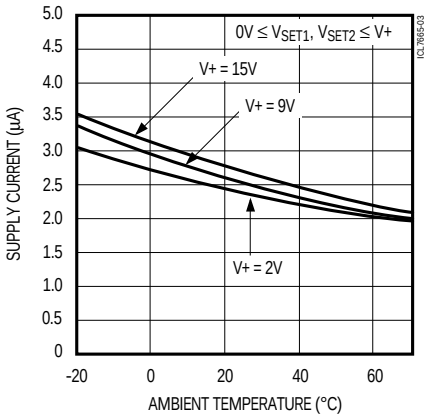
OUT1 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



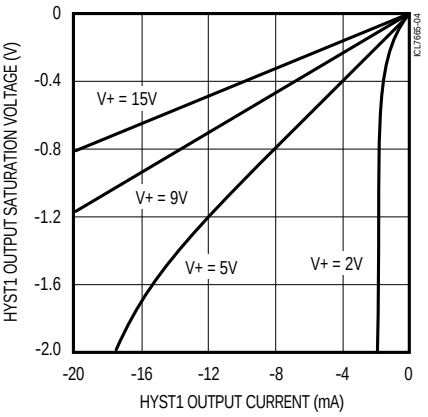
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



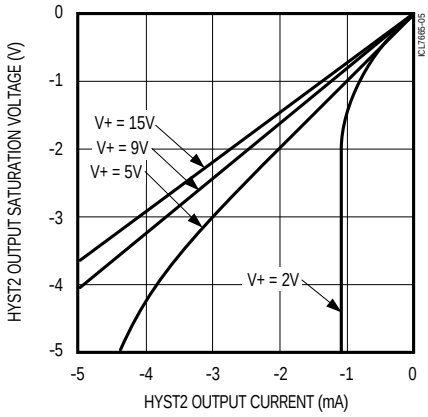
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



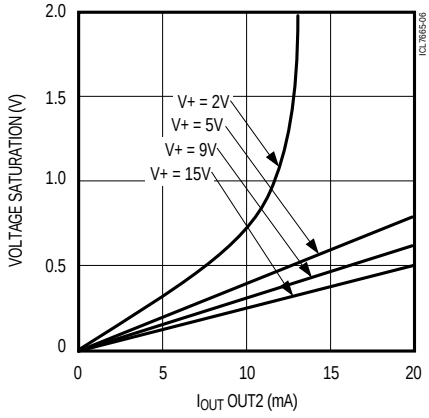
HYST1 OUTPUT SATURATION VOLTAGE vs. HYST1 OUTPUT CURRENT



HYST2 OUTPUT SATURATION VOLTAGE vs. HYST2 OUTPUT CURRENT



OUT2 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



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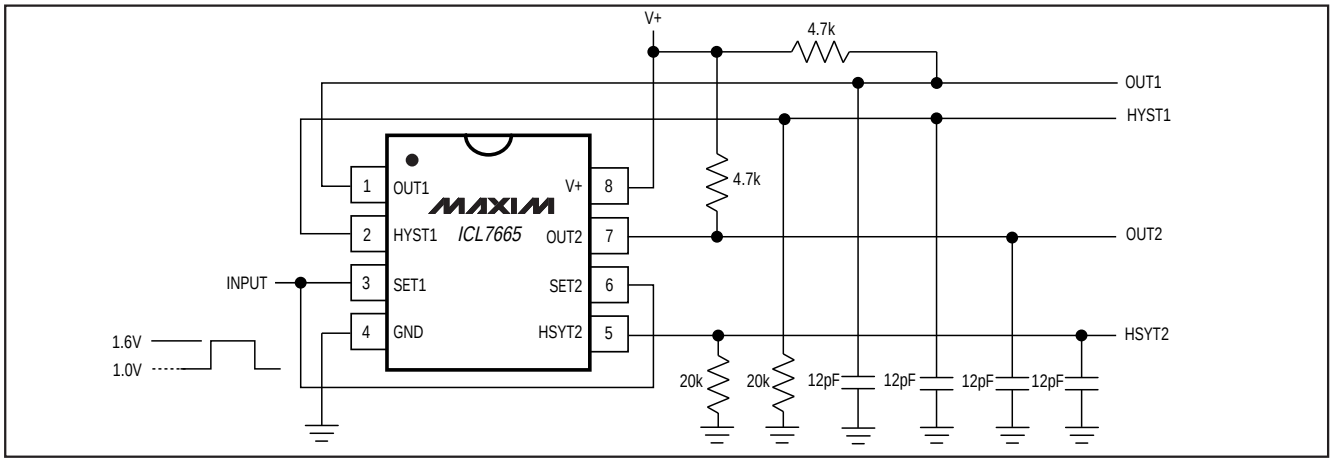

Figure 1. Test Circuit

Detailed Description

As shown in the block diagram of Figure 2, the Maxim ICL7665 combines a 1.3V reference with two comparators, two open-drain N-channel outputs, and two open-drain P-channel hysteresis outputs. The reference and comparator are very low-power linear CMOS circuits, with a total operating current of 10µA maximum, 3µA typical. The N-channel outputs can sink greater than 10mA, but are unable to source any current. These outputs are suitable for wire-OR connections and are capable of driving TTL inputs when an external pull-up resistor is added.

The ICL7665 Truth Table is shown in Table 1. OUT1 is an inverting output; all other outputs are noninverting. HYST1 and HYST2 are P-channel current sources whose sources are connected to V+. OUT1 and OUT2 are N-channel current sinks with their sources connected to ground. Both OUT1 and OUT2 can drive at least one TTL load with a V_{OL} of 0.4V.

Table 1. ICL7665 Truth Table

INPUT*	OUTPUT	HYSTERESIS
V_{SET1} > 1.3V	OUT1 = ON = LOW	HYST1 = ON = HI
V_{SET1} < 1.3V	OUT1 = OFF = HI	HYST1 = OFF = LOW
V_{SET2} > 1.3V	OUT2 = OFF = HI	HYST2 = ON = HI
V_{SET2} < 1.3V	OUT2 = ON = LOW	HYST2 = OFF = LOW

OUT1 is an inverting output; all others are noninverting. OUT1 and OUT2 are open-drain, N-channel current sinks. HYST1 and HYST2 are open-drain, P-channel current sinks.

** See Electrical Characteristics*

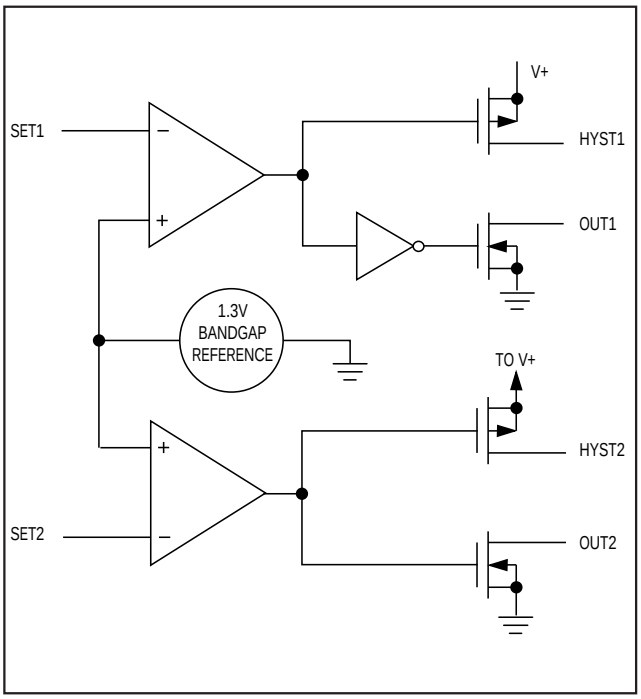

Figure 2. Block Diagram

In spite of the very low operating current, the ICL7665 has a typical propagation delay of only 75µs. Since the comparator input bias current and the output leakages are very low, high-impedance external resistors can be used. This design feature minimizes both the total supply current used and loading on the voltage source that is being monitored.

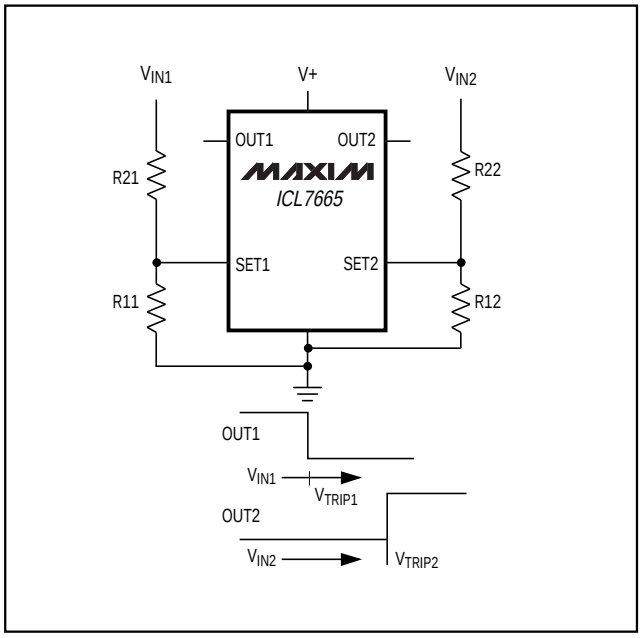

Figure 3. Simple Threshold Detector

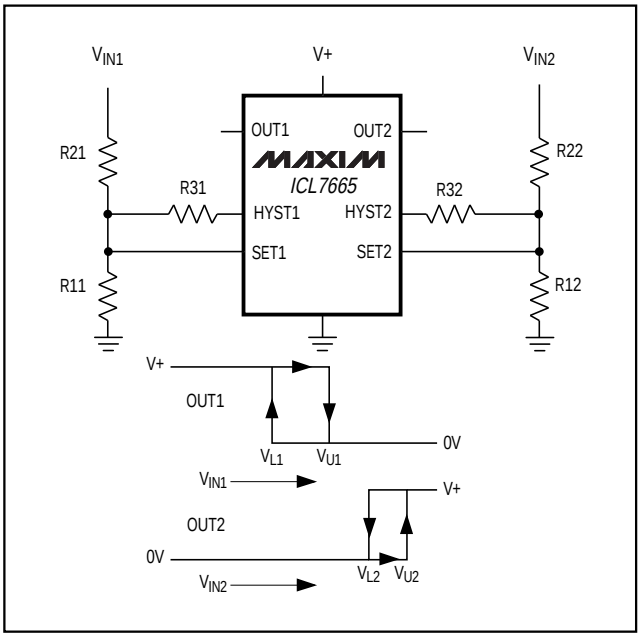

Figure 4. Threshold Detector with Hysteresis

Basic Over/Undervoltage Detection Circuits

Figures 3, 4, and 5 show the three basic voltage detection circuits.

The simplest circuit, depicted in Figure 3, does not have any hysteresis. The comparator trip-point formulas can easily be derived by observing that the comparator changes state when the V_{SET} input is 1.3V. The external resistors form a voltage divider that attenuates the input signal. This ensures that the V_{SET} terminal is at 1.3V when the input voltage is at the desired comparator trip point. Since the bias current of the comparator is only a fraction of a nanoamp, the current in the voltage divider can be less than one microamp without losing accuracy due to bias currents. The ICL7665A has a 2% threshold accuracy at +25°C, and a typical temperature coefficient of 100ppm/°C including comparator offset drift, eliminating the need for external potentiometers in most applications.

Figure 4 adds another resistor to each voltage detector. This third resistor supplies current from the HYST output whenever the V_{SET} input is above the 1.3V threshold. As the formulas show, this hysteresis resistor affects only the lower trip point. Hysteresis (defined as the difference between the upper and lower trip points) keeps noise or small variations in the input signal from repeatedly switching the output when the input signal remains near the trip point for a long period of time.

The third basic circuit, Figure 5, is suitable only when the voltage to be detected is also the power-supply voltage for the ICL7665. This circuit has the advantage that all of the current flowing through the input divider resistors flows through the hysteresis resistor. This allows the use of higher-value resistors, without hysteresis output leakage having an appreciable effect on the trip point.

Resistor-Value Calculations

Figure 3

1) Choose a value for R11. This value determines the amount of current flowing though the input divider, equal to V_{SET} / R11. R11 can typically be in the range of 10kΩ to 10MΩ.
2) Calculate R21 based on R11 and the desired trip point:

$$R21 = R11\left(\frac{V_{TRIP} - V_{SET}}{V_{SET}}\right) = R11\left(\frac{V_{TRIP} - 1.3V}{1.3V}\right)$$

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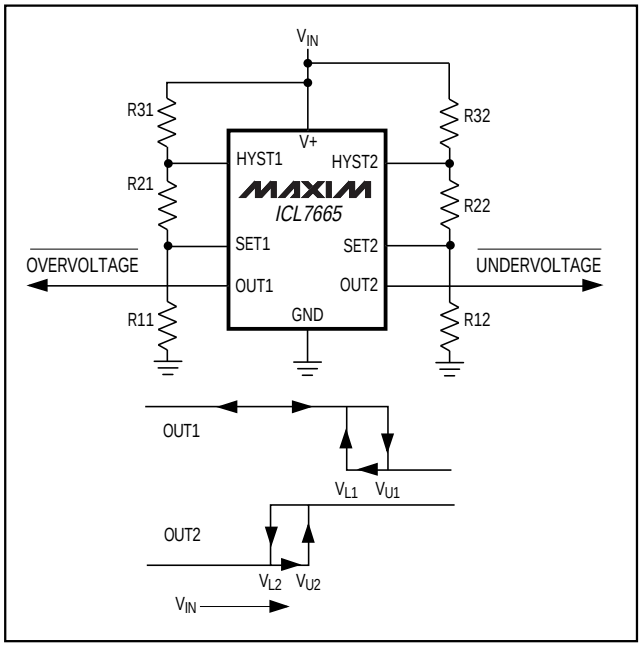

Figure 5. Threshold Detector, V_{IN} = V+

Figure 4

1) Choose a resistor value for R11. Typical values are in the 10kΩ to 10MΩ range.
2) Calculate R21 for the desired upper trip point, V_U, using the formula:

$$R21 = R11\left(\frac{V_U - V_{SET}}{V_{SET}}\right) = R11\left(\frac{V_U - 1.3V}{1.3V}\right)$$

3) Calculate R31 for the desired amount of hysteresis:

$$R31 = \frac{(R21)\,(V+ - V_{SET})}{V_U - V_L} = \frac{(R21)\,(V+ - 1.3V)}{V_U - V_L}$$

or, if V+ = V_{IN}:

$$R31 = \frac{(R21)\,(V_L - V_{SET})}{V_U - V_L} = \frac{(R21)\,(V_L - 1.3V)}{V_U - V_L}$$

4) The trip voltages are not affected by the absolute value of the resistors, as long as the impedances are high enough that the resistance of R31 is much greater than the HYST output's resistance, and the current through R31 is much higher than the HYST output's leakage current. Normally, R31 will be in the 100kΩ to 22MΩ range. Multiplying or dividing all three resistors by the same factor will not affect the trip voltages.

Figure 5

1) Select a value for R11, usually between 10kΩ and 10MΩ.
2) Calculate R21:

$$R21 = R11\left(\frac{V_L - V_{SET}}{V_{SET}}\right) = R11\left(\frac{V_L - 1.3V}{1.3}\right)$$

3) Calculate R31:

$$R31 = R11\left(\frac{V_U - V_L}{V_{SET}}\right)$$

4) As in the other circuits, all three resistor values may be scaled up or down in value without changing V_U and V_L. V_U and V_L depend only on the ratio of the three resistors, if the absolute values are such that the hysteresis output resistance and the leakage currents of the V_{SET} input and hysteresis output can be ignored.

Applications Information

Fault Monitor for a Single Supply

Figure 6 shows a typical over/undervoltage fault monitor for a single supply. In this case, the upper trip points (controlling OUT1) are centered on 5.5V, with 100mV of hysteresis (V_U = 5.55V, V_L = 5.45V); and the lower trip points (controlling OUT2) are centered on 4.5V, also with 100mV of hysteresis. OUT1 and OUT2 are connected together in a wire-OR configuration to generate a power-OK signal.

Multiple-Supply Fault Monitor

The ICL7665 can simultaneously monitor several power supplies, as shown in Figure 7. The easiest way to calculate the resistor values is to note that when the V_{SET} input is at the trip point (1.3V), the current through R11 is 1.3V / R11. The sum of the currents through R21A, R21B and R31 must equal this current when the two input voltages are at the desired low-voltage detection point. Ordinarily, R21A and R21B are chosen so that the current through the two resistors is equal. Note that, since the voltage at the ICL7665 V_{SET} input depends on the voltage of both supplies being monitored, there will be some interaction between the low-voltage trip points for the two supplies. In this example, OUT1 will go low when either supply is 10% below nominal (assuming the other supply is at the nominal voltage), or when both supplies are 5% or more below their nominal voltage. R31 sets the hysteresis, in this case, to about 43mV at the 5V supply or 170mV at the 15V supply. The second section of ICL7665 can be used to detect overvoltage or, as shown in Figure 7, can be used to detect the absence of negative supplies. Note that the trip points for OUT2 depend on both the voltages of the negative power supplies and the actual voltage of the +5V supply.

Combination Low-Battery Warning and Low-Battery Disconnect

Nickel cadmium (NiCd) batteries are excellent rechargeable power sources for portable equipment, but care must be taken to ensure that NiCd batteries are not damaged by overdischarge. Specifically, a NiCd battery should not be discharged to the point where the polarity of the lowest-capacity cell is reversed, and that cell is reverse charged by the higher-capacity cells. This reverse charging will dramatically reduce the life of a NiCd battery. The Figure 8 circuit both prevents reverse charging and gives a low-battery warning. A typical low-battery warning voltage is 1V per cell. Since a NiCd "9V" battery is ordinarily made up of six cells with a nominal voltage of 7.2V, a low-battery warning of 6V is appropriate, with a small hysteresis of 100mV. To prevent overdischarge of a battery, the load should be disconnected when the battery voltage is 1V x (N – 1), where N = number of cells. In this case, the low-battery load disconnect should occur at 5V. Since the battery voltage will rise when the load is disconnected, 800mV of hysteresis is used to prevent repeated on/off cycling.

Power-Fail Warning and Power-Up/Power-Down Reset

Figure 9 illustrates a power-fail warning circuit that monitors raw DC input voltage to the 7805 three-terminal 5V regulator. The power-fail warning signal goes high when the unregulated DC input falls below 8.0V. When the raw DC power source is disconnected or the AC power fails, the voltage on the input of the 7805 decays at a rate of I_{OUT} / C (in this case, 200mV/ms). Since the 7805 will continue to provide a 5V output at 1A until V_{IN} is less than 7.3V, this circuit will give at least 3.5ms of warning before the 5V output begins to drop. If additional warning time is needed, either the trip voltage or filter capacitance should be increased, or the output current should be decreased.

The ICL7665 OUT2 is set to trip when the 5V output has decayed to 3.9V. This output can be used to prevent the microprocessor from writing spurious data to a CMOS battery-backup memory, or can be used to activate a battery-backup system.

AC Power-Fail and Brownout Detector

By monitoring the secondary of the transformer, the circuit in Figure 10 performs the same power-failure warning function as Figure 9. With a normal 110V AC input to the transformer, OUT1 will discharge C1 every 16.7ms when the peak transformer secondary voltage exceeds 10.2V. When the 110V AC power-line voltage is either interrupted or reduced so that the peak voltage is less than 10.2V, C1 will be charged through R1. OUT2, the power-fail warning output, goes high when the voltage on C1 reaches 1.3V. The time constant R1 x C1 determines the delay time before the power-fail warning signal is activated, in this case 42ms or $2\frac{1}{2}$ line cycles. Optional components R2, R3 and Q1 add hysteresis by increasing the peak secondary voltage required to discharge C1 once the power-fail warning is active.

Battery Switchover Circuit

The circuit in Figure 11 performs two functions: switching the power supply of a CMOS memory to a backup battery when the line-powered supply is turned off, and lighting a low-battery-warning LED when the backup battery is nearly discharged. The PNP transistor, Q1, connects the line-powered +5V to the CMOS memory whenever the line-powered +5V supply voltage is greater than 3.5V. The voltage drop across Q1 will only be a couple of hundred millivolts, since it will be saturated. Whenever the input voltage falls below 3.5V, OUT1 goes high, turns off Q1, and connects the 3V lithium cell to the CMOS memory.

The second voltage detector of the ICL7665 monitors the voltage of the lithium cell. If the battery voltage falls below 2.6V, OUT2 goes low and the low-battery-warning LED turns on (assuming that the +5V is present, of course).

Another possible use for the second section of the ICL7665 is the detection of the input voltage falling below 4.5V. This signal could then be used to prevent the microprocessor from writing spurious data to the CMOS memory while its power-supply voltage is outside its guaranteed operating range.

Simple High/Low Temperature Alarm

The circuit in Figure 12 is a simple high/low temperature alarm, which uses a low-cost NPN transistor as the sensor and an ICL7665 as the high/low detector. The NPN transistor and potentiometer R1 form a Vbe multiplier whose output voltage is determined by the Vbe of the transistor and the position of R1's wiper arm. The voltage at the top of R1 will have a temperature coefficient of approximately -5mV/°C. R1 is set so that the voltage at V_{SET2} equals the V_{SET2} trip voltage when the temperature of the NPN transistor reaches the level selected for the high-temperature alarm. R2 can be adjusted so that the voltage at V_{SET1} is 1.3V when the NPN transistor's temperature reaches the low-temperature limit.

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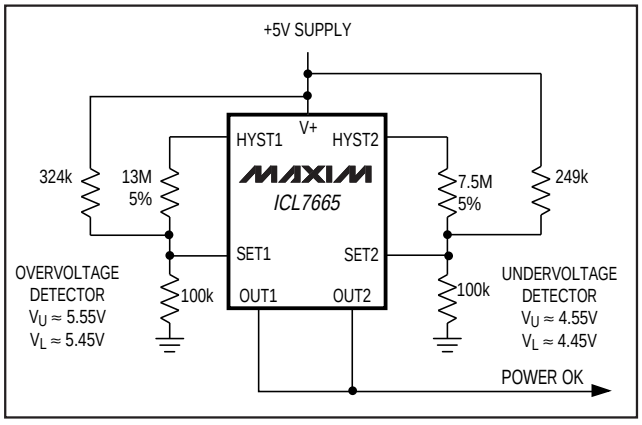


Figure 6. Fault Monitor for a Single Supply

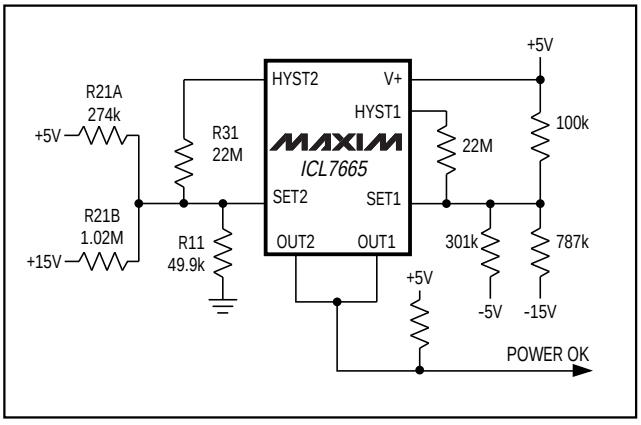


Figure 7. Multiple-Supply Fault Monitor

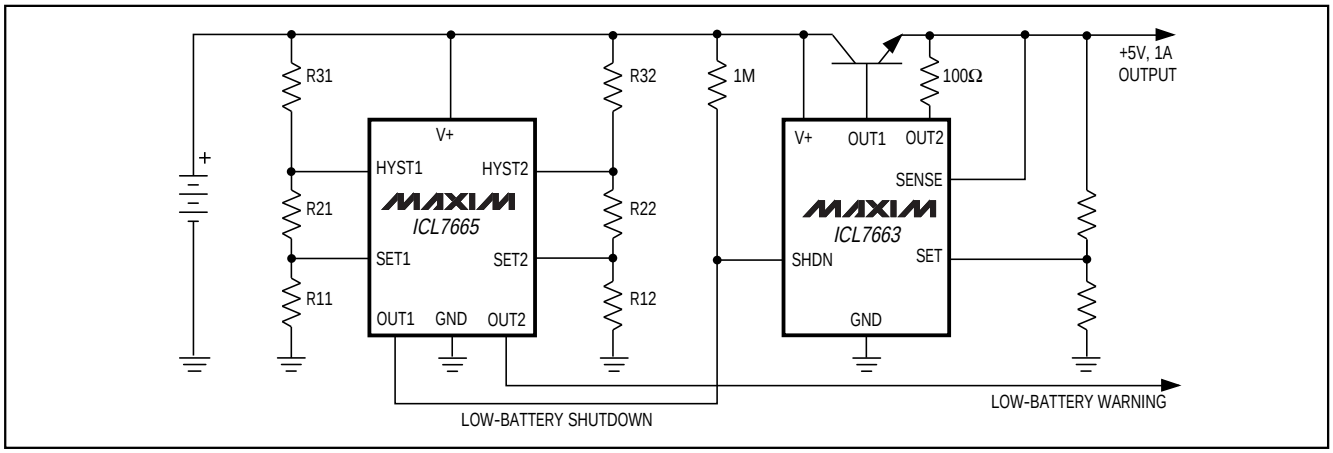


Figure 8. Low-Battery Warning and Low-Battery Disconnect

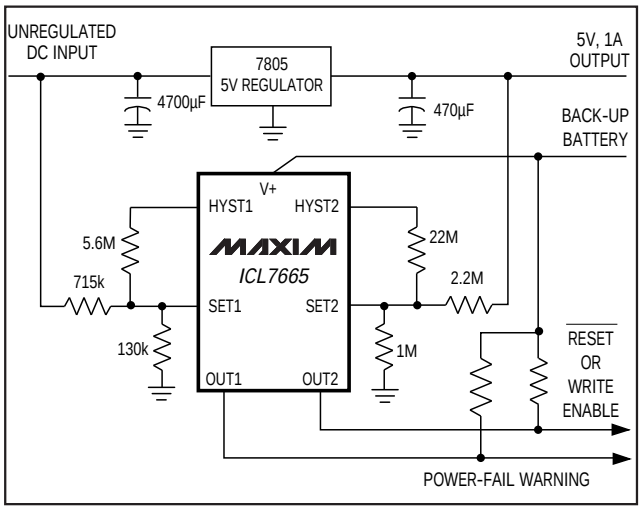


Figure 9. Power-Fail Warning and Power-Up/Power-Down Reset

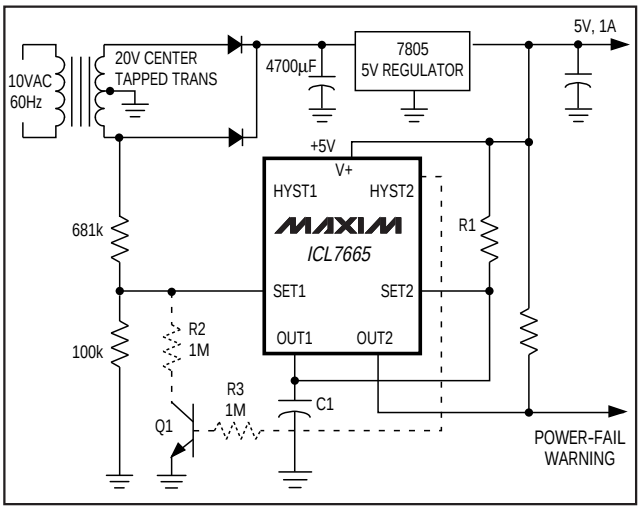


Figure 10. AC Power-Fail and Brownout Detector

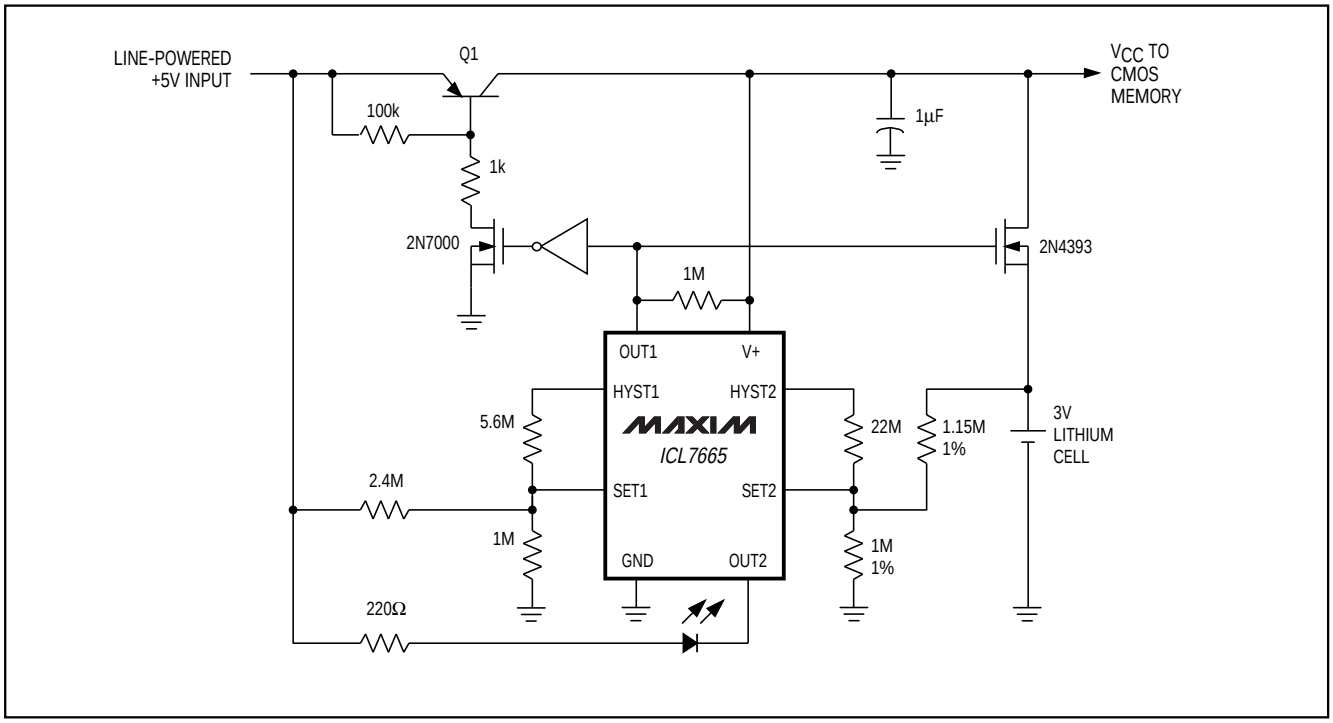


Figure 11. Battery Switchover Circuit

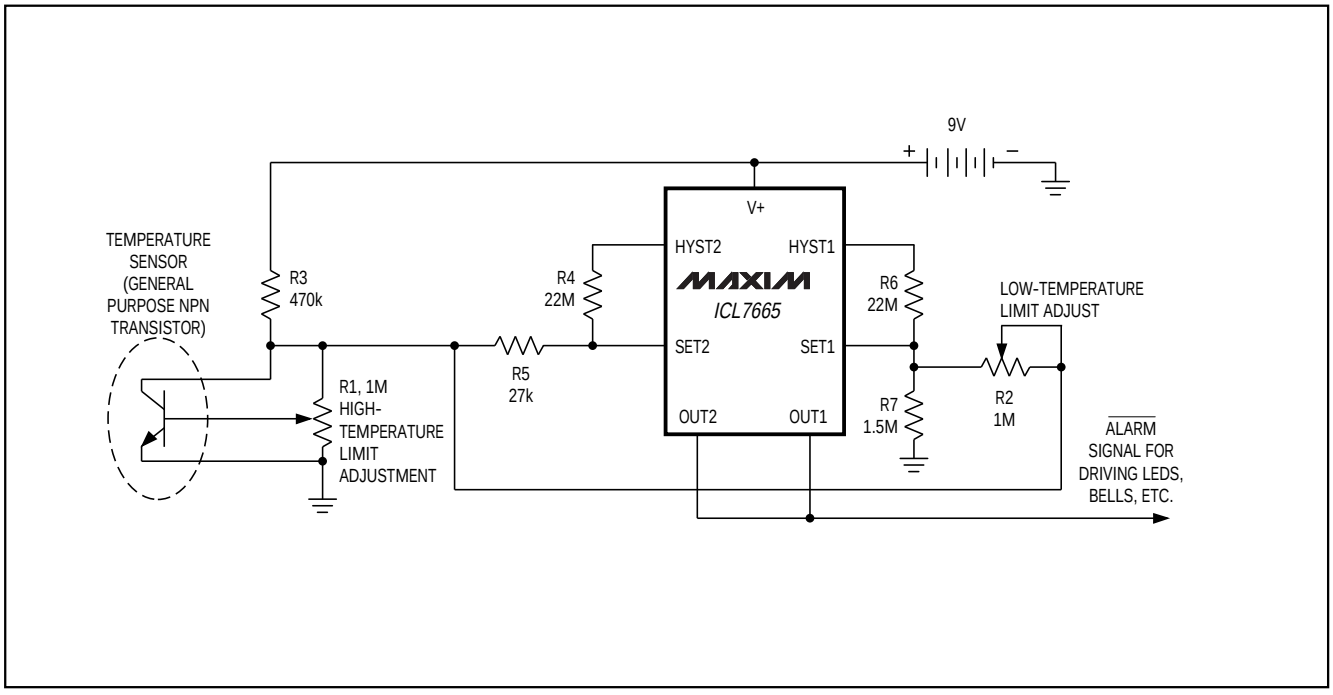


Figure 12. Simple High/Low Temperature Alarm

Microprocessor Voltage Monitor with Dual Over/Undervoltage Detection

SCR Latchup

Like all junction-isolated CMOS circuits, the ICL7665 has an inherent four-layer or SCR structure that can be triggered into destructive latchup under certain conditions. Avoid destructive latchup by following these precautions:

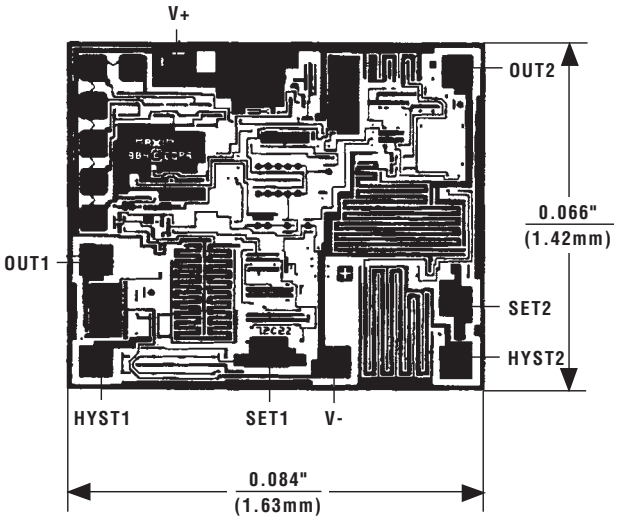
1) If either V_{SET} terminal can be driven to a voltage greater than V+ or less than ground, limit the input current to 500µA maximum. Usually, an input voltage divider resistance can be chosen to ensure the input current remains below 500µA, even when the input voltage is applied before the ICL7665 V+ supply is connected.
2) Limit the rate-of-rise of V+ by using a bypass capacitor near the ICL7665. Rate-of-rise SCRs rarely occur unless: a) the battery has a low impedance—as is the case with NiCd and lead acid batteries; b) the battery is connected directly to the ICL7665 or is switched on via a mechanical switch with low resistance; or c) there is little or no input filter capacitance near the ICL7665. In line-powered systems, the rate-of-rise is usually limited by other factors and will not cause a rate-of-rise SCR action under normal circumstances.
3) Limit the maximum supply voltage (including transient spikes) to 18V. Likewise, limit the maximum voltage on OUT1 and OUT2 to +18V and the maximum voltage on HYST1 and HYST2 to 18V below V+.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
ICL7665AC/D	0°C to +70°C	Dice*
ICL7665IPA+	-20°C to +85°C	8 Plastic DIP
ICL7665IJA+	-20°C to +85°C	8 CERDIP
ICL7665EPA+	-40°C to +85°C	8 Plastic DIP
ICL7665AEPA+	-40°C to +85°C	8 Plastic DIP
ICL7665ESA+	-40°C to +85°C	8 SO
ICL7665AESA+	-40°C to +85°C	8 SO

**Contact factory for dice specifications.*
+Denotes a lead(pb)-free/RoHS-compliant package.

Chip Topography



TRANSISTOR COUNT: 38

SUBSTRATE CONNECTED TO V+.