HMC681A* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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EVALUATION KITS

- HMC681ALP5 Evaluation Board

DOCUMENTATION

Data Sheet

- HMC681A Data Sheet

REFERENCE MATERIALS

Quality Documentation

- Semiconductor Qualification Test Report: PHEMT-J (QTR: 2013-00285)

DESIGN RESOURCES

- HMC681A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SAMPLE AND BUY

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TECHNICAL SUPPORT

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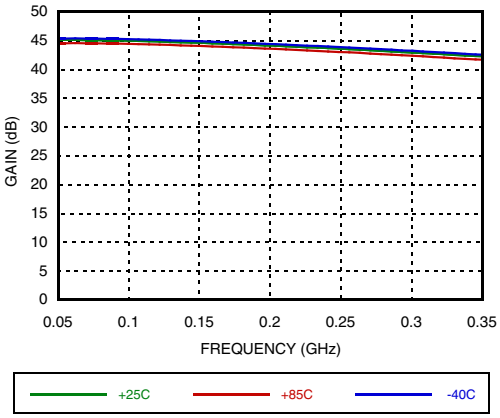
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER w/ SERIAL CONTROL, DC - 1 GHz

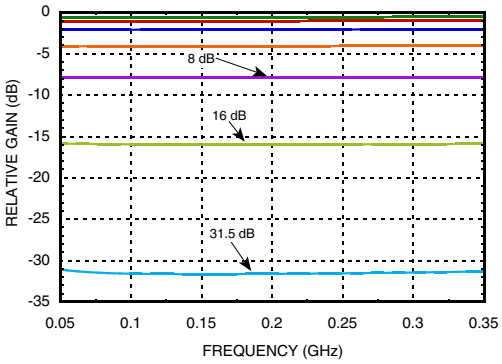
50 to 350 MHz Tuning

Gain vs. Frequency



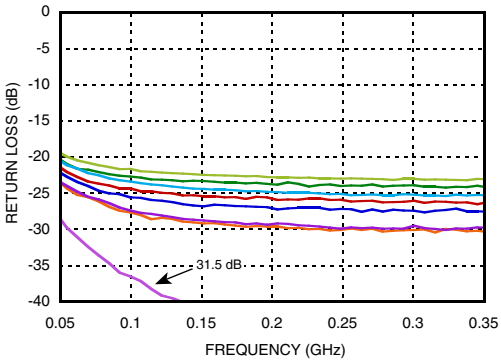
Relative Gain Setting

(Referenced to Maximum Gain State)
(Only Major States are Shown)



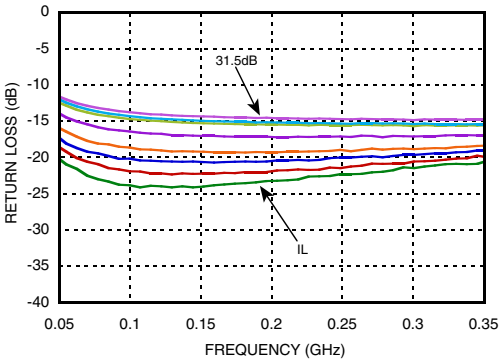
Input Return Loss

(Only Major States are Shown)



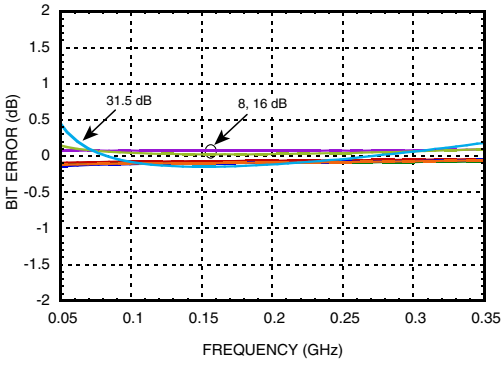
Output Return Loss

(Only Major States are Shown)

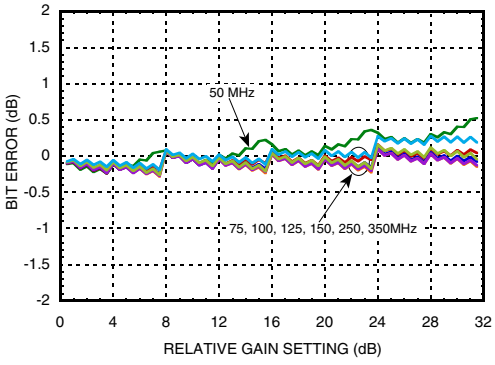


Bit Error vs. Frequency

(Only Major States are Shown)



Bit Error vs. Relative Gain Setting



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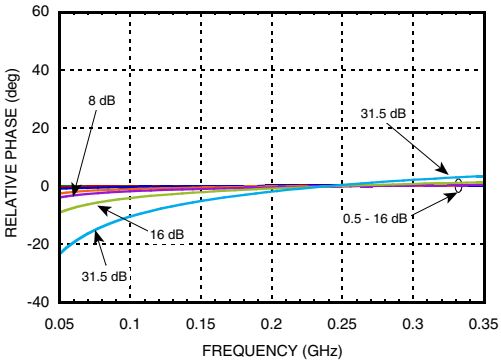
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER w/ SERIAL CONTROL, DC - 1 GHz

50 to 350 MHz Tuning

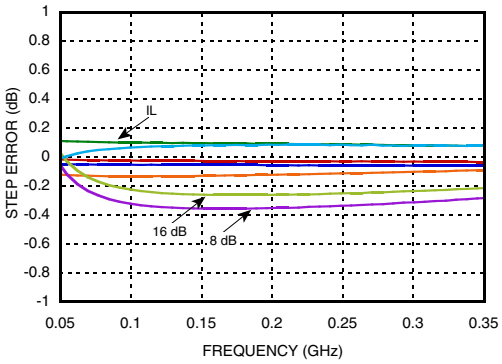
Relative Phase vs. Frequency

(Only Major States are Shown)



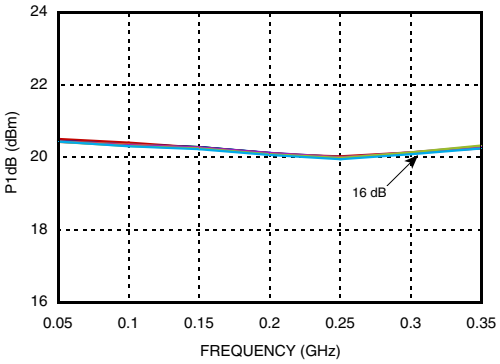
Step Error vs. Frequency

(Only Major States are Shown)

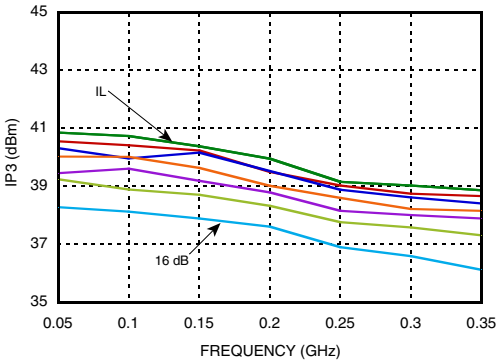


Output P1dB

(Major States shown are IL through 16 dB))



Output IP3 @ 5 dBm Output Power per Tone *(Major States shown are IL through 16 dB)*



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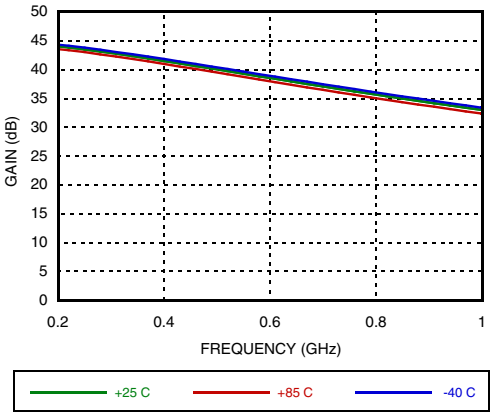
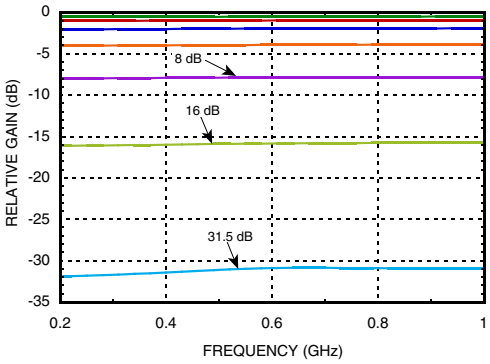
350 to 1000 MHz Tuning

Gain vs. Frequency



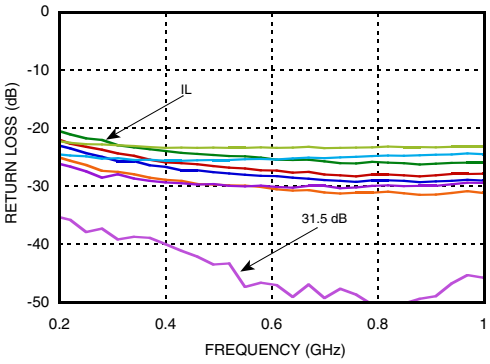
Relative Gain Setting

(Referenced to Maximum Gain State)
(Only Major States are Shown)



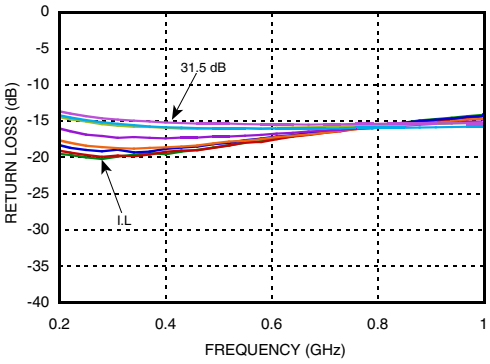
Input Return Loss

(Only Major States are Shown)



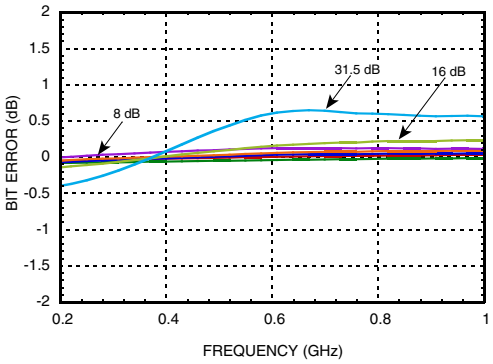
Output Return Loss

(Only Major States are Shown)

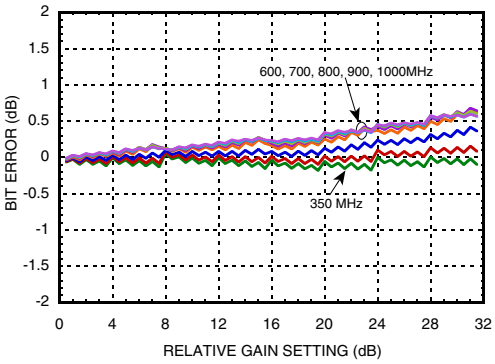


Bit Error vs. Frequency

(Only Major States are Shown)



Bit Error vs. Relative Gain Setting



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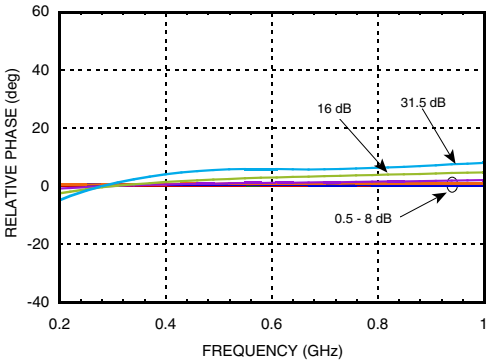
350 to 1000 MHz Tuning

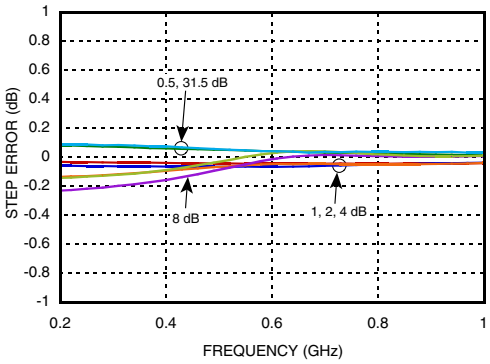
Relative Phase vs. Frequency

(Only Major States are Shown)



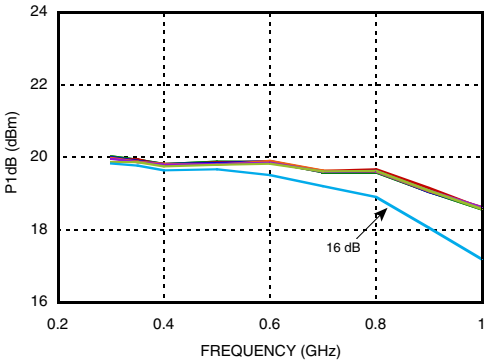
Step Error vs. Frequency

(Only Major States are Shown)

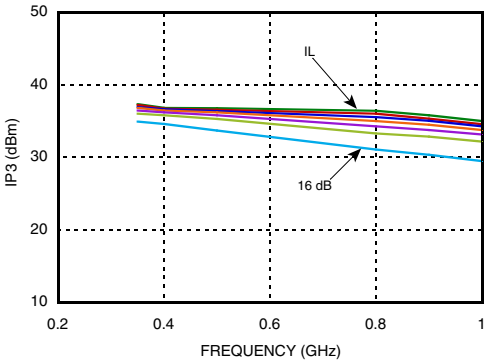


Output P1dB

(Major States shown are IL through 16 dB)



Output IP3 @ 5 dBm Output Power per Tone *(Major States shown are IL through 16 dB)*



Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

PUP Truth Table

LE	PUP1	PUP2	Relative Gain Setting
0	0	0	-31.5
0	1	0	-24
0	0	1	-16
0	1	1	Insertion Loss

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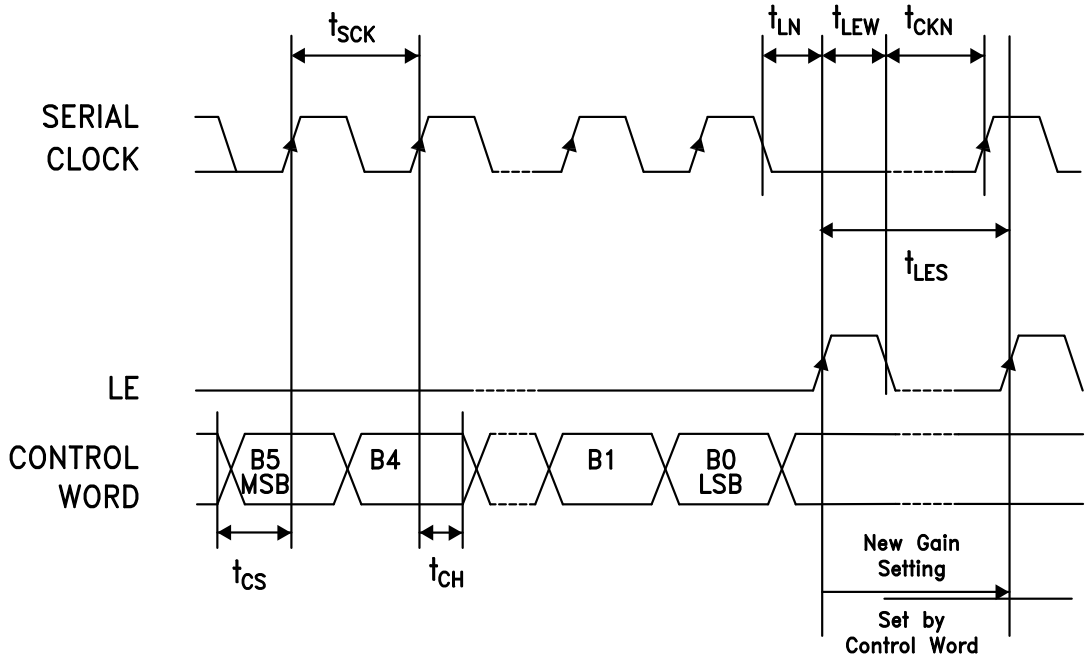
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER w/ SERIAL CONTROL, DC - 1 GHz

Serial Control Interface

The HMC681ALP5E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). It is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches were used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

For all modes of operations, gain will remain constant while LE is kept low.



Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns
Hold Time, $t_{PH.}$	0 ns
Latch Enable Minimum Width, t_{LEN}	10 ns
Setup Time, t_{PS}	2 ns

Truth Table

Serial Word						Relative Gain Setting
B5 16 dB	B4 8dB	B3 4 dB	B2 2 dB	B1 1 dB	B0 0.5 dB	
High	High	High	High	High	High	Reference 0 dB
High	High	High	High	High	Low	-0.5 dB
High	High	High	High	Low	High	-1 dB
High	High	High	Low	High	High	-2 dB
High	High	Low	High	High	High	-4 dB
High	Low	High	High	High	High	-8 dB
Low	High	High	High	High	High	-16 dB
Low	Low	Low	Low	Low	Low	-31.5 dB
Any combination of the above states will provide a relative gain setting approximately equal to the sum of the bits selected.						

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Absolute Maximum Ratings

RF Input Power [1] (At Max Gain Setting)	-10.5 dBm (T = +85 °C)
Digital Inputs ($\overline{\text{Reset}}$, Shift Clock, Latch Enable & Serial Input)	-0.5 to Vdd +0.5V
Bias Voltage (Vdd)	5.5V
Collector Bias Voltage (Vcc)	5.5V
Channel/Junction Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 18.2 mW/°C above 85 °C) [2]	1.18 W
Thermal Resistance [3]	55 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

[1] The Max RF Input Power Rating will increase by 0.5 dB for every 0.5 dB reduction in gain to a maximum RF Input Power of 10 dBm.

[2] This value is the total power dissipation in the amplifier.

[3] This is the thermal resistance for the amplifier.

Bias Voltage

Vdd (V)	Idd (Typ.) (mA)	
+5	2.5	
Vs (V)	Is_1 (mA)	Is_2 (mA)
+5	91	91

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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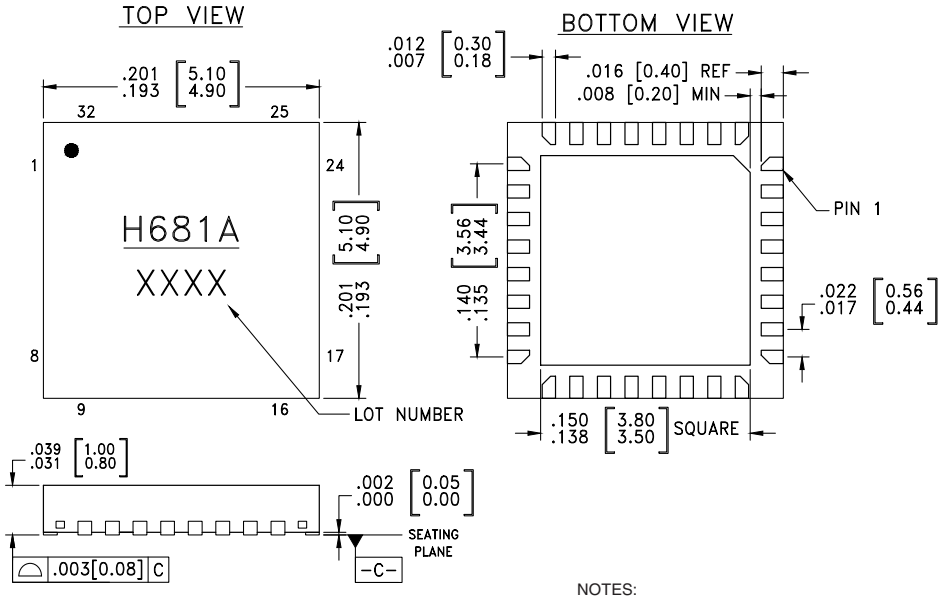
Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC681ALP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H681A XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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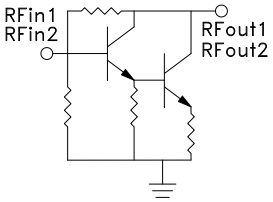
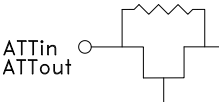
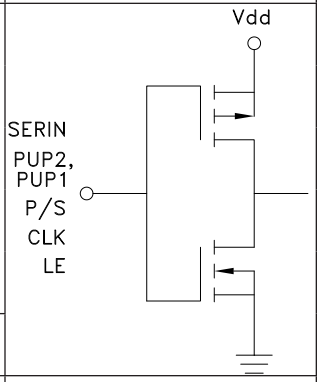
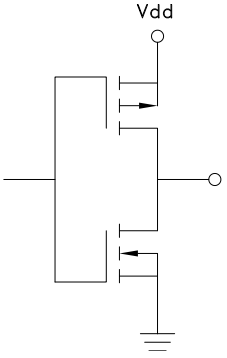
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 5, 9, 14, 16, 23, 28	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
2, 20	RFin1,RFin2	This pin is DC coupled. An off chip DC blocking capacitor is required.	
4, 22	RFout1, RFout2	RF output and DC bias (Vcc) for the output stage of the amplifiers. Amplifier bias provided via external bias tee as shown in application circuit.	
3, 7, 18, 21	GND	These pins and package bottom must be connected to RF/DC ground.	
6, 19	ATTin, ATTout	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
8, 10, 11, 12, 13, 15, 17	ACG1, ACG2, ACG3, ACG4, ACG5, ACG6, ACG7	External capacitors to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
24	SEROUT	Serial input data delayed by 6 clock cycles.	
25, 26	PUP2, PUP1	Refer to truth tables and serial control interface diagram.	
30	CLK		
31	SERIN		
32	LE		
29	P/S	Apply +5V for normal operation.	
27	Vdd	Supply voltage	

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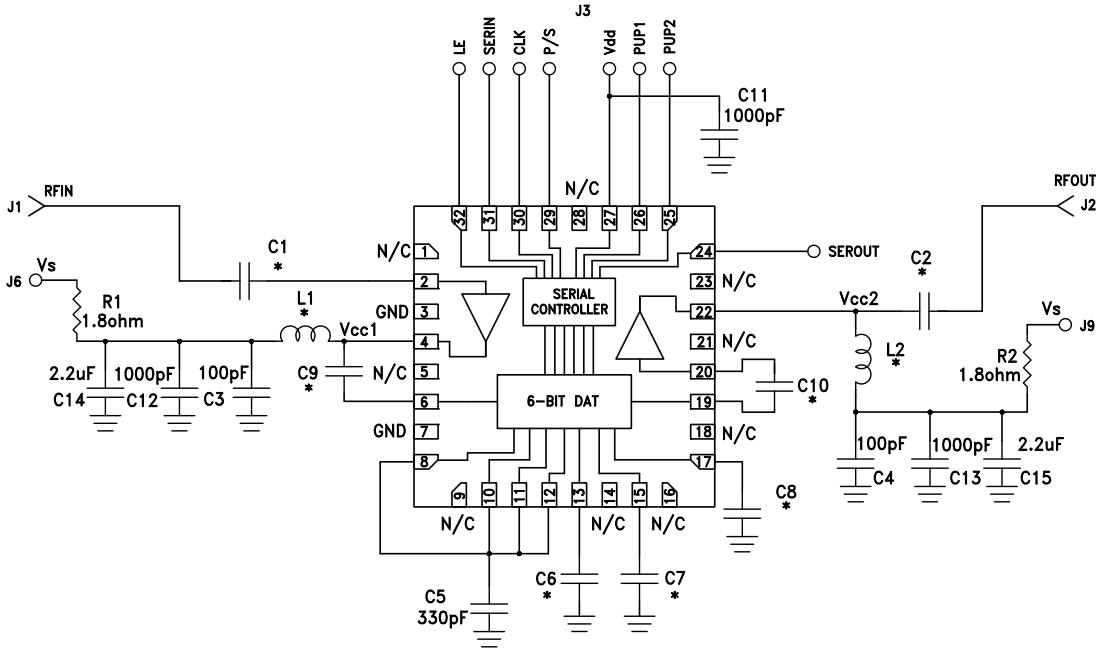
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER w/ SERIAL CONTROL, DC - 1 GHz

Application Circuit



Components for Selected Frequencies

Tuned Frequency	50 - 350 MHz	350 - 1000 MHz
Evaluation PCB	119171-HMC681ALP5	123115-HMC681ALP5
C1, C2, C9, C10	3300 pF	100 pF
C6 - C8	330 pF	100 pF
L1, L2	560 nH	270 nH

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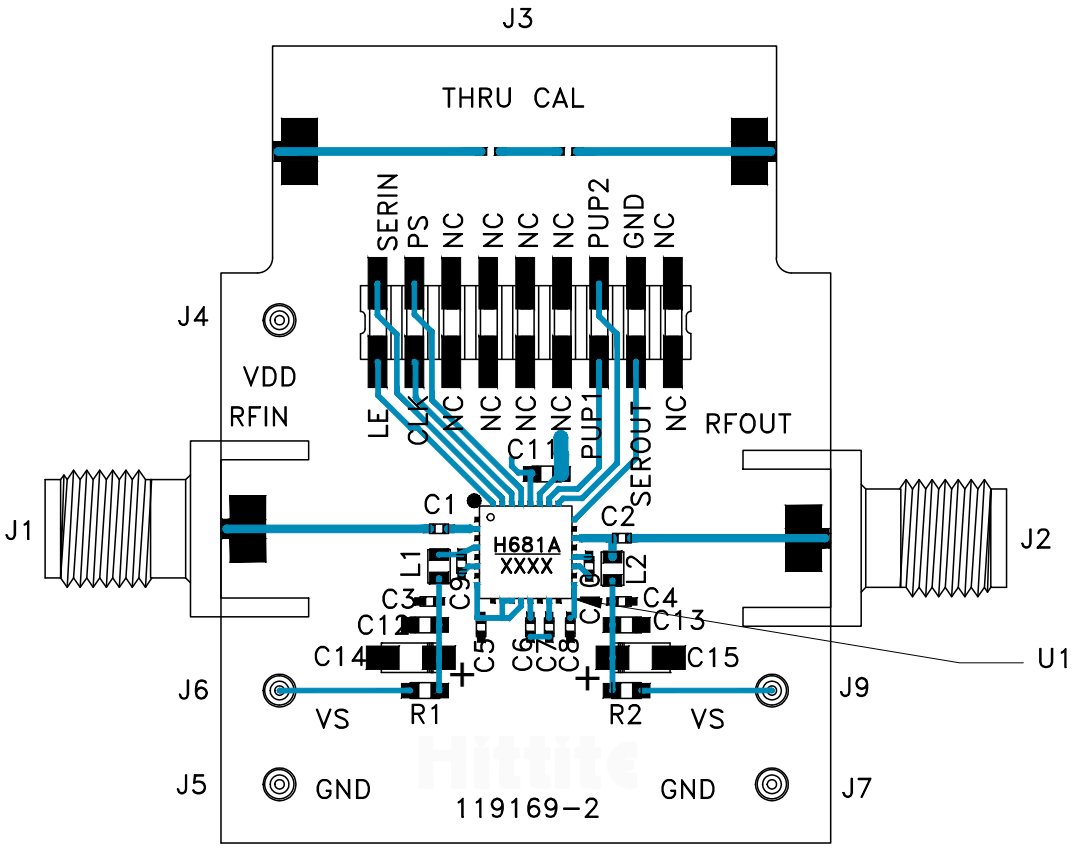
Evaluation PCB



List of Materials for Evaluation PCB [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	18 Pin DC Connector
J4 - J7, J9	DC Pin
C1, C2, C9, C10	Capacitor, 0402 Pkg. [1]
C3 - C5	100 pF Capacitor, 0402 Pkg.
C6 - C8	Capacitor, 0402 Pkg. [1]
C11 - C13	1000 pF Capacitor, 0402 Pkg.
C14, C15	2.2 µF Capacitor, CASE A Pkg.
R1, R2	1.8 Ohm Resistor, 0603 Pkg.
L1, L2	Inductor, 0603 Pkg. [1]
U1	HMC681ALP5E Variable Gain Amplifier
PCB [2]	119169 Evaluation PCB

[1] Please reference “Components for Selected Frequencies” table.

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Refer to “Components for Selected Frequencies” table for part number.

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