HMC1060* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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EVALUATION KITS

- HMC1060LP3E Evaluation Board

DOCUMENTATION

Data Sheet

- HMC1060 Data Sheet

REFERENCE MATERIALS

Quality Documentation

- Package/Assembly Qualification Test Report: 16L 3x3mm QFN Package (QTR: 11003 REV: 02)
- Package/Assembly Qualification Test Report: LP2, LP2C, LP3, LP3B, LP3C, LP3D, LP3F, LP3G (QTR: 2014-0364)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

DESIGN RESOURCES

- HMC1060 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SAMPLE AND BUY

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Electrical Specifications

T_A = +25 °C, VDD = 5.6 V, Unless Otherwise Specified, PTAT Mode is disabled, measured at maximum load conditions in default configuration as shown in Application Schematic.

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage on All Outputs		1.8		5.2	V
Default Output Voltage VR1, VR2, VR3	Default Configuration shown in Application Schematic	3.24	3.3	3.36	V
Default Output Voltage VR4		4.9	5.0	5.1	V
Output Voltage Tolerance [1]	PTAT Mode Disabled			2	%
	PTAT Mode Enabled			3	%
Input Voltage Range (Default)		5.3		5.6	V
Input Voltage Range [2]		3.35	Max (VRx) + 0.3 V	5.6	V
Output Current VR1 [3]	T_A = -40 °C to +85 °C			100	mA
Output Current VR2, VR3 [3]	T_A = -40 °C to +85 °C			50	mA
Output Current VR4 [3]	T_A = -40 °C to +85 °C			300	mA
Total Output Current	T_A = -40 °C to +85 °C			500	mA
Output Noise Voltage Density 10 Hz 100 Hz 1 kHz 10 kHz 100 kHz			2200 120 7 3 3		nV/√Hz
Integrated Output Noise 100 Hz to 100 kHz			1.5		µVrms
Load Regulation, VR4	0 to 300 mA		0.007		% / mA
VR1 PSRR 1 kHz 10 kHz 100 KHz 1 MHz 10 MHz			 80 80 72 60 52		dB
Current Consumption (I_{GND})	VEN = VDD = 5.6 V; Maximum Load Current		2.1		mA
Power Down Current	VEN = Low; VRx outputs are floating (high - impedance) in Power-Down Mode		1	2	µA
Start-Up Transient Time	0 to 90% of final voltage; EN connected to VDD		50		ms
EN Turn-On Delay	0 to 90% of final output voltage Cref = 4.7 µF; Cload = 10 µF; VDD = 5.6 VEN transition from 0 to VDD		30		ms
Enable Input EN High Level		2		VDD + 0.3	V
Enable Input EN Low Level		0		0.8	V
Thermal Protection Threshold Junction Temperature	No loads		150		°C
Maximum Dissipated Power	All Outputs Loaded			1.6	W

[1] When using external resistors to configure the HMC1060LP3E outputs to non-default levels, the temperature coefficient of external resistors may increase the output voltage tolerance. Note that internal resistors have a temperature coefficient of +270 ppm/°C.

[2] Minimum input voltage (VDD) is defined by maximum desired output voltage. As an example minimum input voltage (VDD) of 4.3 V is required to set the HMC1060LP3E outputs as follows VR1 = VR2 = VR3 = 3.3 V, VR4 = 4 V.

[3] The outputs will withstand short-circuit conditions for a duration of less than 10 seconds.

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Typical Performance Characteristics

T_A = +25 °C, VDD = 5.6 V, Unless Otherwise Specified, PTAT Mode is disabled, measured at maximum load conditions in default configuration as shown in Application Schematic.

Figure 1. Typical Output Noise Density at Each HMC1060LP3E Output

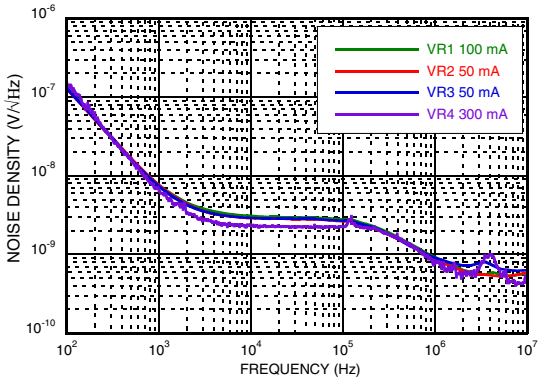


Figure 2. Typical Output Noise Density vs. Capacitor Values [1]

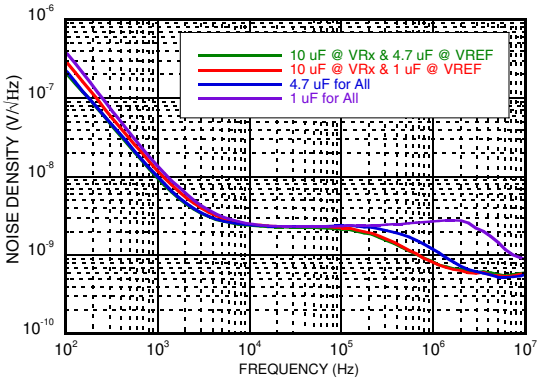


Figure 3. VR1, VR2, VR3, & VR4 Power Supply Rejection Ratio (PSRR)

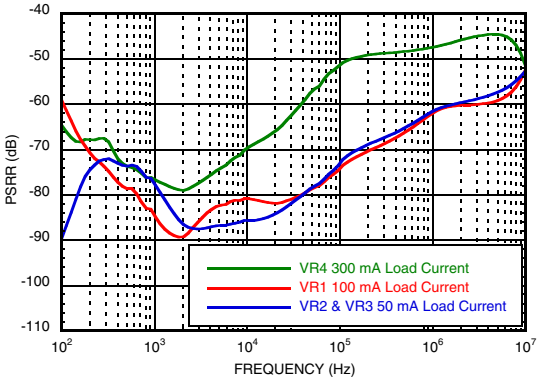


Figure 4. VR4 PSRR vs. VDD (4.7µF on VR4 and VREF)

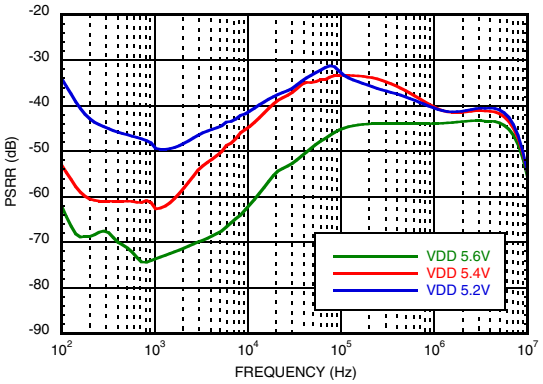


Figure 5. VR1, 2, 3 Voltage vs. Temperature, PTAT Mode Disabled

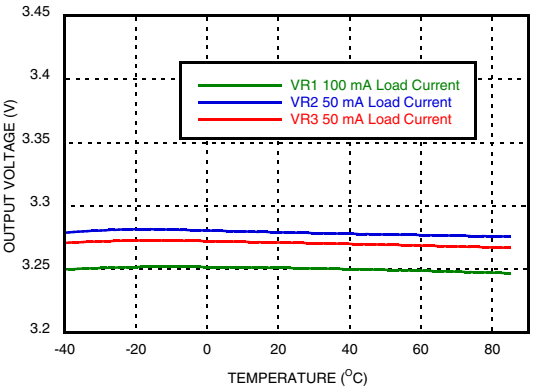
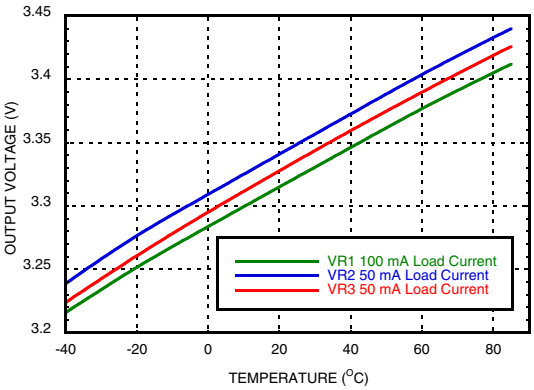


Figure 6. VR1, 2, 3 Voltage vs. Temperature, PTAT Mode Enabled



[1] VREF capacitor corresponds to C1 in Application Schematic. VRx capacitors correspond to capacitors C10, C7, C8, C9 at the output of VR1, VR2, VR3 and VR4 pins of the HMC1060LP3E respectively.

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Figure 7. VR4 Output Voltage vs. Temperature, PTAT Mode Disabled [2]

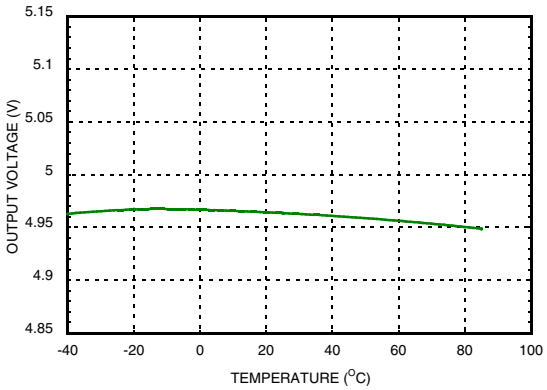


Figure 8. VR4 Output Voltage vs. Temperature, PTAT Mode Enabled [2]

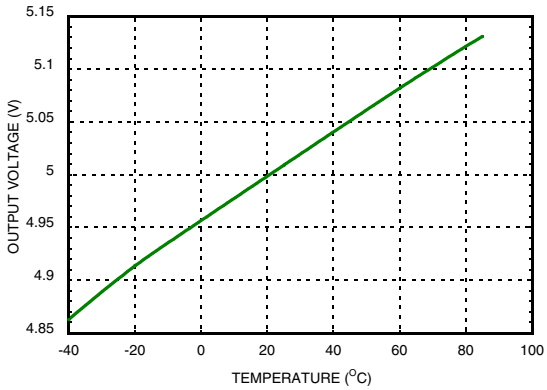


Figure 9. VR4 Output Voltage vs. Supply Voltage On VDD Pin, PTAT Mode Disabled [2]

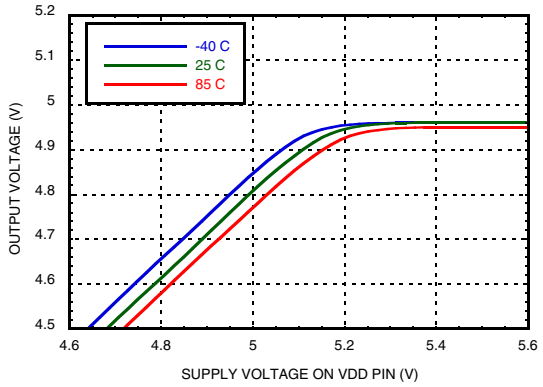


Figure 10. VR4 Output Voltage vs. Supply Voltage On VDD Pin, PTAT Mode Enabled [2]

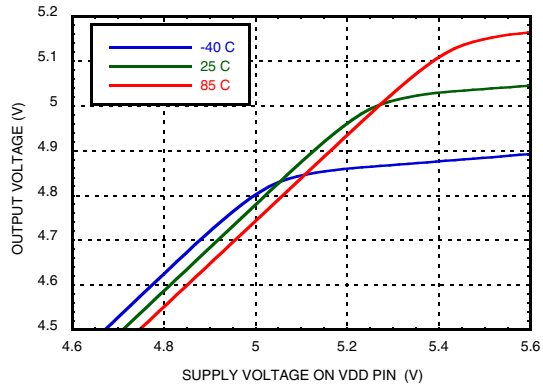


Figure 11. VR4 Output Voltage vs. Load [2]

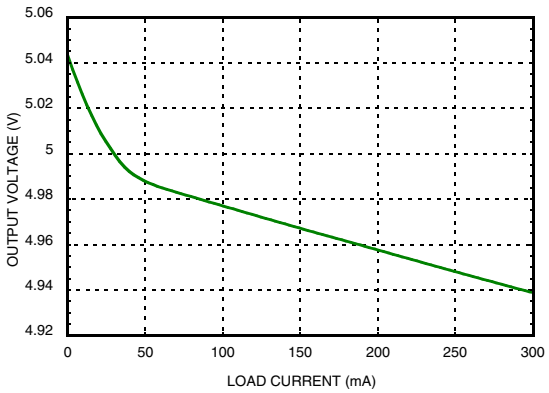
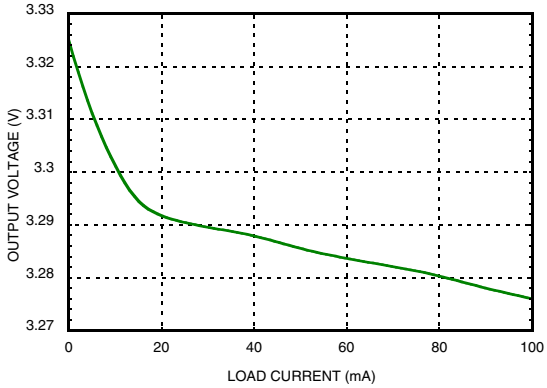


Figure 12. VR1 Output Voltage vs. Load



[2] Measured results were compensated for evaluation board losses.

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QUAD LOW NOISE HIGH PSRR LINEAR VOLTAGE REGULATOR

Absolute Maximum Ratings

VDD to GND Voltage (max / min)	+6.5 V / -0.3 V [1]
EN to GND Voltage (max / min)	VDD + 0.5 V / -0.3 V
RDx / HVx to GND Voltage (max / min)	VDD + 0.5 V / -0.3 V
Thermal Resistance (Junction to ground paddle)	25 °C/W
Maximum Junction Temperature	+150 °C [2]
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 3A

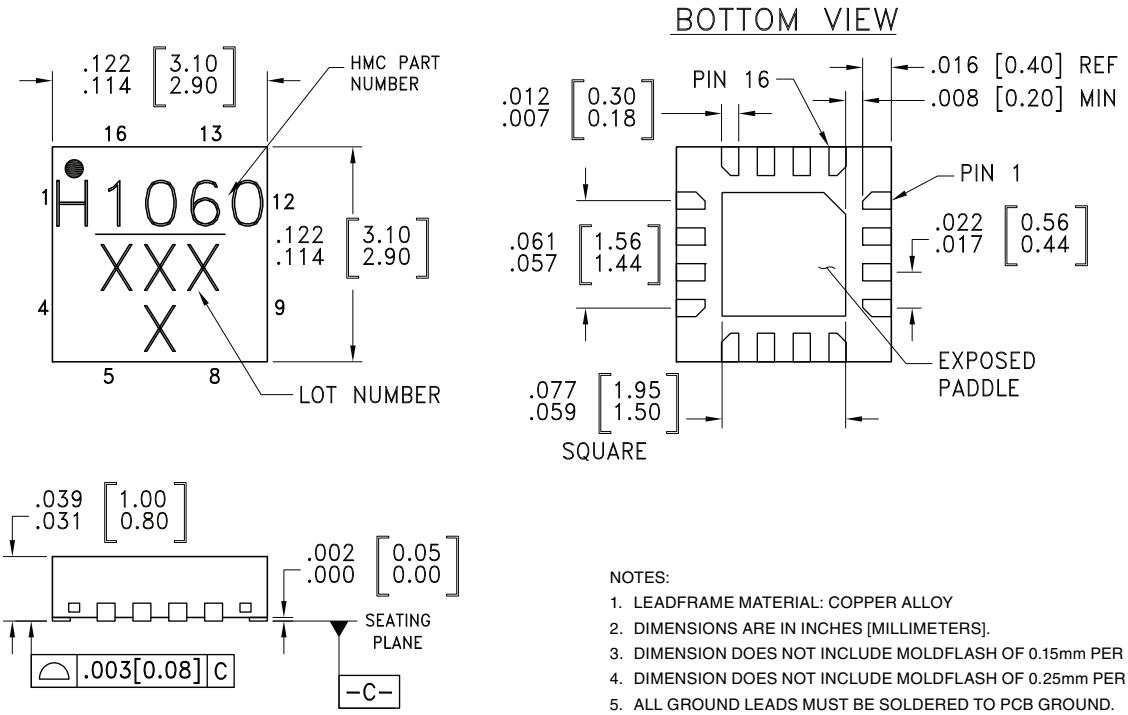
[1] Including short transient events

[2] Operation above +125 °C may shorten the lifetime of the device. Operation above +150 °C risks immediate damage to the device.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The absolute maximum ratings apply individually only and not in combination.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB GROUND.
6. CLASSIFIED AS MOISTURE SENSITIVITY LEVEL (MSL) 1.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC1060LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	1060 XXX X

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

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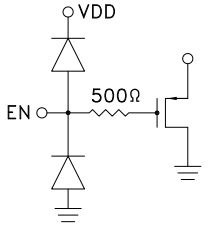
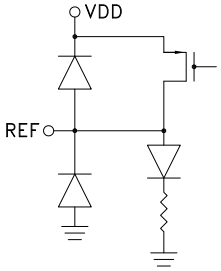
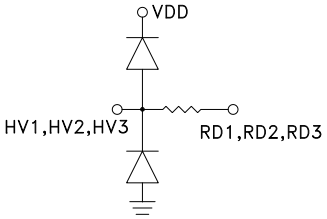
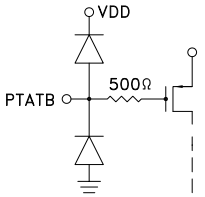
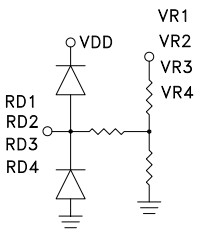
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	VDD	Unregulated power supply input	
2	GND	Supply Ground	
3	EN	Enable Input, TTL Logic Level. The VRx outputs are floating (high impedance) when EN = Low.	
4	REF	Reference voltage (band-gap) output. Cannot be used to source/sink current to/from external circuits. Voltage on REF pin = 1.17 at +27°C when PTAT Mode is disabled, and equals 1.37 V at +27°C when PTAT Mode is enabled. Must be measured with 10 GΩ meter such as Agilent 33410A, typical 10 MΩ DVM may read erroneously.	
5	HV3	Used with RD3 to set VR3 output voltage.	
13	HV2	Used with RD2 to set VR2 output voltage.	
16	HV1	Used with RD1 to set VR1 output voltage.	
8	PTATB	Sets all output voltages in PTAT mode when connected to GND, default mode when open	
6	RD3	Feedback for VR3.	
7	RD4	Feedback for VR4	
14	RD2	Feedback for VR2	
15	RD1	Feedback for VR1	

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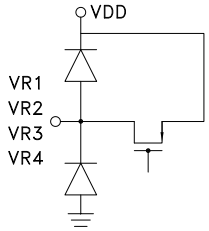
Pin Descriptions *(Continued...)*

Pin Number	Function	Description	Interface Schematic
9	VR4	Regulator output #4	
10	VR3	Regulator output #3	
11	VR2	Regulator output #2	
12	VR1	Regulator output #1	
Package Base	N/C	Should contact PCB metallic area for best thermal dissipation. Can be connected to Ground.	

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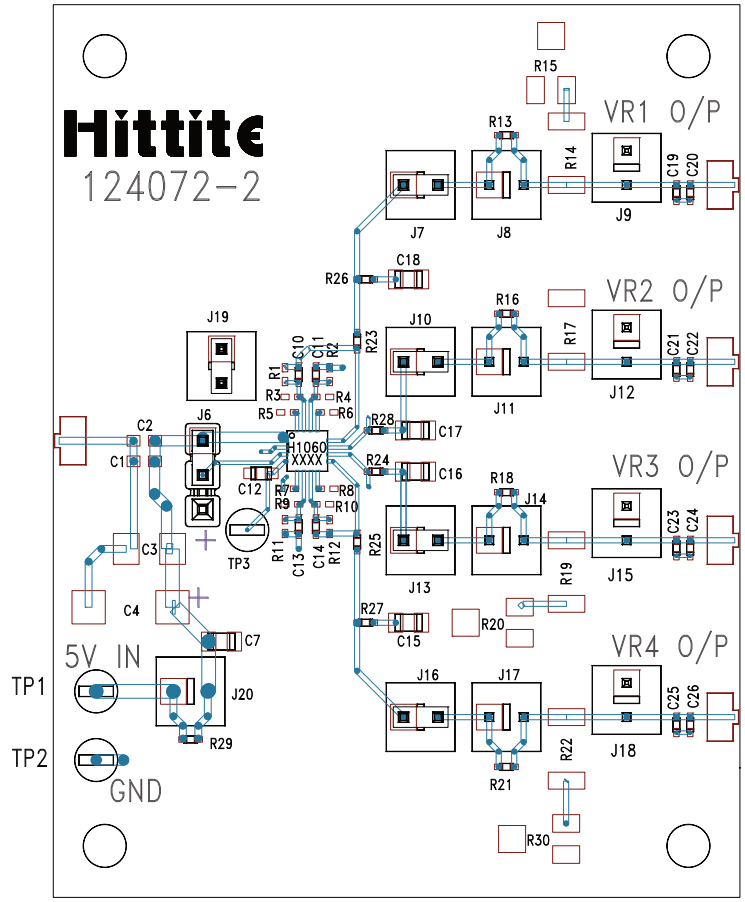
Evaluation PCB



A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view the Eval PCB Schematic please visit www.hittite.com and choose HMC1060LP3E from the "Search by Part Number" pull down menu.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1060LP3E Evaluation PCB	EVAL01-HMC1060LP3E

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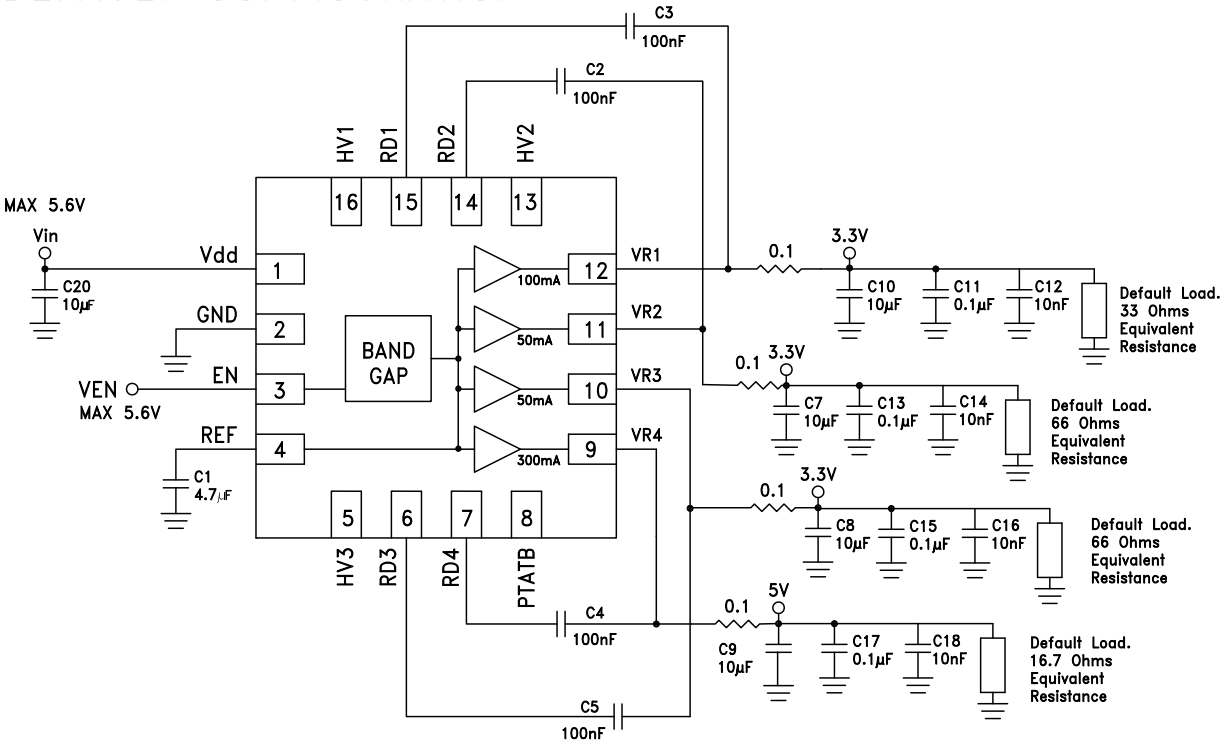
Application Schematic

DEFAULT CONFIGURATION



In order to achieve the typical noise performance specified in the Electrical Specifications Table, a 4.7 µF decoupling capacitor between REF and GND pins (C1), and 100 nF capacitors connected between output pins VRx (x=1,2,3,4) and respective RDx pins (C2, C3, C4 and C5) are required. If noise performance is not critical for a particular output, the 100 nF capacitor can be omitted for the corresponding regulator output. In that case, noise spectral density will typically increase by a factor of 20 at 10 kHz. The 4.7 µF REF capacitor causes approximately 40 ms typical turn-on start-up time. The effects of reducing the REF capacitor on regulator noise performance and regulator turn-on time are shown in Figure 2 and External Enable Pin & Power Up Timing section respectively.

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Theory Of Operation

HMC1060LP3E is a four output ultra low noise regulator. The four outputs can be configured to supply anywhere from 1.8 V to 5.2 V. Three outputs (VR1, VR2, and VR3) are configured to supply 3.3 V by default, and have a different maximum current rating. VR1 is rated at 100 mA maximum, and VR2 and VR3 are rated at a maximum of 50 mA each. The fourth output, VR4, is configured to supply 5 V by default, and is rated at 300 mA maximum current. Details specifying various configuration options are available in Output Voltage Configuration section. Default configuration is shown in Application Schematic section.

The HMC1060LP3E includes a number of features including:

- Thermal Protection feature that disables the outputs of the HMC1060LP3E when the device temperature reaches a critical temperature. More details are available Thermal Protection section.
- PTAT (Proportional To Absolute Temperature) feature that can be enabled or disabled via an external PTATB pin of the HMC1060LP3E. PTAT feature, when enabled, scales the output voltage with device temperature in order to supply optimal supply voltage and current at each temperature in order to maximize the performance of devices supplied by the HMC1060LP3E. More information about PTAT feature is available in PTAT Feature and Benefits of PTAT sections.

Thermal Protection

The thermal protection circuitry of the HMC1060LP3E disables the outputs when junction temperature rises to approximately +150°C. The outputs are kept disabled until the junction temperature cools down by approximately 15°C. The outputs are then re-enabled.

In cases where ambient temperature and/or power dissipation are sufficiently high to re-heat the HMC1060LP3E repeatedly to +150°C, the thermal protection feature of the HMC1060LP3E will repeat. As a result the thermal protection feature will cycle the outputs On and Off, protecting the HMC1060LP3E and the components it supplies from damage. After the overloads, or other fault conditions are removed/changed, the HMC1060LP3E output will return to normal operation.

If a momentary short-circuit occurs at the output, the associated increase in temperature may activate the thermal protection circuitry, protecting the HMC1060LP3E and the components it supplies. The device is not protected from short circuit events lasting longer than 10 seconds.

Operation at Absolute Maximum Ratings levels may damage the HMC1060LP3E immediately. Reliable, long term operation requires adherence to Electrical Specifications.

Stability Considerations

A regulator is a feedback system. A large capacitor with low ESR (Equivalent Series Resistance) may affect the feedback dynamics and can result in unstable operation or noise peaking. Two approaches are recommended to ensure regulator stability:

1. If only one decoupling capacitor is used at the output, the chosen capacitor must have an ESR as defined in the Stability Requirements table below. This guarantees stability over all loading conditions with the chosen decoupling capacitor.
2. In the case where several capacitors are connected at the output (which is often the case with noise and spurious emission sensitive circuits), the recommended approach is to insert a small resistor in series with the load after the 100 nF feedback capacitor (0.1 Ω resistances shown in the Application Schematic). Recommended ESR values are shown in the Stability Requirements table below.

Stability Requirements

Total Capacitance at VRx	Recommended Equivalent Series Resistance
0.1 µF to 1 µF	200 mΩ
> 1 µF	100 mΩ

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HMC1060LP3E's PTAT (Proportional to Absolute Temperature) Feature

The performance of most electronic circuits varies with temperature. The effect on performance is usually most prevalent at high temperatures, where the electronic circuits slow down due to changes in transistor characteristics.

The HMC1060LP3E PTAT Mode is designed to counterbalance the effect of temperature changes on devices supplied by the HMC1060LP3E. When PTAT Mode is enabled, the HMC1060LP3E scales output voltage proportionally with temperature, resulting in higher supply voltage at high temperatures and lower supply voltage at lower temperatures, as shown in Figure 6 and Figure 8.

Higher supply voltage has the opposite effect as that of temperature increase. It increases supply current and speeds up electronic circuits, thereby improving performance and offsetting the negative effect of high temperature on device performance.

HMC1060LP3E PTAT mode is enabled by grounding HMC1060LP3E's PTATB pin. It is disabled by leaving the PTATB pin of the HMC1060LP3E floating.

The rate at which HMC1060LP3E's PTAT mode scales supply voltage with temperature is optimized to work with Hittite's Wideband PLLs with Integrated VCOs, such as the HMC830LP6GE. However, this feature is also beneficial for other products as well. Most electronic circuits slow down at higher temperatures. Higher supply voltage at higher temperatures has the opposite effect of speeding up the circuitry by providing more current and thereby improving performance.

Output Voltage Configuration

All of the outputs of the HMC1060LP3E can be configured to supply anywhere from 1.8 V to 5.2 V. The output voltage is configured using external resistors. PTAT mode can be enabled/disabled for all output options.

Default Configuration

Three outputs (VR1, VR2, and VR3) supply 3.3 V by default, and one output (VR4) defaults to 5 V. The Default configuration of the HMC1060LP3E is shown in the Application Schematic section of this document.

Supply Voltage Less Than Default Configuration

The outputs of the HMC1060LP3E are configured to supply voltages less than the default values, down to 1.8 V minimum, by connecting a resistance (Ry in Figure 13) between pins VRx and RDx (where x = 1,2,3,4). Figure 13 shows an example of configuring VR1 output. Other outputs are configured in exactly the same way (ie. Ry is added between VR2 & RD2, VR3 & RD3 and between VR4 & RD4).

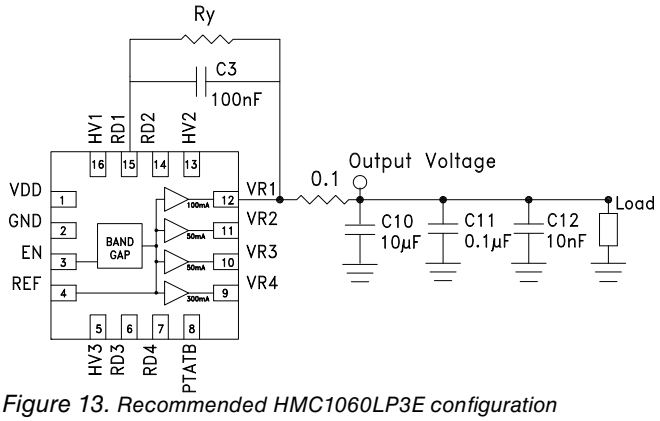

Figure 13. Recommended HMC1060LP3E configuration for supplying output voltage values less than default.[1]

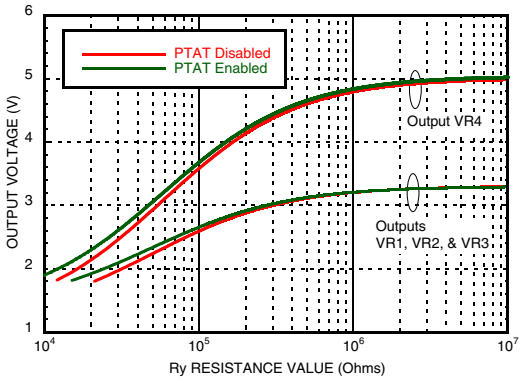

Figure 14. HMC1060LP3E output voltage as a function of resistance Ry for each output at 27°C. [2]

Resistance, Ry, required to configure the HMC1060LP3E to the desired output voltage level for each output of the HMC1060LP3E is shown in Figure 14. The exact value of Ry can be calculated using (EQ 1), where internal resistances

[1] Example shows the configuration of only VR1 output of the HMC1060LP3E. Other outputs are configured in exactly the same way. .

[2] This curve is accurate only in cases where output voltage less than default is required. Minimum level is 1.8 V.

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R1, R2, and band-gap voltage VREF are provided in the Output Configuration Table, and where VRx (x = 1,2,3,4) is the desired output voltage level of each HMC1060LP3E output, as measured at the output pin.

$$R_Y = \frac{R_2\left(\frac{VRx}{VREF} - 1\right)}{1 - \frac{R_2}{R_1}\left(\frac{VRx}{VREF} - 1\right)} \qquad \textbf{(EQ 1)}$$

Output Configuration Table

Output	PTAT Mode	R1 (kΩ)	R2 (kΩ)	R3 (kΩ) [1]	VREF (V)
VR1, VR2, VR3	Disabled	50	27.4	34.6	1.17
	Enabled	50	35.5	34.6	1.37
VR4	Disabled	59	18	N/A	1.17
	Enabled	59	22	N/A	1.37

[1] Internal resistor R3 exists between pins RD1 and HV1, between RD2 and HV2, and between RD3 and HV3. Internal resistances R1, R2, and R3 have a temperature coefficient of +270 ppm/°C. When using external resistances to configure the HMC1060LP3E to non-default output voltages it may be beneficial to use the R3 resistance value in order to achieve a desired resistance Rx when configuring VR1, VR2, and/or VR3 outputs to voltages greater than default value (3.3 V)

Supply Voltage Greater Than Default Configuration

To configure any or all of the VR1, VR2, and VR3 outputs of the HMC1060LP3E to supply 5 V, connect the appropriate HV pin (HV1, HV2, and HV3 corresponding to outputs VR1, VR2, VR3 respectively) of the HMC1060LP3E to ground, as shown in Figure 15. This output configuration is only supported if PTAT Mode is disabled.

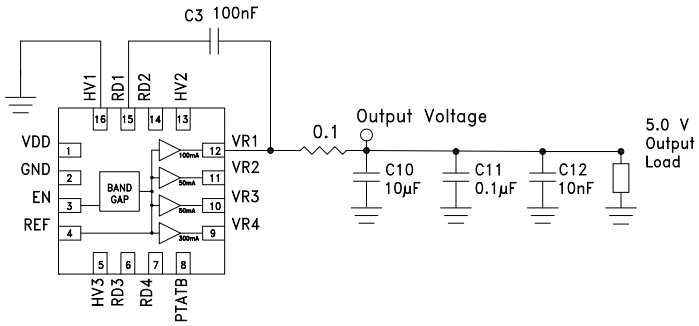

Figure 15. Recommended HMC1060LP3E configuration for supplying 5 V at the output of VR1 pin.[3]

Other output voltages values that are greater than the default value are achieved by using and external resistor Rx as shown in Figure 16. Output configuration in Figure 16 supports both PTAT mode enabled and disabled.

[3] Other outputs (VR2 and VR3) are not shown in this example, but are configured for 5 V output in exactly the same way. VDD input is limited to 5.6 V maximum and 5.3 V minimum.

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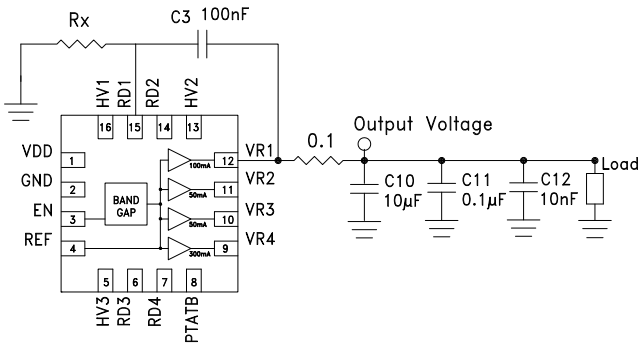

Figure 16. *Recommended HMC1060LP3E configuration for supplying output voltage values greater than default.* [4]

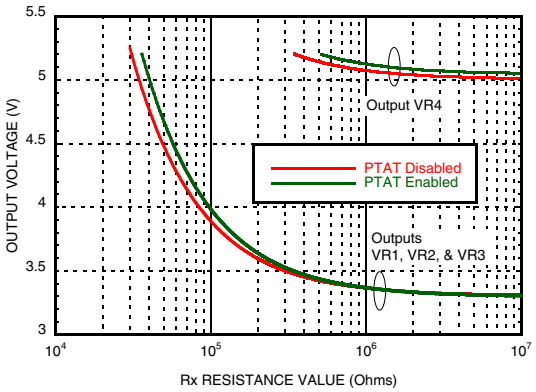

Figure 17. *HMC1060LP3E output voltage as a function of resistance Rx for each output at 27°C.* [5]

Resistance, Rx, required to configure the HMC1060LP3E to the desired output voltage level for each output of the HMC1060LP3E is shown in Figure 17. The exact value of Rx can be calculated using (EQ 2), where internal resistances R1, R2, and band-gap voltage VREF are provided in the Output Configuration Table, and where VRx (x = 1,2,3,4) is the desired output voltage level of each HMC1060LP3E output, as measured at the output pin.

$$R_x = \frac{R_1 R_2}{\left(\frac{VRx}{VREF} - 1\right) R_2 - R_1} \qquad \textbf{(EQ 2)}$$

Configuration Examples

1. To set VR1 = VR2 = VR3 = 5 V in with PTAT Mode disabled, pins HV1, HV2 and HV3 are connected to GND. Note that this configuration is only possible when PTAT Mode is disabled. If similar configuration is required with PTAT Mode enabled, configuration provided in example 3 below must be followed.
2. To set VR1 = VR2 = VR3 = 1.8 V in with PTAT Mode disabled, external resistance Ry = 21 kΩ shown in Figure 13 is required.
3. To set VR1 = 5 V in PTAT Mode, external resistance Rx = 40.3 kΩ shown in Figure 16 is required. Please note that for optimal temperature compensation, the 5 V level on VR1 can be achieved by connecting 5.7 kΩ (40.3 kΩ – R3) from HV1 pin to GND (see Output Configuration Table for more detail). This is due to the fact that the internal resistors of the HMC1060LP3E have a temperature coefficient of +270 ppm/°C. When the default output voltage is modified by using an external resistor with a different temperature coefficient, the temperature behavior of the respective output will differ from this specification, although the difference will likely be insignificant.

Application Information

The HMC1060LP3E ultra low noise regulator features market leading noise performance. It is capable of supplying all of the power needs of Hittite's Wideband PLL with Integrated VCOs products, such as the HMC830LP6GE, by itself. This capability along with market leading noise performance make the HMC1060LP3E an ideal choice for supplying Hittite's broad range of PLL with Integrated VCOs products.

Figure 18 shows a noise comparison between the HMC1060LP3E and a standard off-the-shelf low noise DC power supply. It illustrates the superior noise performance of the HMC1060LP3E at most frequencies.

[4] Example shows the configuration of only VR1 output of the HMC1060LP3E. Other outputs are configured in exactly the same way. VDD input is limited to 5.6 V maximum and Output Voltage + 300 mV minimum.

[5] This curve is accurate only in cases where output voltage greater than default is required. Output voltage is limited to 5.2 V maximum for each output.

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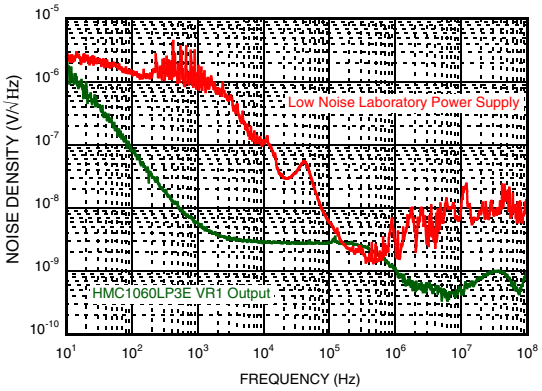

Figure 18. HMC1060LP3E Comparison with typical Low Noise Laboratory DC Power Supply

Superior noise performance shown in Figure 18 can significantly improve performance of components supplied by the HMC1060LP3E. As an example, Figure 19 shows that using the HMC1060LP3E low noise regulator instead of a high quality low noise laboratory power supply can improve the HMC507LP5E VCO phase noise by up to 10 dB.

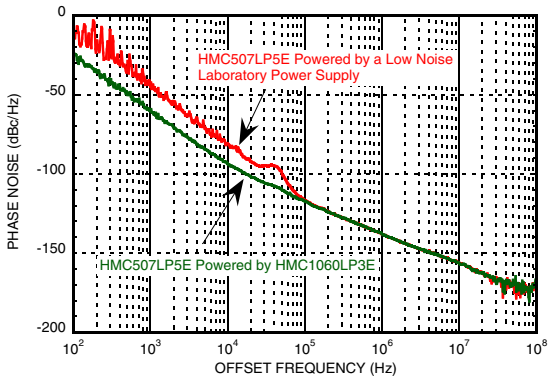

Figure 19. Free running VCO Phase Noise performance of HMC507LP5E VCO operating at 7.19 GHz powered by HMC1060LP3E vs Typical low noise laboratory power supply.

Benefits of PTAT (Proportional To Absolute Temperature)

In addition to market leading noise performance the HMC1060LP3E includes a PTAT (Proportional To Absolute Temperature) feature that enables Hittite's Wideband PLL with Integrated VCOs to achieve maximum Phase Noise and output power performance across all operating temperatures.

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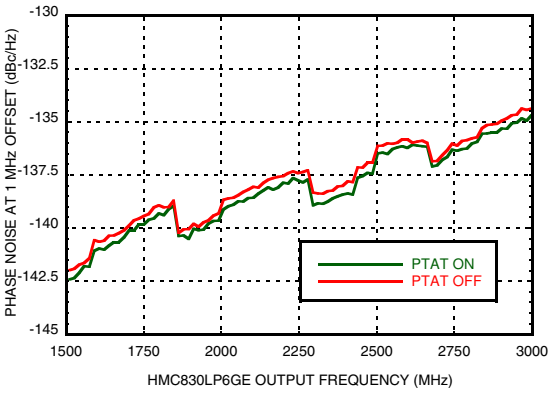

Figure 20. HMC830LP6GE Phase Noise improvement observed as a result of enabling HMC1060LP3E's PTAT Mode.[6]

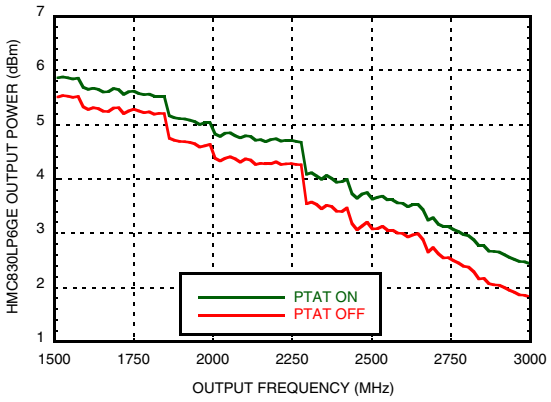

Figure 21. HMC830LP6GE Output Power improvement observed as a result of enabling HMC1060LP3E's PTAT Mode.[6]

In some cases, application circuit performance can be enhanced at high temperatures by increasing the input supply voltage as the temperature increases. The HMC1060LP3E offers a PTAT option that has been designed to improve the performance of Hittite's PLLs with Integrated VCOs. It is also potentially useful in many other applications, but the user needs to verify the performance in a particular application circuit with this mode.

Figure 20 and Figure 21 quantify the benefits of HMC1060LP3E's PTAT mode. Figure 20 shows that the HMC1060LP3E's PTAT mode enables the HMC830LP6GE to achieve 0.5 dB better Phase Noise performance across all operating frequencies at +85°C. Similarly, Figure 21 shows that the HMC1060LP3E's PTAT mode enables the HMC830LP6GE to achieve up to 0.8 dB increase in output power at +85°C across all operating frequencies.

External Enable Pin & Power-Up Timing

The HMC1060LP3E features an external Enable pin (EN) that can be used to enable/disable the outputs of the HMC1060LP3E. This feature is especially useful in complex systems where the power-up and power-down procedure of various subsystems requires precise management. HMC1060LP3E's enable pin (EN) allows the controller to power-cycle and turn on/off all of the circuits and components supplied by the HMC1060LP3E.

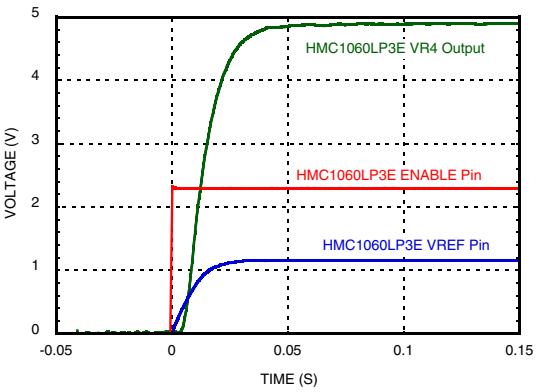

Figure 22. HMC1060LP3E Power up transient using 1 µF capacitor at the VREF input.

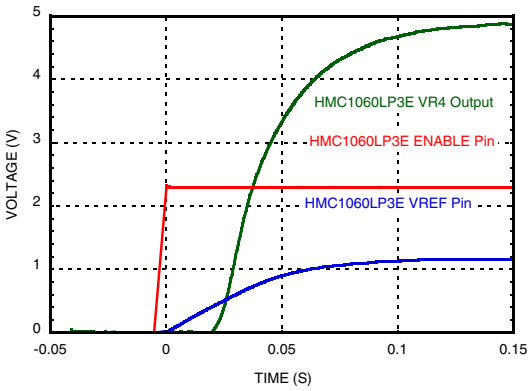

Figure 23. HMC1060LP3E Power up transient using 4.7 µF capacitor at the VREF input.

The power-up/power-down and power-cycle time can be controlled in the HMC1060LP3E by appropriately adjusting the REF pin capacitor (C1 in the Application Schematic). As an example Figure 22 and Figure 23 show that using a 1 µF capacitor on the REF pin of the HMC1060LP3E instead of 4.7 µF can reduce speed of the power up by approximately 15 milliseconds. Figure 2 shows the effect on output noise when C1 is adjusted.

[6] Measured at +85°C. The HMC830LP6GE is powered solely by HMC1060LP3E.

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