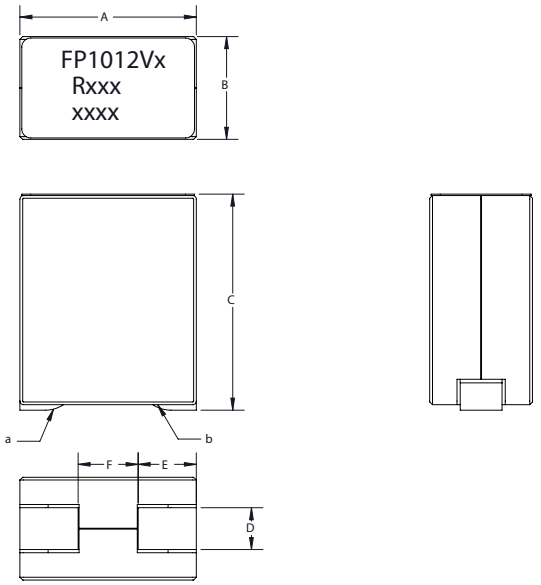
Product specifications

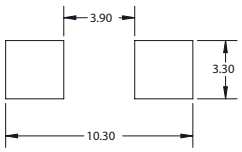
Part number[5]	OCL[1] (nH) ±10%	FLL[2] (nH) minimum	I_{rms}[3] (A)	$I_{sat}1$[4] (A)	$I_{sat}2$[5] (A)	$I_{sat}3$[6] (A)	DCR (mΩ) @ +20 °C ±10%	K-factor[7]
FP1012V2-R100-R	100	72	84	125	105	100	0.125	305
FP1012V2-R120-R	120	86	84	105	88	81	0.125	305
FP1012V2-R150-R	150	108	84	83	70	66	0.125	305
FP1012V2-R330-R	330	231	84	36	28	26	0.125	305

1. Open Circuit Inductance (OCL) Test parameters: 100 kHz, 0.1 Vrms, 0.0 Adc, +25 °C
2. Full Load Inductance (FLL) Test parameters: 100 kHz, 0.1 Vrms, $I_{sat}1$, +25 °C
3. I_{rms}: DC current for an approximate temperature rise of 40 °C without core loss. Derating is necessary for AC currents. PCB layout, trace thickness and width, air-flow, and proximity of other heat generating components will affect the temperature rise. It is recommended that the temperature of the part not exceed +125 °C underworst case operating conditions verified in the end application.
4. $I_{sat}1$: Peak current for approximately 20% rolloff @ +25 °C
5. $I_{sat}2$: Peak current for approximately 20% rolloff @ +100 °C
6. $I_{sat}3$: Peak current for approximately 20% rolloff @ +125 °C
7. K-factor: Used to determine Bp-p for core loss (see graph). Bp-p = K * L * ΔI * 10^{-3}. Bp-p:(Gauss), K: (K-factor from table), L: (Inductance in nH), ΔI (Peak to peak ripple current in Amps).
8. Part Number Definition: FP1012Vx-Rxxx-R
   FP1012 = Product code and size
   Vx= Version indicator
   Rxxx=Inductance value in µH, R=decimal point
   -R suffix = RoHS compliant

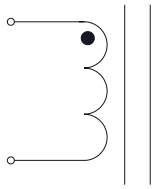
Dimensiuons-mm



Recommended pad layout



Schematic

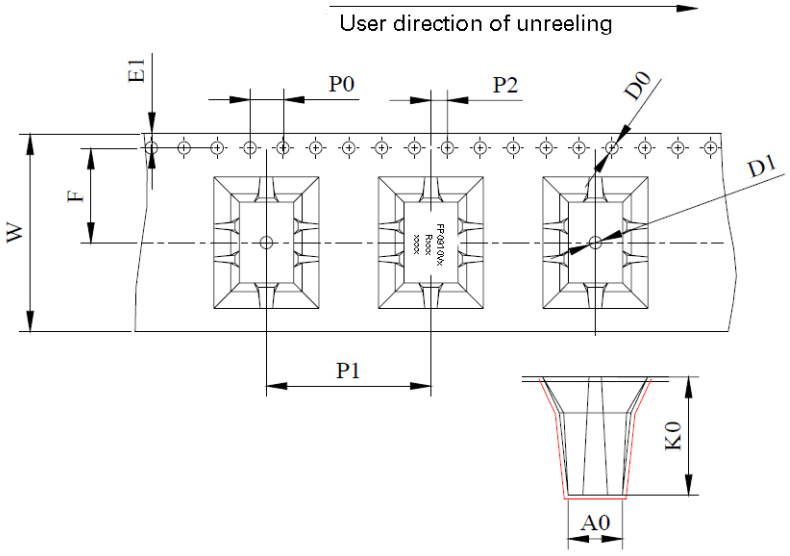


Dimension	
A	10 maximum
B	6.0 maximum
C	12 maximum
D	2.3 nominal
E	3.2 nominal
F	3.3 nominal

Part marking: FP1012=Product code and size, Vx=Version indicator, Rxxx= inductance value in uH, R=decimal point, xxxx= lot code
Tolerances are ±0.15 millimeters unless stated otherwise
All soldering surfaces to be coplanar within 0.1 millimeters
Pad layout tolerances are ±0.1 millimeters unless stated otherwise
DCR is measured from point "a" to point "b"
Do not route traces or vias underneath the inductor

Packaging information- mm

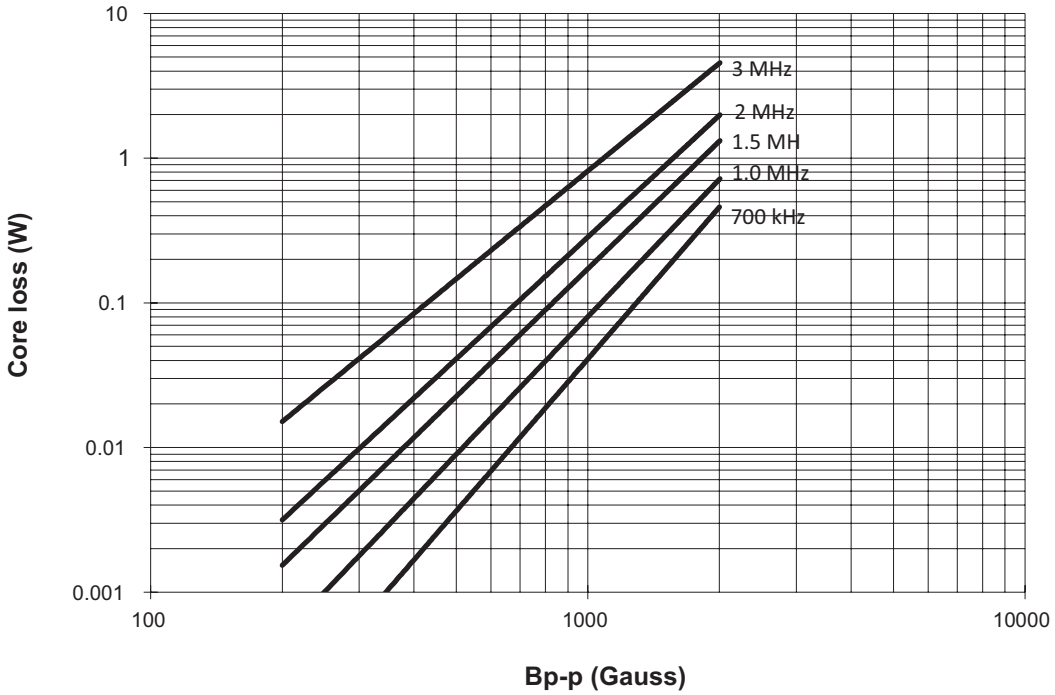
Supplied in tape and reel packaging, 250 parts per 13" diameter reel



W ±0.3	24.00
F±0.1	11.50
E1±0.10	1.75
P0±0.10	4.00
P1±0.10	20.00
P2±0.1	2.00
D0+0.10/-0	1.50
D1+0.10/-0	1.50
A0	6.2±010
B0	10.2±0.10
K0	12.2±0.10
T ±0.05	0.5

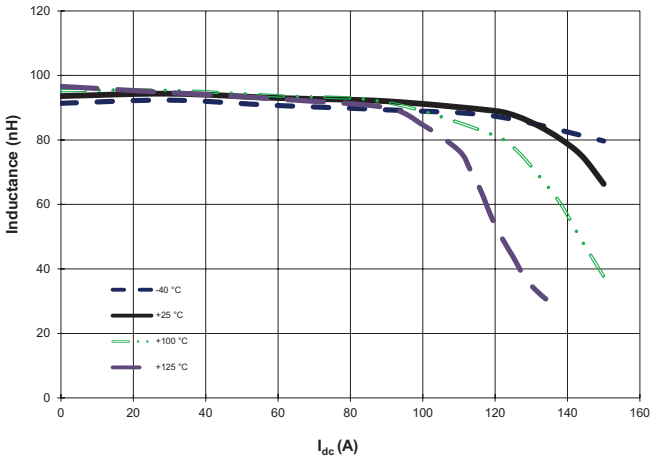
Temperature rise vs. total loss

Core loss vs Bp-p

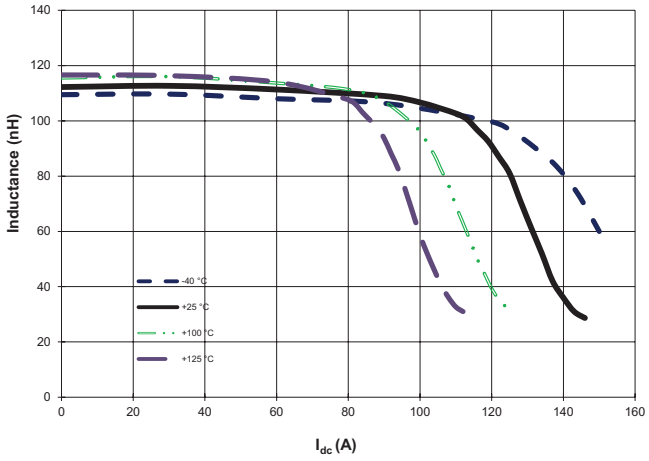


Inductance characteristics

FP1012V2-R100-R

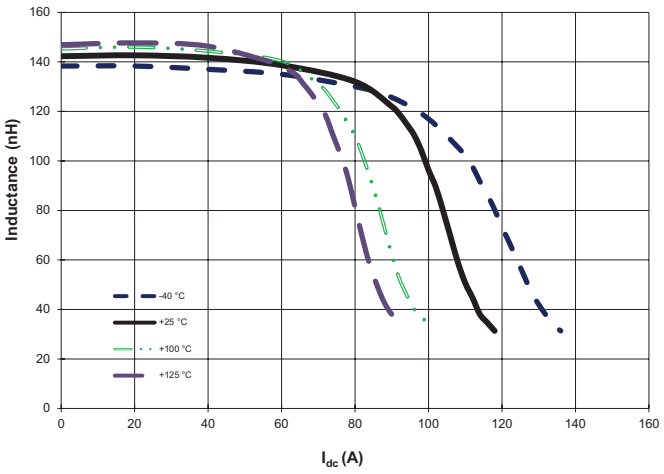


FP1012V2-R120-R

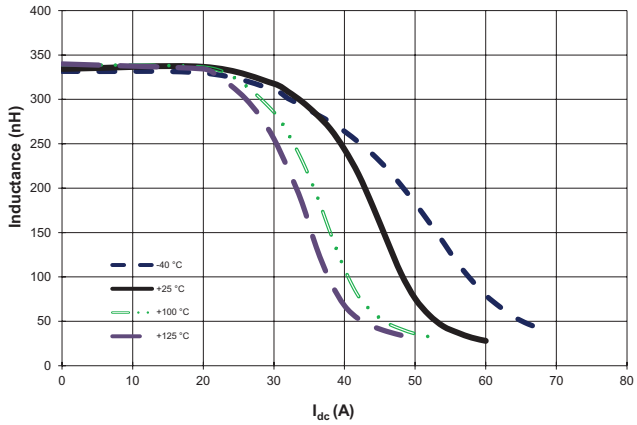


Inductance characteristics

FP1012V2-R150-R



FP1012V2-R330-R



Solder reflow profile

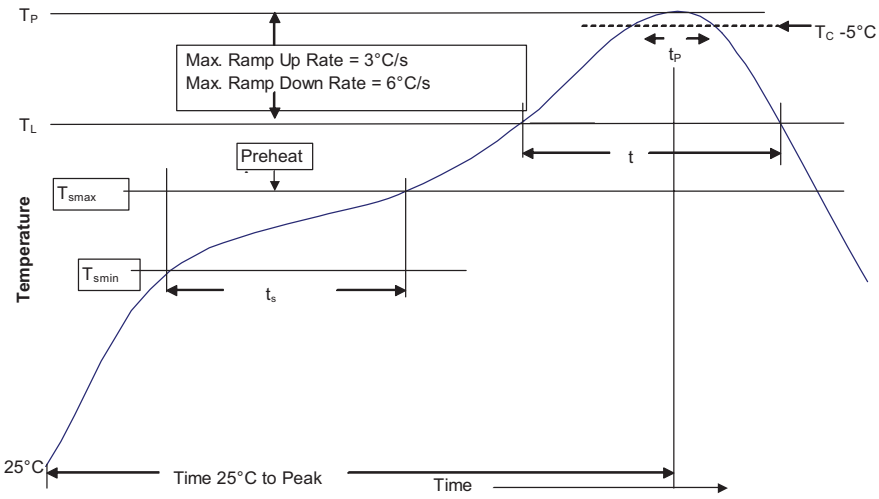


Table 1 - Standard SnPb solder (T_C)

Package thickness	Volume mm3 <350	Volume mm3 ≥350
<2.5 mm)	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2 - Lead (Pb) free solder (T_C)

Package thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 – 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Reference J-STD-020

Profile feature		Standard SnPb solder	Lead (Pb) free solder
Preheat and soak	• Temperature min. (T_{smin})	100 °C	150 °C
	• Temperature max. (T_{smax})	150 °C	200 °C
	• Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp up rate T_{smax} to T_p		3 °C/ second max.	3 °C/ second max.
Liquidous temperature (T_L) Time at liquidous (t_L)		183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_P)*		Table 1	Table 2
Time (t_p)** within 5 °C of the specified classification temperature (T_C)		20 seconds**	30 seconds**
Average ramp-down rate (T_p to T_{smax})		6 °C/ second max.	6 °C/ second max.
Time 25 °C to Peak temperature		6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

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