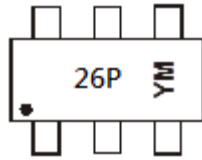


## Marking Information

TSOT26



Shanghai A/T Site

26P = Product Type Marking Code  
 YM = Date Code Marking for SAT (Shanghai Assembly/Test Site)  
 Y or Y = Year (ex: H = 2020)  
 M = Month (ex: 9 = September)

### Date Code Key

Year	2013	...	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	A	...	H	I	J	K	L	M	N	O	P	R

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

## Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-20	V
Gate-Source Voltage	V <sub>GSS</sub>	±8	V
Drain Current (Note 5) Continuous	I <sub>D</sub>	T <sub>A</sub> = +25°C -4.5	A
		T <sub>A</sub> = +70°C -3.7	
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	-20	A
Body-Diode Continuous Current (Note 5)	I <sub>S</sub>	-2.0	A

## Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	1.2	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	Steady State 100	°C/W
		t < 10s 74	
Total Power Dissipation (Note 6)	P <sub>D</sub>	1.8	W
Thermal Resistance, Junction to Ambient (Note 6)	R <sub>θJA</sub>	Steady State 70	°C/W
		t < 10s 46	
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.  
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>STATIC PARAMETERS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	—	—	V	I <sub>D</sub> = -250μA, V <sub>GS</sub> = 0V
Zero Gate Voltage Drain Current @ T <sub>J</sub> = +55°C (Note 8)	I <sub>DSS</sub>	—	—	-1 -10	μA	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V
Zero Gate Voltage Drain Current @ T <sub>J</sub> = +150°C (Note 8)	I <sub>DSS</sub>	—	—	-100	μA	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V
Gate-Body Leakage Current	I <sub>GSS</sub>	—	—	±100	nA	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±8V
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.4	—	-1.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	25 33	45 65	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.5A V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -3.8A
Static Drain-Source On-Resistance @ T <sub>J</sub> = +125°C (Note 8)	R <sub>DS(ON)</sub>	—	—	72	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.5A
Diode Forward Voltage	V <sub>SD</sub>	-0.5	-0.72	-1.4	V	I <sub>S</sub> = -2.1A, V <sub>GS</sub> = 0V
On State Drain Current (Note 8)	I <sub>D(ON)</sub>	10	—	—	A	V <sub>DS</sub> ≤ 5V, V <sub>GS</sub> = 4.5V
<b>DYNAMIC PARAMETERS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	1,496	2,990	pF	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	130	260	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	116	230	pF	
Total Gate Charge	Q <sub>G</sub>	—	14.4	25	nC	V <sub>DS</sub> = -10V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.5A
Gate-Source Charge	Q <sub>GS</sub>	—	2.6	5		
Gate-Drain Charge	Q <sub>GD</sub>	—	2.7	5.5		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	8.5	30	ns	V <sub>DS</sub> = -5V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -1A, R <sub>G</sub> = 6.0Ω
Rise Time	t <sub>R</sub>	—	11	60		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	61	130		
Fall Time	t <sub>F</sub>	—	25	100		

Notes: 7. Short duration pulse test used to minimize self-heating effect.  
 8. Guaranteed by design. Not subject to product testing.

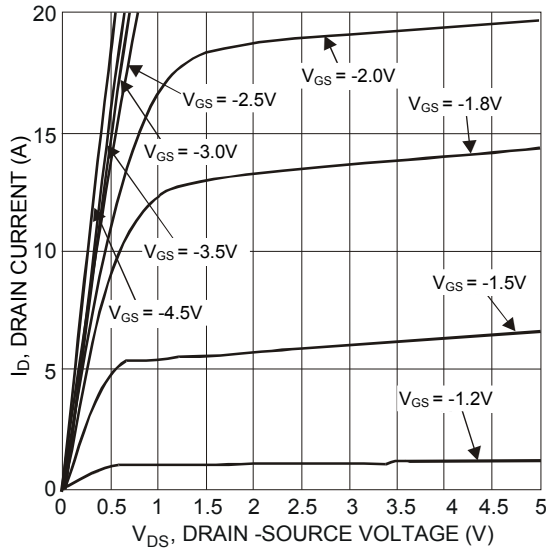


Figure 1 Typical Output Characteristics

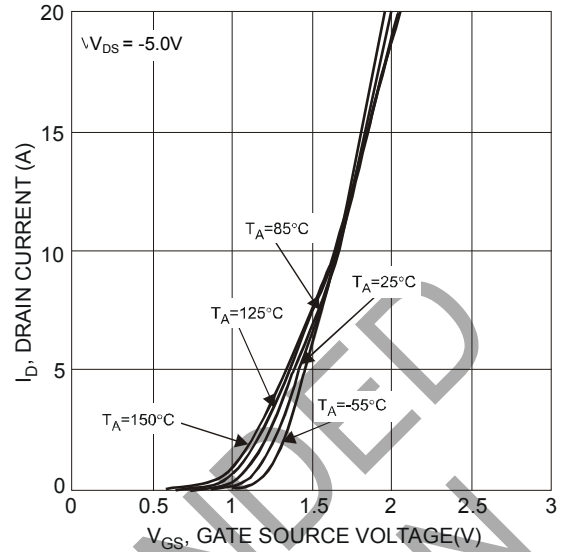


Figure 2 Typical Transfer Characteristics

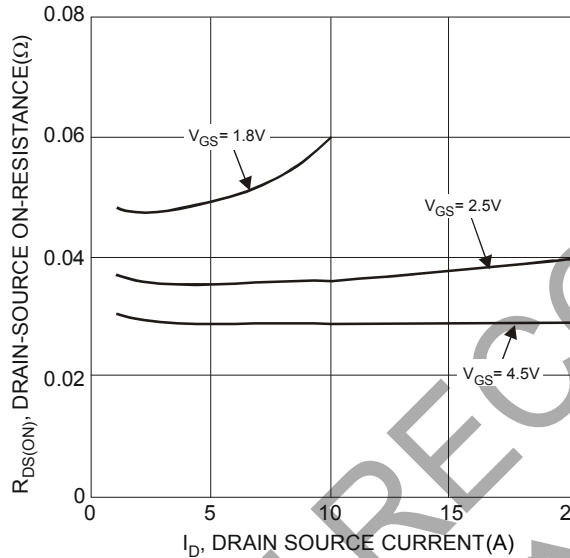


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

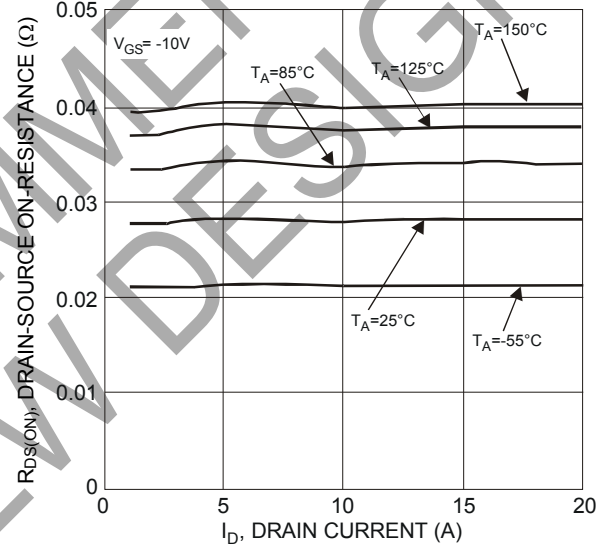


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

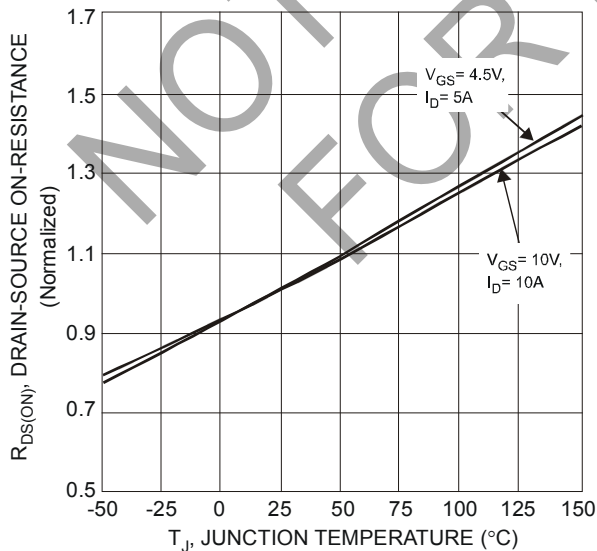


Figure 5 On-Resistance Variation with Temperature

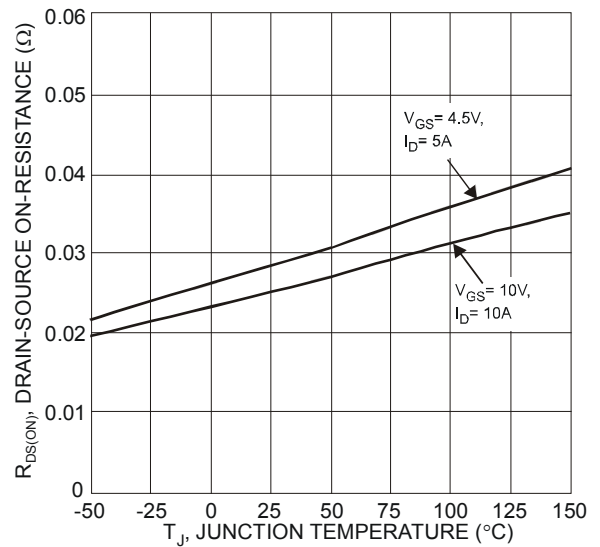


Figure 6 On-Resistance Variation with Temperature

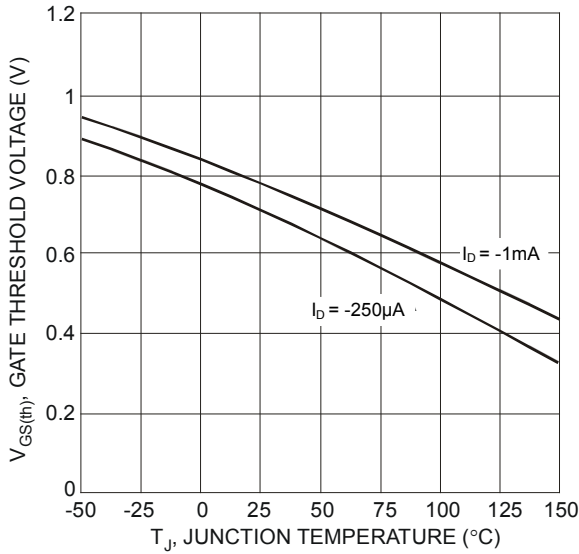


Figure 7 Gate Threshold Variation vs. Junction Temperature

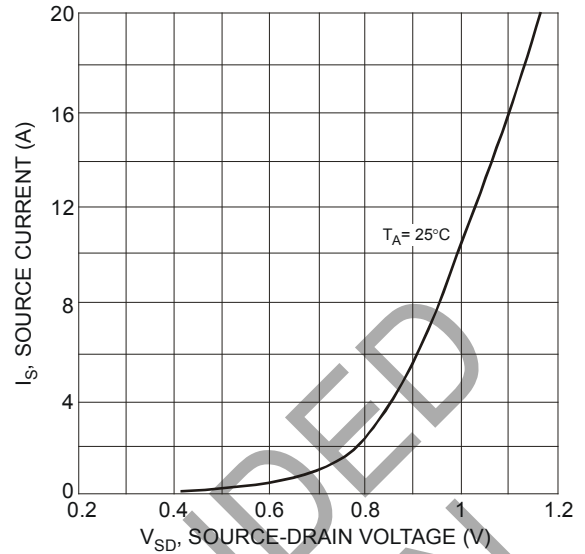


Figure 8 Diode Forward Voltage vs. Current

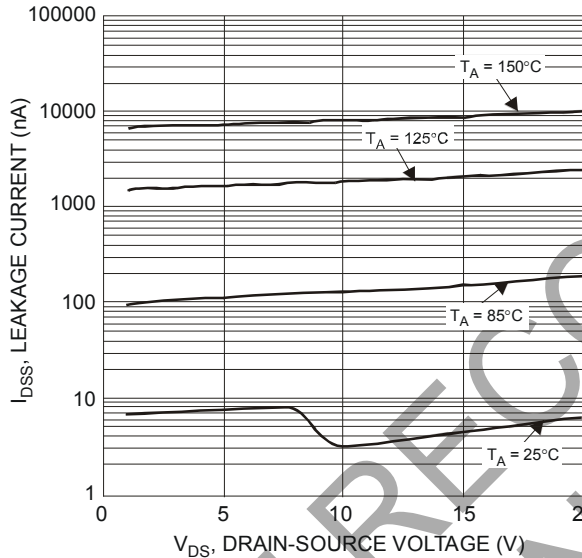


Figure 9 Typical Drain-Source Leakage Current vs. Voltage

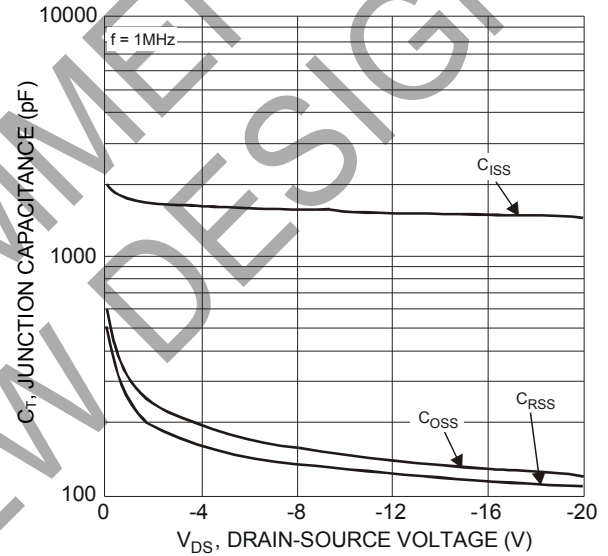


Figure 10 Typical Junction Capacitance

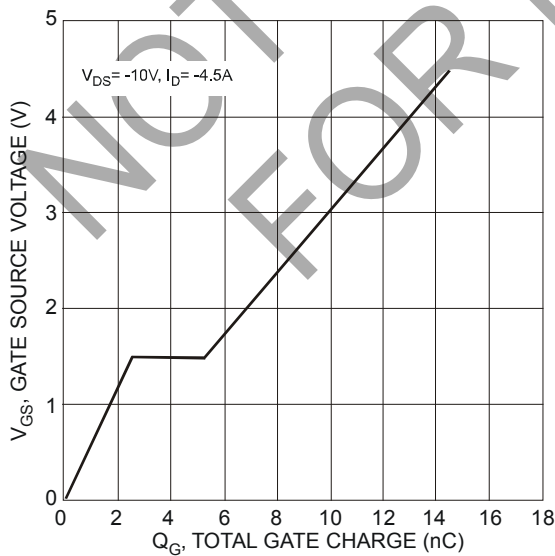
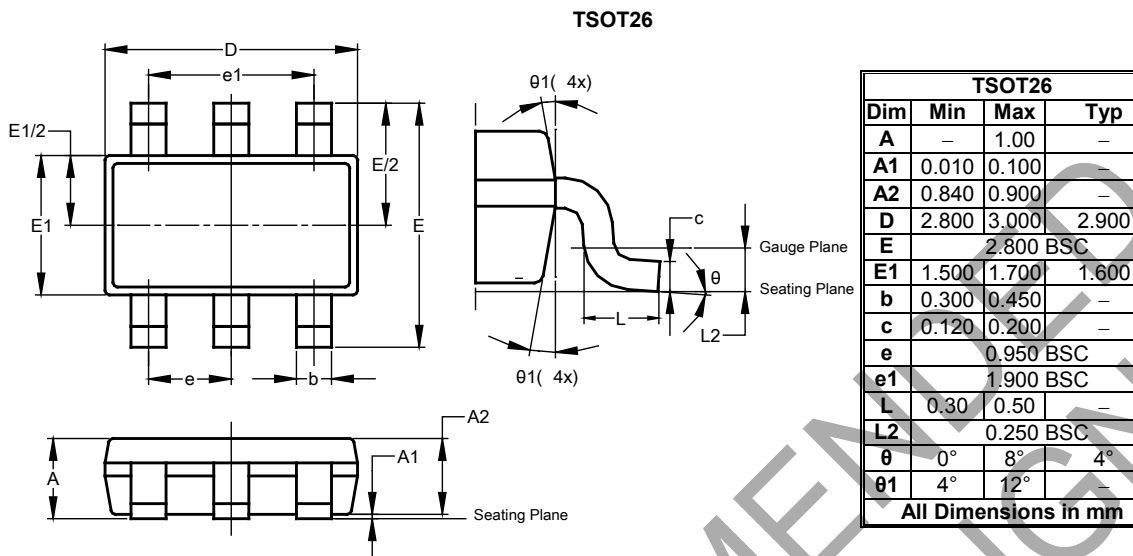


Figure 11 Gate Charge Characteristics

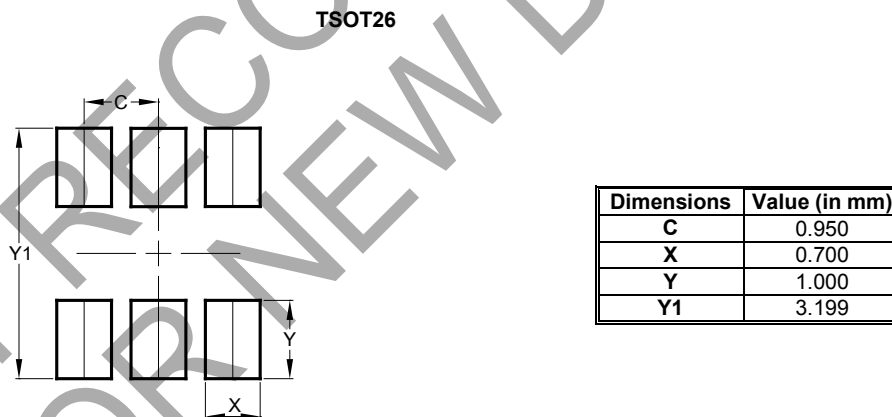
## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



## Suggested Pad Layout

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