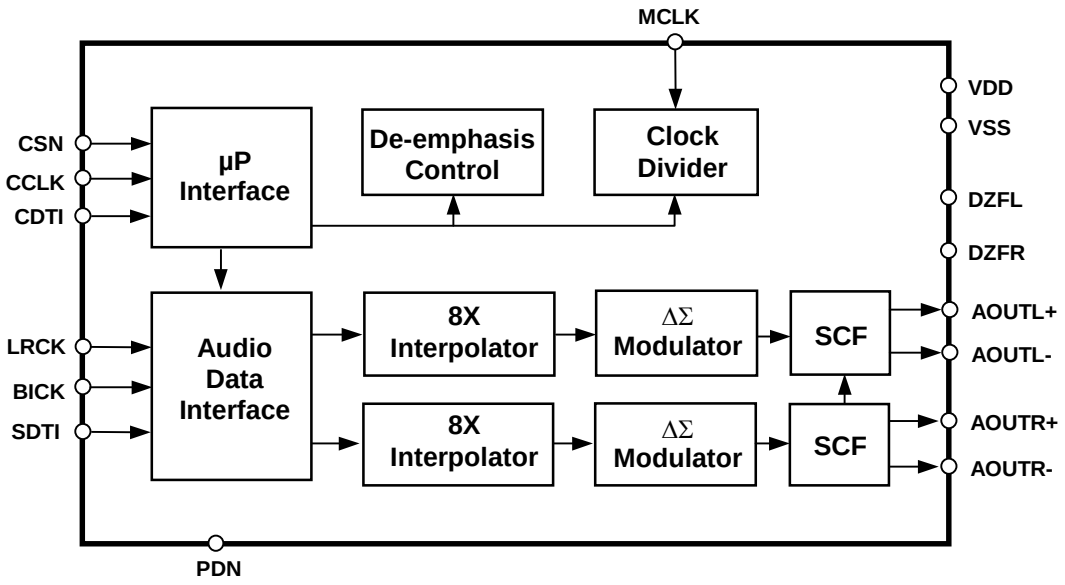
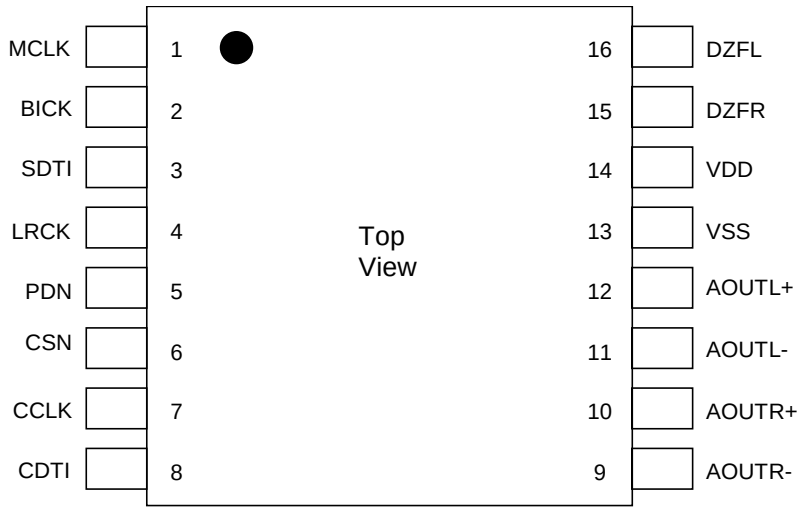


■ Ordering Guide

AK4482VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4482	Evaluation board for AK4482	

■ Pin Layout



PIN/Function

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power-Down Mode Pin When at "L", the AK4482 is in the power-down mode and is held in reset. The AK4482 should always be reset upon power-up.
6	CSN	I	Chip Select Pin
7	CCLK	I	Control Data Input Pin
8	CDTI	I	Control Data Input Pin
9	AOUTR-	O	Rch Negative Analog Output Pin
10	AOUTR+	O	Rch Positive Analog Output Pin
11	AOUTL-	O	Lch Negative Analog Output Pin
12	AOUTL+	O	Lch Positive Analog Output Pin
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin
15	DZFR	O	Rch Data Zero Input Detect Pin
16	DZFL	O	Lch Data Zero Input Detect Pin

Note 1. All input pins must not be left floating.

ABSOLUTE MAXIMUM RATING

(VSS=0V; Note 2)

Parameter	Symbol	min	max	Unit
Power Supply	VDD	-0.3	6.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 2. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 2)

Parameter	Symbol	min	typ	max	Unit
Power Supply	VDD	4.75	5.0	5.25	V

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta = 25°C; VDD = 5.0V; fs = 44.1kHz; BICK = 64fs; Signal Frequency = 1kHz; 24bit Input Data; Measurement frequency = 20Hz ~ 20kHz; R_L ≥2kΩ; unless otherwise specified)

Parameter			min	typ	max	Unit
Resolution					24	Bits
Dynamic Characteristics (Note 3)						
THD+N	fs=44.1kHz	0dBFS		-100	-90	dB
	BW=20kHz	-60dBFS		-48	-	dB
	fs=96kHz	0dBFS		-97	-90	dB
	BW=40kHz	-60dBFS		-45	-	dB
	fs=192kHz	0dBFS		-97	-	dB
	BW=40kHz	-60dBFS		-45	-	dB
Dynamic Range (-60dBFS with A-weighted) (Note 4)			105	111		dB
S/N (A-weighted) (Note 5)			105	111		dB
Interchannel Isolation (1kHz)			90	110		dB
Interchannel Gain Mismatch				0.2	0.5	dB
DC Accuracy						
Gain Drift				100	-	ppm/°C
Output Voltage (Note 6)			±2.25	±2.4	±2.55	Vpp
Load Resistance (Note 7)			2			kΩ
Power Supplies						
Power Supply Current (VDD)						
Normal Operation (PDN = "H", fs=44.1kHz)				20	30	mA
Double Operation (PDN = "H", fs=96kHz)				24	36	mA
Quad Operation (PDN = "H", fs=192kHz)				30	45	mA
Power-Down Mode (PDN = "L") (Note 8)				10	100	μA

Note 3. Measured by Audio Precision, System Two. Refer to the evaluation board manual.
Note 4. 100dB at 16bit data.
Note 5. S/N does not depend on input data size.
Note 6. Full-scale voltage(0dB). Output voltage scales with the VDD voltage.
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = ±2.4Vpp×VDD/5
Note 7. Regarding Load Resistance, AC load is 4kΩ (min) with a DC cut capacitor.
Note 8. All digital input pins including (MCLK, BICK and LRCK) are fixed to VDD or VSS.

SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD = 4.75 ~ 5.25V; fs = 44.1kHz; SD = "0"; SLOW = "0")

Parameter			Symbol	min	typ	max	Unit
Digital filter							
Passband	±0.05dB (Note 9)		PB	0		20.0	kHz
	-6.0dB			-	22.05	-	kHz
Stopband	(Note 9)		SB	24.1			kHz
Passband Ripple			PR	-0.005		± 0.0001	dB
Stopband Attenuation			SA	70			dB
Group Delay	(Note 10)		GD	-	27	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.1kHz	FR	-	-0.2/+0.2	-	dB
	40.0kHz	fs=96kHz	FR	-	-0.3/+0.3	-	dB
	80.0kHz	fs=192kHz	FR	-	-1/+0.1	-	dB

Note 9. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 10. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD = 4.75~5.25V; fs = 44.1kHz; SD = "0"; SLOW = "1")

Parameter			Symbol	min	typ	max	Unit
Digital Filter							
Passband	±0.04dB (Note 11)		PB	0		8.1	kHz
	-3.0dB			-	18.2	-	kHz
Stopband	(Note 11)		SB	39.2			kHz
Passband Ripple			PR	-0.07		+0.02	dB
Stopband Attenuation			SA	72			dB
Group Delay	(Note 10)		GD	-	27	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	-5/+0.1	-	dB
	40.0kHz	fs=96kHz	FR	-	-4/+0.1	-	dB
	80.0kHz	fs=192kHz	FR	-	-5/+0.1	-	dB

Note 11. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.185×fs (@±0.04dB), SB=0.888×fs.

SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD = 4.75 ~ 5.25V; fs = 44.1kHz; SD = "1"; SLOW = "0")

Parameter			Symbol	min	typ	max	Unit
Digital filter							
Passband	±0.05dB (Note 9)		PB	0		20.0	kHz
	-6.0dB			-	22.05	-	kHz
Stopband	(Note 9)		SB	24.1			kHz
Passband Ripple			PR	-0.0080		+0.0016	dB
Stopband Attenuation			SA	56.5			dB
Group Delay	(Note 10)		GD	-	6	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.1kHz	FR	-	-0.2/+0.2	-	dB
	40.0kHz	fs=96kHz	FR	-	-0.3/+0.3	-	dB
	80.0kHz	fs=192kHz	FR	-	-1/+0.1	-	dB

Note 9. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 10. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

SHORT DELAY SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD = 4.75~5.25V; fs = 44.1kHz; SD = "1"; SLOW = "1")

Parameter			Symbol	min	typ	max	Unit
Digital Filter							
Passband	±0.04dB (Note 11)		PB	0		8.1	kHz
	-3.0dB			-	18.2	-	kHz
Stopband	(Note 11)		SB	39.2			kHz
Passband Ripple			PR	0.00		0.02	dB
Stopband Attenuation			SA	62.4			dB
Group Delay	(Note 10)		GD	-	5	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0.1/-5	-	dB
	40.0kHz	fs=96kHz	FR	-	+0.1/-4	-	dB
	80.0kHz	fs=192kHz	FR	-	+0.1/-5	-	dB

Note 11. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.185×fs (@±0.04dB), SB=0.888×fs.

DC CHARACTERISTICS

(Ta = 25°C; VDD = 4.75 ~ 5.25V)

Parameter		Symbol	min	typ	max	Unit
High-Level Input Voltage		VIH	2.2	-	-	V
Low-Level Input Voltage		VIL	-	-	0.8	V
High-Level Output Voltage	(Iout = -80μA)	VOH	VDD-0.4	-	-	V
Low-Level Output Voltage	(Iout = 80μA)	VOL	-		0.4	V
Input Leakage Current		Iin	-	-	± 10	μA

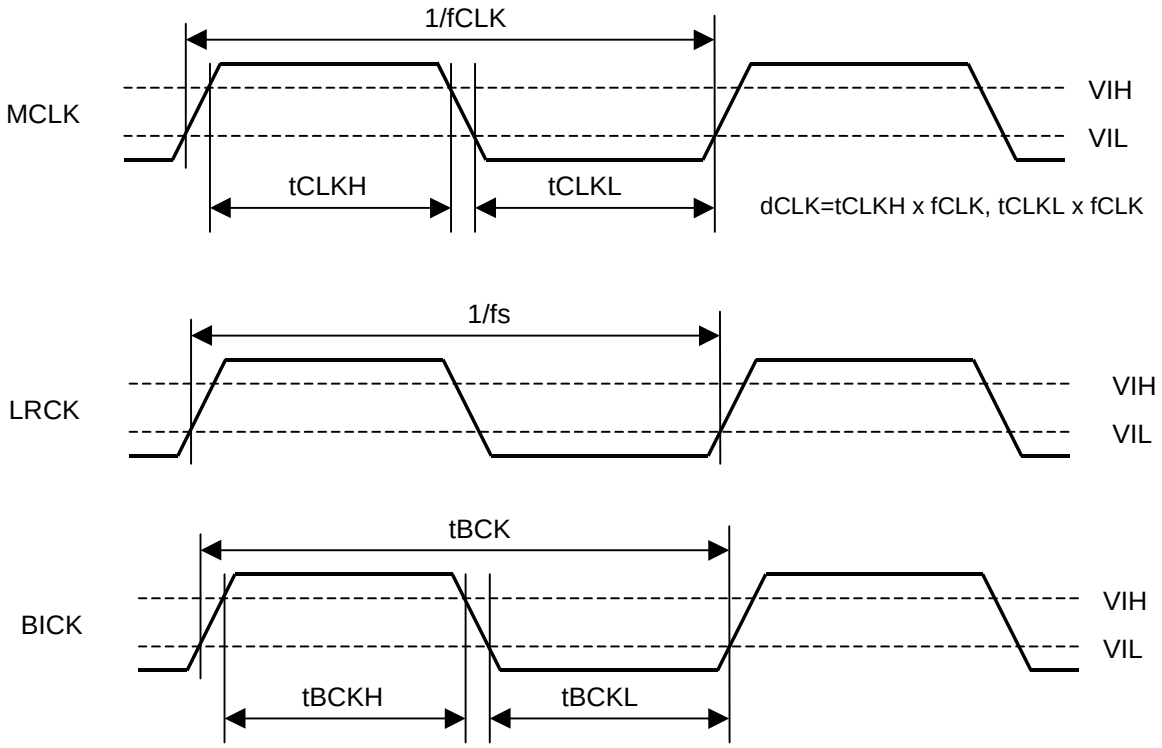
SWITCHING CHARACTERISTICS

(Ta = 25°C; VDD = 4.75 ~ 5.25V; C_L = 20pF)

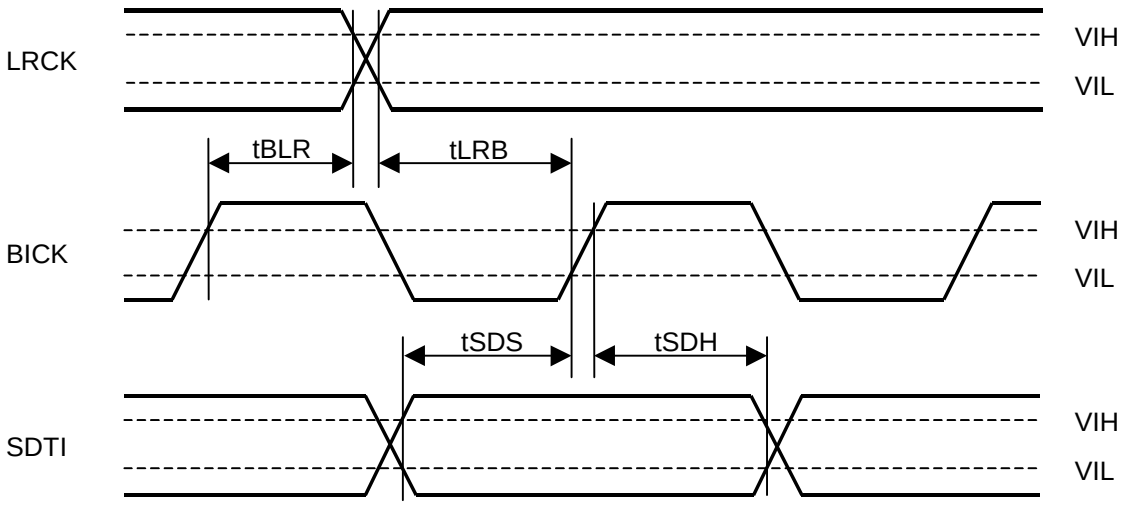
Parameter	Symbol	min	typ	max	Unit
Master Clock Frequency	fCLK	2.048	11.2896	41.472	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency					
Normal Speed Mode	fsn	8		54	kHz
Double Speed Mode	fsd	60		108	kHz
Quad Speed Mode	fsq	120		216	kHz
Duty Cycle	Duty	45		55	%
Audio Interface Timing					
BICK Period					
Normal Speed Mode	tBCK	1/128fs			ns
Double/Quad Speed Mode	tBCK	1/64fs			ns
BICK Pulse Width Low	tBCKL	30			ns
Pulse Width High	tBCKH	30			ns
BICK "↑" to LRCK Edge (Note 12)	tBLR	20			ns
LRCK Edge to BICK "↑" (Note 12)	tLRB	20			ns
SDTI Hold Time	tSDH	20			ns
SDTI Setup Time	tSDS	20			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Reset Timing					
PDN Pulse Width (Note 13)	tPD	150			ns

Note 12. BICK rising edge must not occur at the same time as LRCK edge.
Note 13. The AK4480 can be reset by bringing the PDN pin "L" to "H" upon power-up.

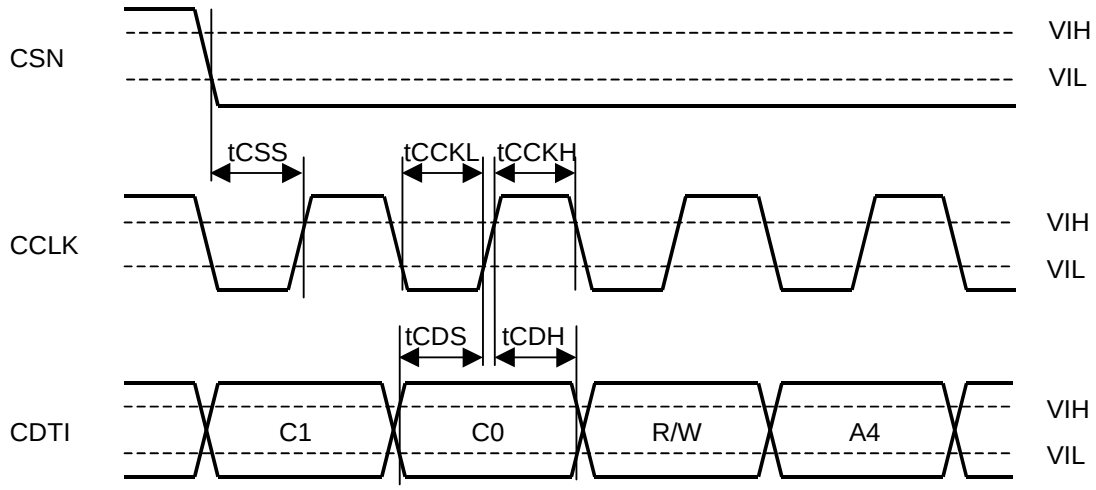
■ Timing Diagram



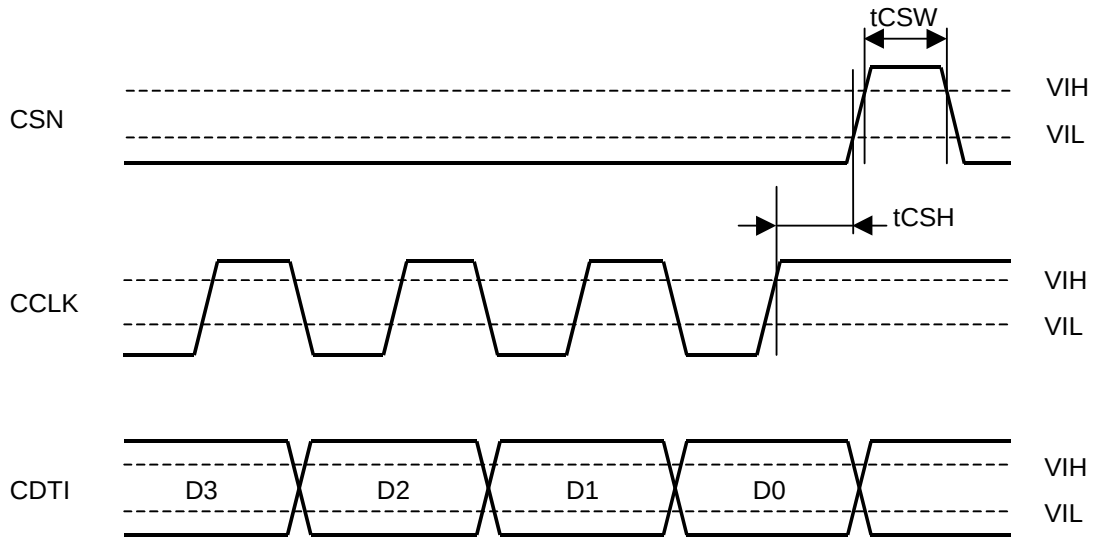
Clock Timing



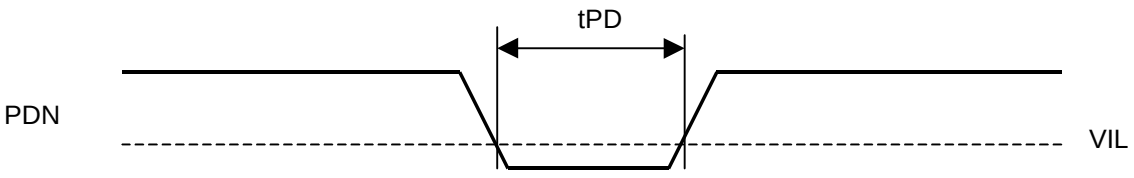
Serial Interface Timing



WRITE Command Input Timing



WRITE Data Input Timing



Power-down Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4482, are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two modes for setting MCLK frequency, Manual Setting Mode and Auto Setting Mode. In manual setting mode (ACKS bit = "0": Register 00H), sampling speed is set by DFS1-0 bits (Table 1) and the MCLK frequency in each speed mode is set automatically (Table 2~Table 4). The AK4482 is in auto setting mode when a reset is released (PDN = "↑"). In auto setting mode, sampling speed and MCLK frequency are detected automatically (Table 5). Then the initial master clock is set to the appropriate frequency (Table 6) so that DIF1-0 bits setting are not necessary.

The AK4482 is automatically placed in power saving mode when MCLK or LRCK is stopped during normal operation, and the analog output goes to AVDD/2 (typ). When MCLK and LRCK are input again, the AK4482 is powered up. After exiting reset following power-up, the AK4482 is not fully operational until MCLK and LRCK are input.

DFS1 bit	DFS0 bit	Sampling Rate (fs)		
0	0	Normal Speed Mode	8kHz~54kHz	(default)
0	1	Double Speed Mode	60kHz~108kHz	
1	0	Quad Speed Mode	120kHz~216kHz	

Table 1. Sampling Speed (Manual Setting Mode)

LRCK	MCLK				BICK
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK		BICK
fs	128fs	192fs	64fs
176.4kHz	22.5792MHz	33.8688MHz	11.2896MHz
192.0kHz	24.5760MHz	36.8640MHz	12.2880MHz

Table 4. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 5. Sampling Speed (Auto Setting Mode: Default)

LRCK	MCLK (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	-	-	16.3840	24.5760	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	

Table 6. System Clock Example (Auto Setting Mode)

■ Audio Serial Interface Format

Data is shifted in via the SDTI pin using BICK and LRCK inputs. Five data formats are supported and selected by the DIF2-0 bits as shown in Table 7. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20-bit and 16-bit MSB justified formats by zeroing the unused LSBs.

Mode	DIF2 bit	DIF1 bit	DIF0 bit	SDTI Format	BICK	Figure	
0	0	0	0	16bit LSB justified	≥32fs	Figure 1	
1	0	0	1	20bit LSB justified	≥40fs	Figure 2	
2	0	1	0	24bit MSB justified	≥48fs	Figure 3	(default)
3	0	1	1	24bit I^2S Compliment	≥48fs	Figure 4	
4	1	0	0	24bit LSB justified	≥48fs	Figure 2	

Table 7. Audio Data Format

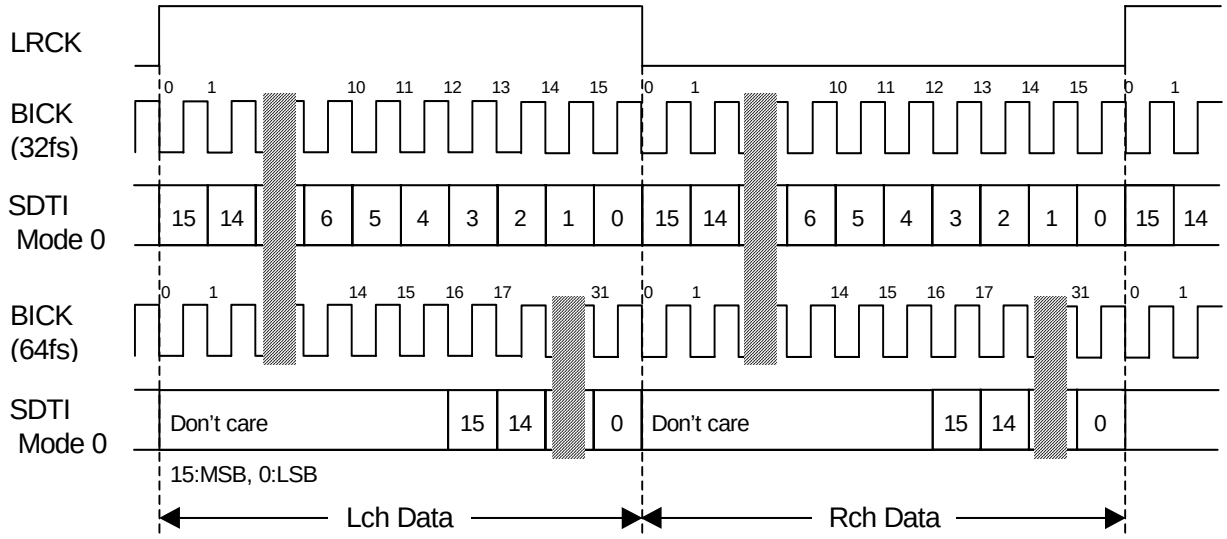


Figure 1. Mode 0 Timing

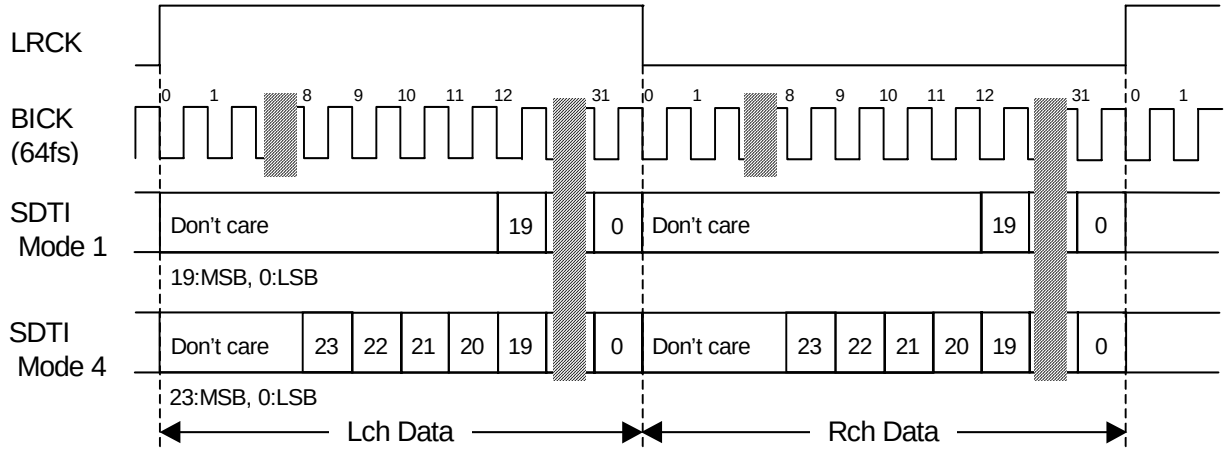


Figure 2. Mode 1, 4 Timing

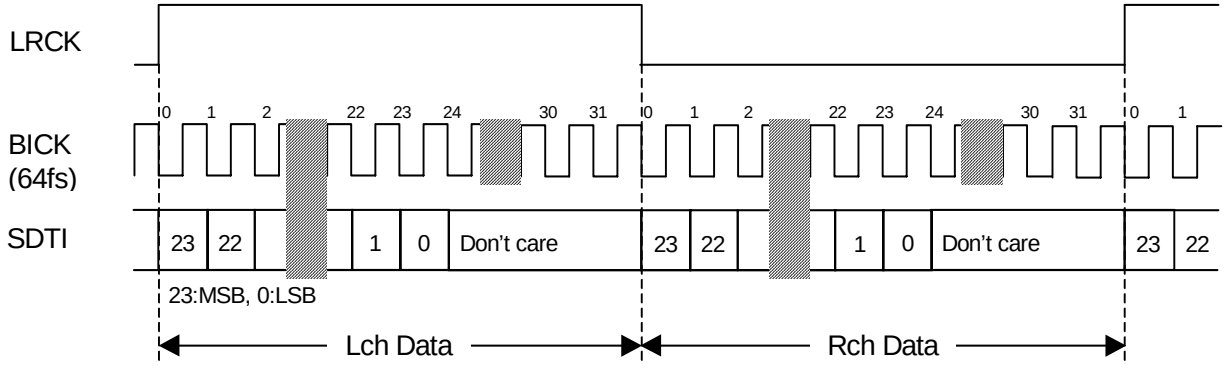


Figure 3. Mode 2 Timing

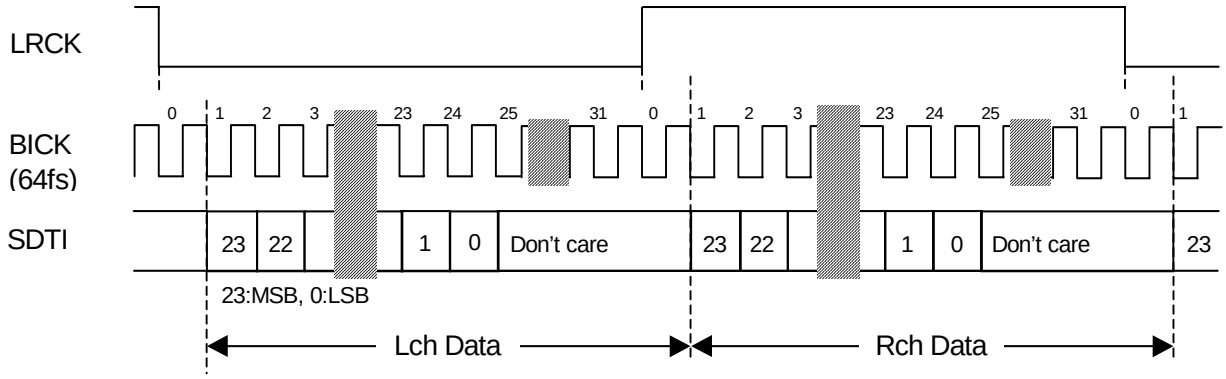


Figure 4. Mode 3 Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32kHz, 44.1kHz or 48kHz sampling rates (tc = 50/15µs). It is enabled and disabled with DEM1-0 bits. In double speed mode and quad speed mode, the digital de-emphasis filter is off.

DEM1 bit	DEM0 bit	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 8. De-emphasis Filter Control (Normal Speed Mode)

■ Output Volume

The AK4482 includes channel independent digital output volume control (ATT) with 256 levels at linear step including MUTE. This volume control is in front of the DAC and it can attenuate the input data from 0dB to –48dB and mute. When changing output levels, transitions are executed in soft change; thus no switching noise occurs during these transitions. Transition times when changing one level and all levels are shown below.

Sampling Speed	Transition Time	
	1 Level	256 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

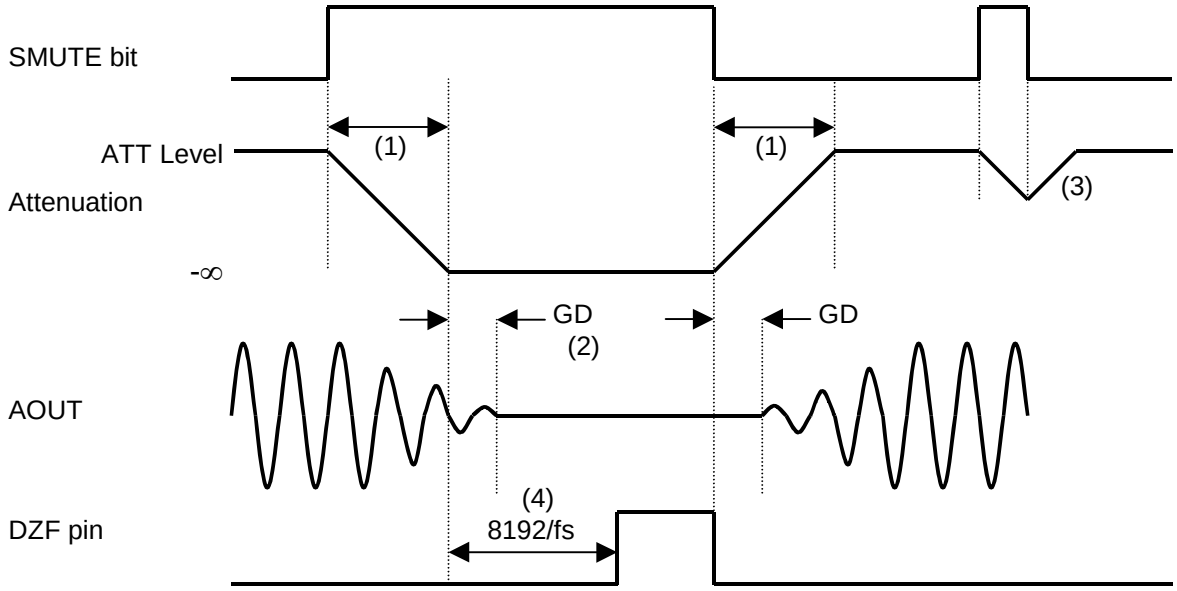
Table 9. ATT Transition Time

■ Zero Detection

The AK4482 has channel-independent zero detect function. When the input data at each channel is continuously zeros for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin of each channel immediately returns to "L" if the input data of each channel is not zero after becoming "H". When the RSTN bit is "0", the DZF pins of both channels become "H". The DZF pins of both channels become "L" in 4 ~ 5/fs if the input data are not "0" after RSTN bit returns to "1". The DZF pins of both channels go to "H" only if the input data for both channels are continuously zeros for 8192 LRCK cycles when DZFM bit is set to "1". The zero detect function can be disabled by setting the DZFE bit. In this case, DZF pins of both channels are always "L". The DZFB bit can invert the polarity of the DZF pin.

■ Soft Mute Operation

The soft mute operation is performed at digital domain. When the SMUTE bit set to "1", the output signal is attenuated by −∞ during ATT_DATA × ATT transition time (Table 9) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time. If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Note:
(1) ATT_DATA × ATT transition time (Table 9). For example, this time is 1020LRCK cycles (1020/fs) at ATT_DATA=255 in Normal Speed Mode.
(2) The analog output corresponding to the digital input has group delay (GD).
(3) If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.
(4) When the input data for each channel is continuously zeros for 8192 LRCK cycles, the DZF pin for each channel goes to "H". The DZF pin immediately returns to "L" if input data are not zero.

Figure 5. Soft Mute and Zero Detection Function

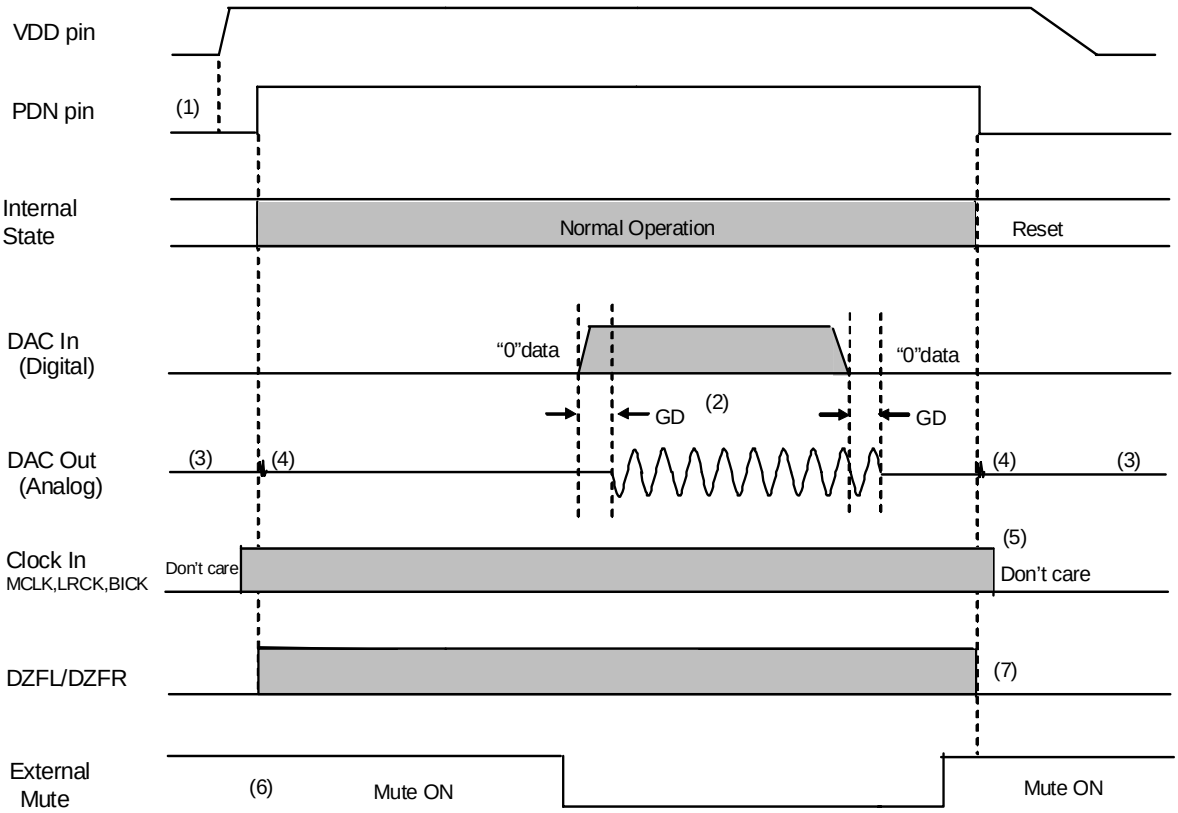
■ System Reset

The AK4482 should be reset once by bringing the PDN pin = "L" upon power-up. The reset and power-down mode are released by MCLK input, and the internal timing starts clocking by a rising edged of LRCK after exiting the power down mode by MCLK. The AK4482 is in power-down state until MCLK and LRCK are input.

■ Power ON/OFF Timing

The AK4482 is placed in power-down mode by bringing the PDN pin "L" and the registers are initialized. The analog outputs are floating (Hi-Z). As some click noise occurs at the edge of the PDN signal, the analog output should be muted externally if the click noise influences system application.

The AK4482 can be reset by setting RSTN bit to "0". In this case, the registers are not initialized and the corresponding analog outputs become 2.3V(@VDD=5V) (typ). As some click noise occurs at the edge of RSTN signal, the analog output should be muted externally if the click noise influences system application.



Notes:

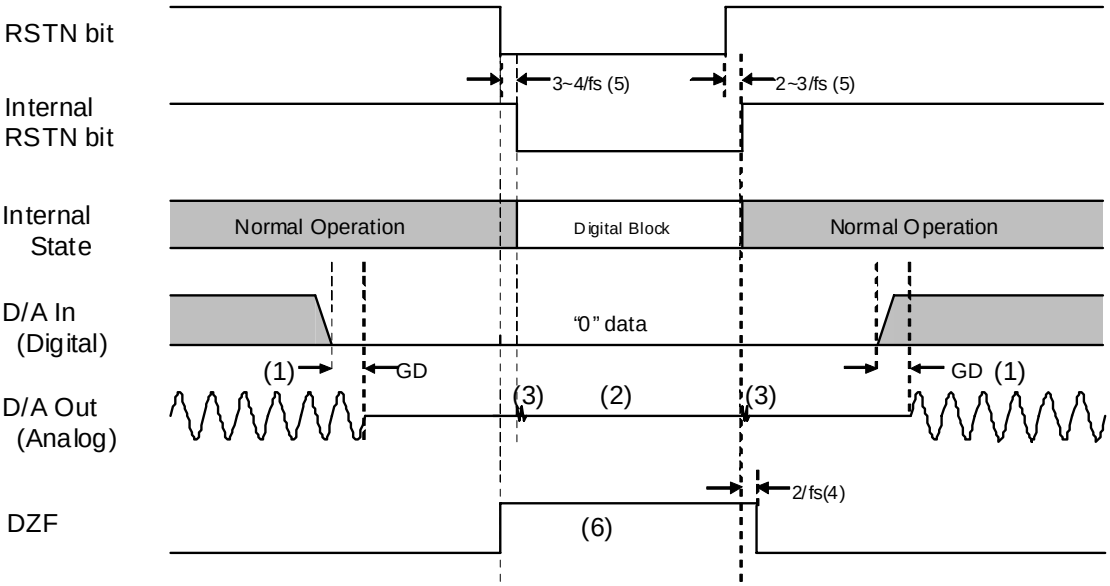
(1) After VDD is powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) Analog outputs are floating (Hi-Z) in power-down mode.
(4) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(5) MCLK, BICK and LRCK clocks can be stopped in power-down mode (PDN pin= "L").
(6) Mute the analog output externally if click noise (4) adversely affect system performance
The timing example is shown in this figure.
(7) DZFL/R pins are "L" in the power-down mode (PDN pin = "L").

Figure 6. Power-down/up Sequence Example

■ Reset Function

(1) RESET by RSTN bit = "0"

When RSTN bit = "0", the AK4482's digital section is powered down but the internal register values are not initialized. The analog outputs become VCML/R voltage and DZF pins of both L and R channels become "H". Figure 7 shows the example of reset by RSTN bit.



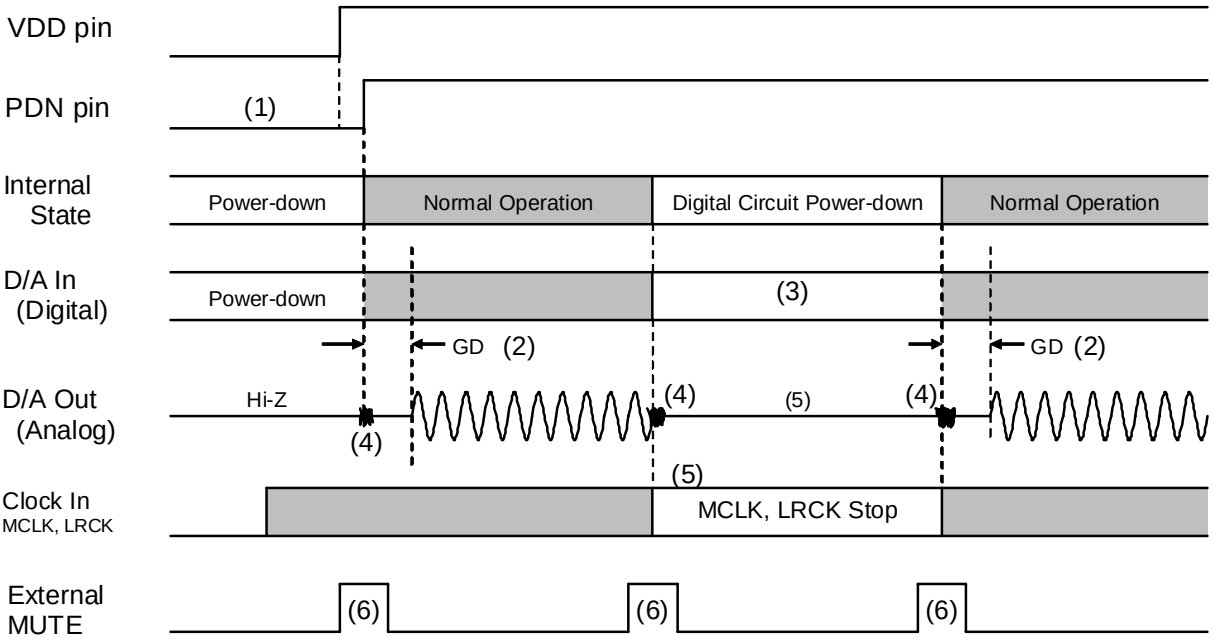
Note:

(1) The analog output corresponding to digital input has group delay (GD).
(2) The analog outputs are 2.3V(@VDD=5.0 typ.) when RSTN bit = "0".
(3) Click noise occurs at the edges ("↑ ↓") of the internal timing of RSTN bit.
This noise is output even if "0" data is input.
(4) The DZF pins become "H" when the RSTN bit is set to "0", and return to "L" in 2/fs after the RSTN bit is changed to "1".
(5) There is a delay, 3 ~ 4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2 ~ 3/fs from RSTN bit "1" to the internal RSTN bit "1".
(6) Mute the analog output externally if click noise (3) or Hi-z output (2) influences system applications. The timing example is shown in this figure.

Figure 7. Reset Timing Example

(2) RESET by MCLK or LRCK/WCK stop

The AK4482 is automatically placed in reset state when MCLK or LRCK is stopped during PCM mode (RSTN pin ="H"), and the analog outputs become floating (Hi-z). When MCLK and LRCK are input again, the AK4482 exit reset state and starts the operation. Zero detect function is not available when MCLK or LRCK is stopped.



Notes:

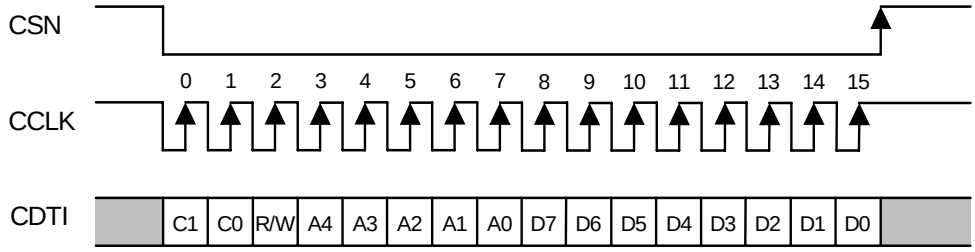
(1) After VDD is powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) The digital data can be stopped. Click noise after MCLK or LRCK is input again can be reduced by inputting "0" data during this period.
(4) Click noise occurs within 3 ~ 4LRCK cycles from rising edge (↑) of PDN signal or MCLK inputs. This noise is output even if "0" data is input.
(5) MCLK, BICK and LRCK clocks can be stopped in reset mode (MCLK or LRCK stopped).
(6) Mute the analog output externally if click noise (4) influences system applications. The timing example is shown in this figure.

Figure 8. Reset Timing Example 2

■ Mode Control Interface

Functions of the AK4482 can be controlled by registers. Internal registers may be written to through3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2-bits, C1/0, fixed to "01"), Read/Write (1-bit; fixed to "1"), Register address (MSB first, 5-bits) and Control data (MSB first, 8-bits). The AK4482 latches the data on the rising edge of CCLK, so data should be clocked in on the falling edge. Writing data is valid when CSN "↑". The clock speed of CCLK is 5MHz (max). The CSN pin should be "H" when not accessing to the registers.

Setting the PDN pin to "L" resets the registers to their default values. In serial control mode, the internal timing circuit is reset by the RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 9. Control I/F Timing

* The AK4482 does not support the read command. C1-0 and R/W are fixed to "011".
* When the AK4482 is in power down mode (PDN pin = "L") or the MCLK is not provided, a writing into the control registers is prohibited.

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	0	0	0	0	0	DZFB	0	SD
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Notes:

For addresses from 05H to 1FH, data must not be written.
When the PDN pin goes "L", the registers are initialized to their default values.
When RSTN bit goes "0", the only internal timing is reset and the registers are not initialized to their default values.
All data can be written to the register even if PW or RSTN bit is "0".

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
default		1	0	0	0	1	0	1	1

RSTN: Internal timing reset control
0: Reset. All registers are not initialized.
1: Normal Operation
When MCLK frequency or DFS changes, the AK4382A should be reset by PDN pin or RSTN bit.

PW: Power down control
0: Power down. All registers are not initialized.
1: Normal Operation

DIF2-0: Audio data interface formats (Table 7)
Initial: "010", Mode 2

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the setting of DFS1-0 are ignored. When this bit is "0", DFS1-0 set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
default		0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal operation
1: DAC outputs soft-muted

DEM1-0: De-emphasis Response (Table 8)
Initial: "01", OFF

DFS1-0: Sampling speed control
00: Normal Speed Mode
01: Double Speed Mode
10: Quad Speed Mode
When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

SLOW: Slow Roll-off Filter Enable
0: Sharp Roll-off Filter
1: Slow Roll-off Filter

DZFM: Data Zero Detect Mode
0: Channel Separated Mode
1: Channel ANDed Mode
If the DZFM bit is set to "1", the DZF pins of both channels go to "H" only when the input data at both channels are continuously zeros for 8192 LRCK cycles.

DZFE: Data Zero Detect Enable

0: Disable

1: Enable

Zero detect function can be disabled by DZFE bit "0". In this case, the DZF pins of both channels are always "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	0	0	0	0	0	DZFB	0	SD
default		0	0	0	0	0	0	0	0

SD: Digital filter Setting

0: Sharp roll off filter or Slow roll off filter

1: Short delay Sharp roll off filter or Short delay Slow roll off filter

SD bit	SLOW bit	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay Sharp roll-off filter	(default)
1	1	Short delay Slow roll-off filter	

Table 10 Digital Filter setting

DZFB: Inverting Enable of DZF

0: DZF goes "H" at Zero Detection

1: DZF goes "L" at Zero Detection

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
default		1	1	1	1	1	1	1	1

$ATT = 20 \log_{10} (ATT\_DATA / 255)$ [dB]

00H: Mute

SYSTEM DESIGN

Figure 10 shows the system connection diagram. An evaluation board (AKD4482) demonstrates the optimum layout, power supply arrangements and measurement results.

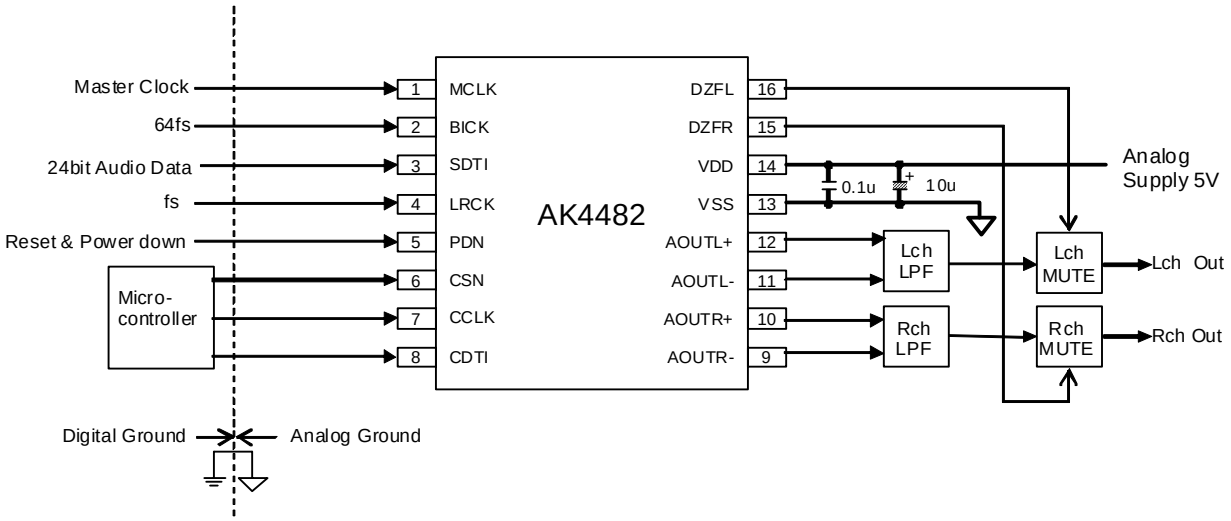


Figure 10. Typical Connection Diagram

Notes:
- LRCK = fs, BICK=64fs.
- When AOUT drives a capacitive load, some resistance should be added in series between AOUT and the capacitive load.
- All input pins except pull-down pins should not be allowed to float.

1. Grounding and Power Supply Decoupling

VDD and VSS are supplied from the analog supply and should be separated from the system digital supply. Decoupling capacitors, especially 0.1µF ceramic capacitors for high frequency bypass, should be placed as near to VDD as possible. The differential voltage between VDD and VSS pins set the analog output range.

2. Analog Output

The analog outputs are fully differential outputs at 2.4Vpp x VDD/5V, centered around 2.3V (typ). The differential outputs are summed externally, V_{AOUT} = (AOUT+)-(AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 4.8Vpp (typ.@VDD = 5V). The bias voltage of the external summing circuit is supplied externally. The input data format is two's complement. The output voltage (V_{AOUT}) is positive full scale for 7FFFFFH (@24-bits) and negative full scale for 800000H (@24-bits). The ideal V_{AOUT} is 0V for 000000H(@24-bits).

The internal switched capacitor filters (SCF) attenuate the noise generated by the delta sigma modulator beyond the audio passband. AOUT+/- DC off-set can be reduced without AC coupling capacitors since the AK4482 output is differential. Figure 11 and Figure 12 show examples of an external LPF circuit summing the differential outputs with an op-amp.

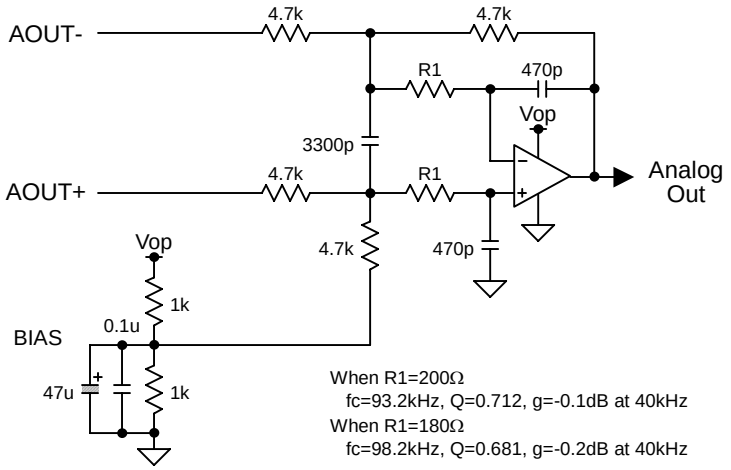


Figure 11. External 2nd order LPF Circuit Example (using op-amp with single power supply)

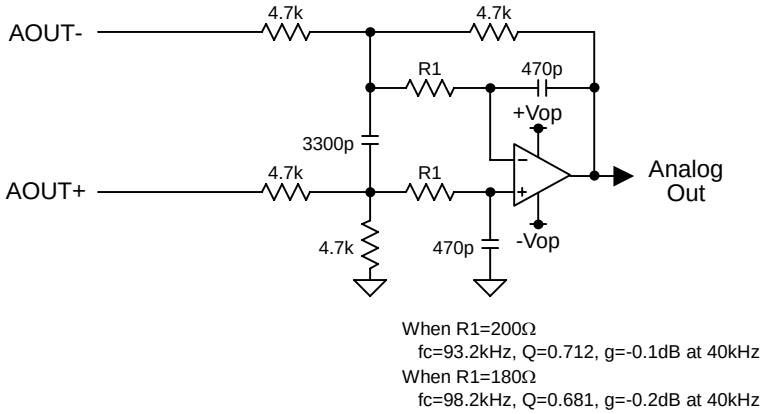
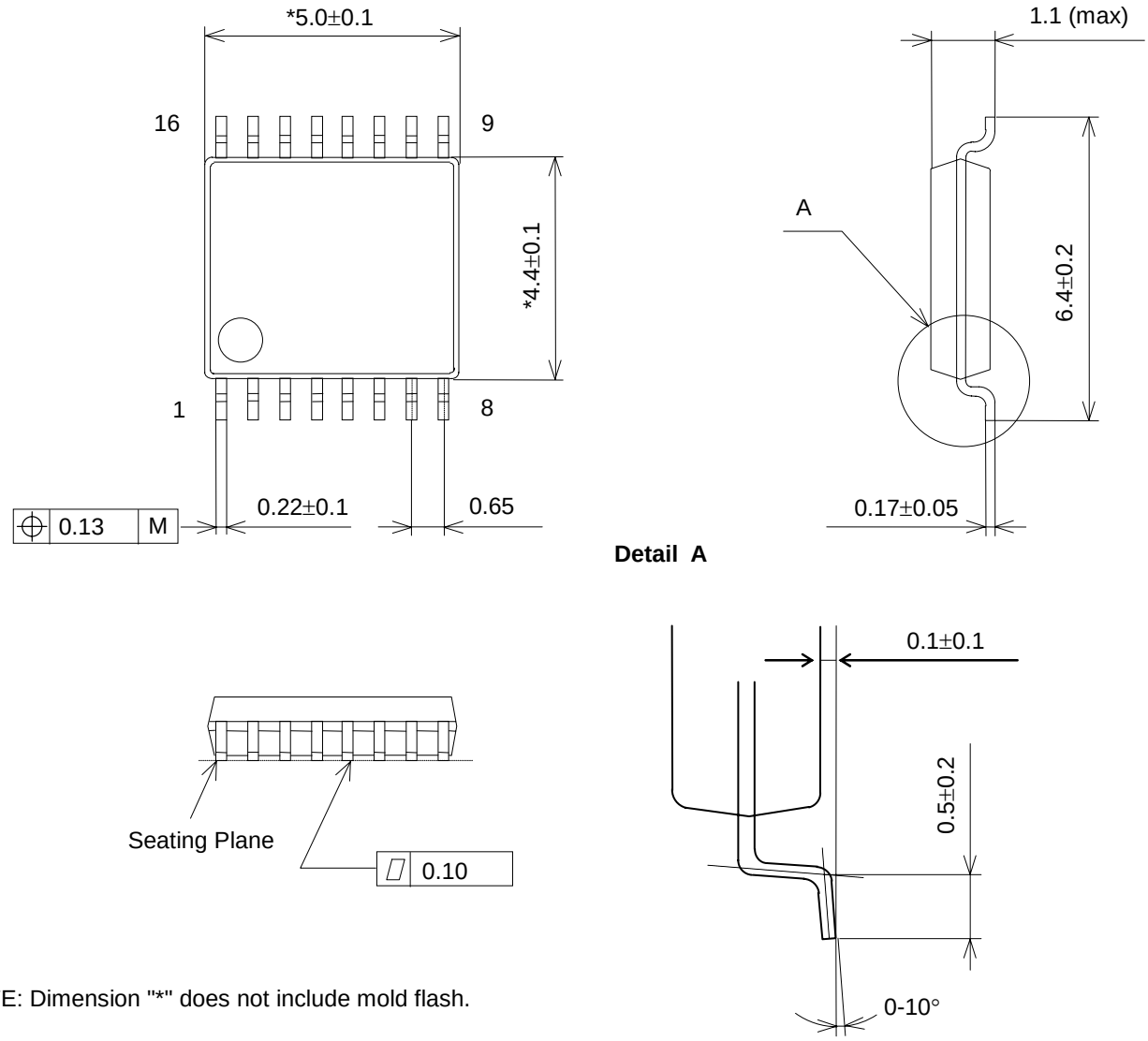


Figure 12. External 2nd order LPF Circuit Example (using op-amp with dual power supplies)

PACKAGE

16pin TSSOP (Unit: mm)

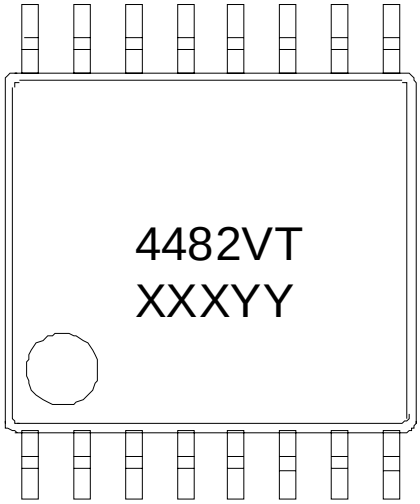


NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

Package molding compound:	Epoxy, Halogen (Bromine and Chlorine) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code : XXXYY (5 digits)
   XXX: Date Code
   YY: Lot#
3) Marketing Code : 4482VT

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
12/04/26	00	First Edition		
12/05/08	01	Error Correction	6	SHARP ROLL OFF FILTER Measurement conditions: DEM=OFF → SD= "0" SLOW ROLL OFF FILTER Measurement conditions: AVDD=DVDD → VDD DEM=OFF → SD= "0"
			7	SHORT DELAY SHARP ROLL OFF FILTER Measurement conditions: DEM=OFF → SD= "1" SHORT DELAY SLOW ROLL OFF FILTER Measurement conditions: AVDD=DVDD → VDD DEM=OFF → SD= "1"
			19	■ Register Map 02H, D0: MD → SD
			21	■ Register Definitions 02H, D0: MD → SD

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