TABLE OF CONTENTS

REVISION HISTORY

3/13—Revision D: Initial Version

FUNCTIONAL BLOCK DIAGRAM

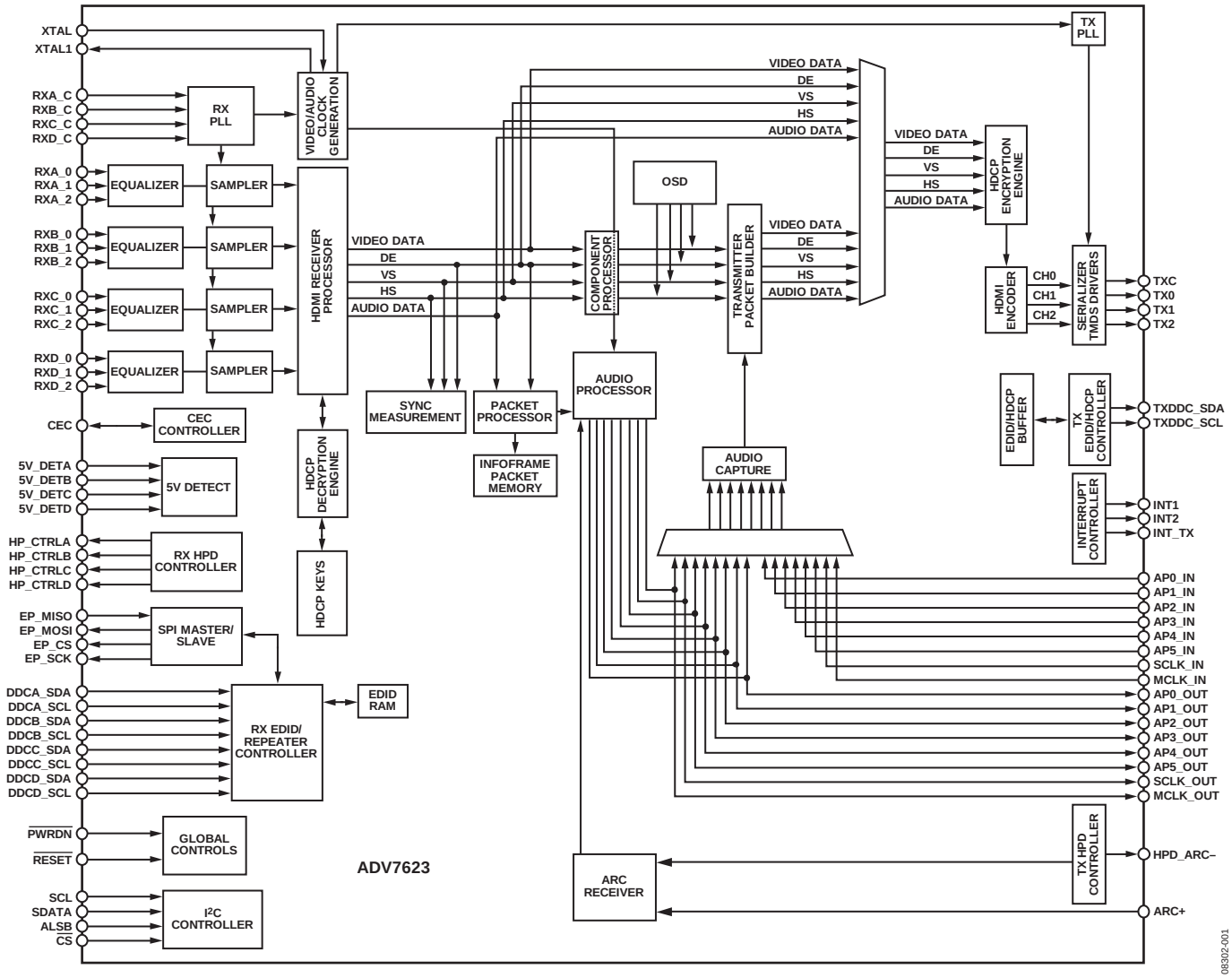


Figure 1.

SPECIFICATIONS

CVDD = 1.8 V ± 5%, DVDD = 1.8 V ± 5%, DVDDIO = 3.3 V ± 5%, PVDD = 1.8 V ± 5%, TVDD = 3.3 V ± 5%, TXAVDD = 1.8 V ± 5%, TXPVDD = 1.8 V ± 5%, TXPLVDD = 1.8 V ± 5%, T_{MIN} to T_{MAX} = 0°C to 70°C.

DIGITAL, HDMI, AND AC SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS					
Input High Voltage (V_{IH})		2			V
Input Low Voltage (V_{IL})				0.8	V
Input Current (I_{IN})	$\overline{\text{RESET}}$, EP_MISO, ALSB and $\overline{\text{CS}}$ pins	−60		+60	µA
	Other digital inputs	−10		+10	µA
Input Capacitance (C_{IN})				10	pF
DIGITAL INPUTS (5 V TOLERANT) [1]					
Input High Voltage (V_{IH})		2.6			V
Input Low Voltage (V_{IL})				0.8	V
Input Current (I_{IN})		−82		+82	µA
DIGITAL OUTPUTS					
Output High Voltage (V_{OH})		2.4			V
Output Low Voltage (V_{OL})				0.4	V
High Impedance Leakage Current (I_{LEAK})			10		µA
Output Capacitance (C_{OUT})				20	pF
HDMI					
TMDS Differential Pin Capacitance			0.3		pF
AC SPECIFICATIONS					
Input Specifications					
Intrapair (+ to −) Differential Input Skew for TMDS Clock Rates up to 222.75 MHz		0.4 t_{BIT}			ps
Intrapair (+ to −) Differential Input Skew for TMDS Clock Rates Above 222.75 MHz		0.15 t_{BIT} + 112			ps
Channel-to-Channel Differential Input Skew				0.2 t_{PIXEL} + 1.78	ns
TMDS Input Clock Range		25		225	MHz
TMDS Input Clock Jitter Tolerance			0.5	0.25	t_{BIT}
Output Specifications					
TMDS Output Clock Frequency		20		225	MHz
TMDS Output Clock Duty Cycle		48		52	%
TMDS Output Differential Swing		900	1100	1200	mV
Differential Output Timing					
Low-to-High Transition Time		75	175		ps
High-to-Low Transition Time		75	175		ps

[1] The following pins are 5 V tolerant: DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, DDCC_SCL, DDCC_SDA, DDCD_SCL, DDCD_SDA, TXDDC_SDA, TXDDC_SCL, HP_CTRLA, HP_CTRLB, HP_CTRLC, HP_CTRLD, HPD_ARC−, 5V_DETA, 5V_DETB, 5V_DETC, 5V_DETD, $\overline{\text{PWRDN}}$, CEC, ARC+.

DATA AND I²C TIMING CHARACTERISTICS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VIDEO SYSTEM CLOCK AND XTAL						
Crystal Nominal Frequency				28.63636		MHz
Crystal Frequency Stability					±50	ppm
External Clock Source[1]		External crystal must operate at 1.8 V				
Input High Voltage	V_{IH}	XTAL driven with external clock source	1.2			V
Input Low Voltage	V_{IL}	XTAL driven with external clock source			0.4	V
RESET FEATURE						
Reset Pulse Width			5			ms
I²C PORTS (FAST MODE)						
xCL Frequency[2]					400	kHz
xCL Minimum Pulse Width High[2]	t_1		600			ns
xCL Minimum Pulse Width Low[2]	t_2		1.3			µs
Hold Time (Start Condition)	t_3		600			ns
Setup Time (Start Condition)	t_4		600			ns
xDA Setup Time[2]	t_5		100			ns
xCL and xDA Rise Time[2]	t_6				300	ns
xCL and xDA Fall Time[2]	t_7				300	ns
Setup Time (Stop Condition)	t_8		0.6			µs
I²C PORTS (NORMAL MODE)						
xCL Frequency[2]					100	kHz
xCL Minimum Pulse Width High[2]	t_1		4.0			µs
xCL Minimum Pulse Width Low[2]	t_2		4.7			µs
Hold Time (Start Condition)	t_3		4.0			µs
Setup Time (Start Condition)	t_4		4.7			µs
xDA Setup Time[2]	t_5		250			ns
xCL and xDA Rise Time[2]	t_6				1000	ns
xCL and xDA Fall Time[2]	t_7				300	ns
Setup Time (Stop Condition)	t_8		4.0			µs
AUDIO OUTPUT PORT (MASTER MODE)						
SCLK Mark Space Ratio	t_{13}:t_{14}		45:55		55:45	% duty cycle
APx_OUT Data Transition Time (LRCLK)[3]	t_{15}	End of valid data to negative SCLK edge			10	ns
APx_OUT Data Transition Time (LRCLK)[3]	t_{16}	Negative SCLK edge to start of valid data			10	ns
APx_OUT Data Transition Time (I²S Data)[3]	t_{17}	End of valid data to negative SCLK edge			5	ns
APx_OUT Data Transition Time (I²S Data)[3]	t_{18}	Negative SCLK edge to start of valid data			5	ns
AUDIO INPUT PORT						
APx_IN Setup Time (I²S Data)[3]	t_{19}		2			ns
APx_IN Hold Time (I²S Data)[3]	t_{20}		2			ns
APx_IN Setup Time (LRCLK)[3]	t_{19}		2			ns
APx_IN Hold Time (LRCLK)[3]	t_{20}		2			ns

[1] This part must be configured for external oscillator operation. A 1.8 V oscillator must be used.
[2] The prefix x refers to S, DDCA_S, DDCB_S, DDCC_S, and DDCD_S.
[3] The suffix x refers to 0, 1, 2, 3, 4, and 5.

Timing Diagrams

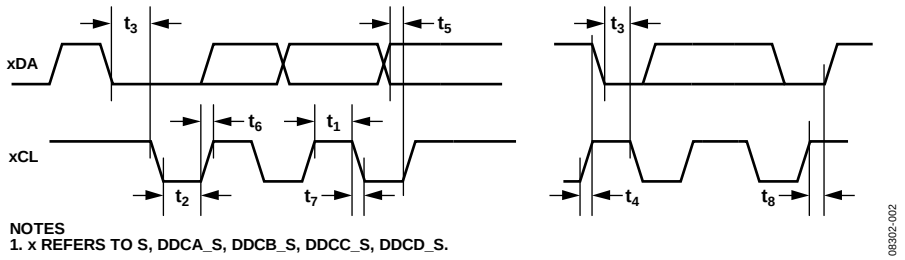


Figure 2. I²C Timing

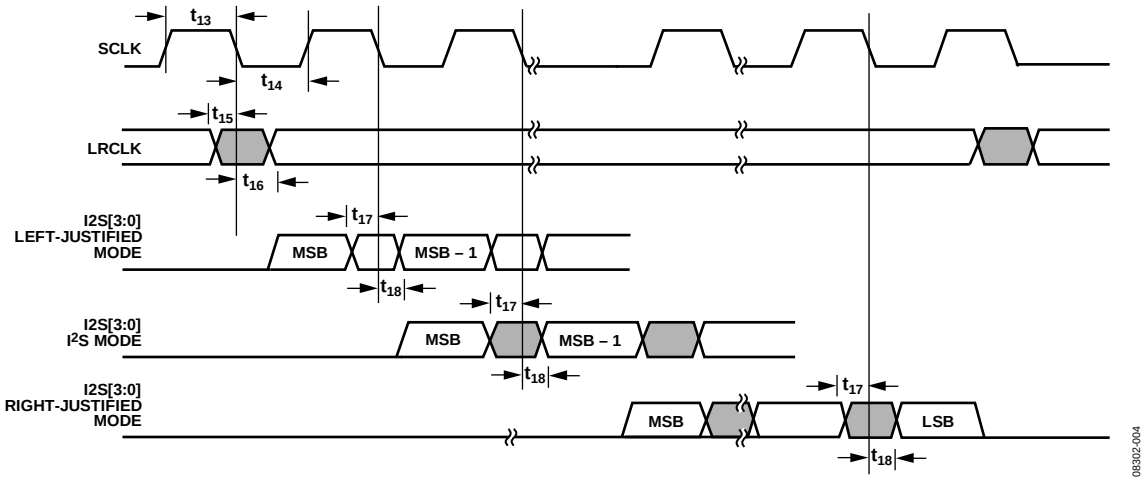


Figure 3. I²S Output Timing

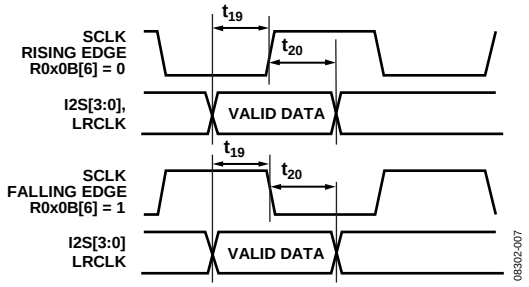


Figure 4. I²S Input Timing

POWER SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLIES					
Comparator Power Supply (CVDD)	1.71	1.8	1.89	V	
Digital Core Power Supply (DVDD)	1.71	1.8	1.89	V	
Digital I/O Power Supply (DVDDIO)	3.14	3.3	3.46	V	
PLL Power Supply (PVDD)	1.71	1.8	1.89	V	
Termination Power Supply (TVDD)	3.14	3.3	3.46	V	
TX TMDS Output Power Supply (TXAVDD)	1.71	1.8	1.89	V	
TX Power Supply (TXPVDD)	1.71	1.8	1.89	V	
TX PLL Power Supply (TXPLVDD)	1.71	1.8	1.89	V	
CURRENT CONSUMPTION[1, 2, 3, 4]					
Comparator Power Supply (I_{CVDD})		481	545	mA	Four ports with 1080p 12-bit, Xpressview and OSD enabled
			1.0	mA	Power-Down Mode 1
			1.0	mA	Power-Down Mode 0
Digital Core Power Supply (I_{DVDD})		301	350	mA	Four ports with 1080p 12-bit, Xpressview and OSD enabled
			9.0	mA	Power-Down Mode 1
			6.7	mA	Power-Down Mode 0
Digital I/O Power Supply (I_{DVDDIO})		1.0	2.0	mA	Four ports with 1080p 12-bit, Xpressview and OSD enabled
			3.4	mA	Power-Down Mode 1
			3.3	mA	Power-Down Mode 0
PLL Power Supply (I_{PVDD})		34.0	39.6	mA	Four ports with 1080p 12-bit, Xpressview and OSD enabled
			1.7	mA	Power-Down Mode 1
			1.6	mA	Power-Down Mode 0
Termination Power Supply (I_{TVDD})		283	312	mA	Four ports with 1080p 12-bit, Xpressview and OSD enabled
			0.4	mA	Power-Down Mode 1
			0.4	mA	Power-Down Mode 0
TX TMDS Output Power Supply (I_{TXAVDD})		13.0	14.3	mA	Four ports with 1080p 12-bit, Xpressview and OSD enabled
			0.5	mA	Power-Down Mode 1
			0.3	mA	Power-Down Mode 0
TX Power Supply (I_{TXPVDD})		5.0	6.6	mA	Four ports with 1080p 12-bit, Xpressview and OSD enabled
			2.8	mA	Power-Down Mode 1
			2.8	mA	Power-Down Mode 0
TX PLL Power Supply ($I_{TXPLVDD}$)		23.0	26.4	mA	Four ports with 1080p 12-bit, Xpressview and OSD enabled
			1.6	mA	Power-Down Mode 1
			1.6	mA	Power-Down Mode 0

[1] All maximum current values are guaranteed by characterization to assist in power supply design.
[2] Typical current consumption values are recorded with nominal voltage supply levels and at room temperature.
[3] Maximum current consumption values are recorded with maximum rated voltage supply levels and at room temperature.
[4] Termination power supply includes TVDD current consumed off chip.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
CVDD to GND	2.2 V
DVDD to GND	2.2 V
PVDD to GND	2.2 V
DVDDIO to GND	4.0 V
TVDD to GND	4.0 V
TXAVDD to GND	2.2 V
TXPVDD to GND	2.2 V
TXPLVDD to GND	2.2 V
Digital Inputs Voltage to GND	GND − 0.3 V to DVDDIO + 0.3 V up to a maximum of 4.0 V
5 V Tolerant Digital Inputs to GND[1]	5.5 V
Digital Output Voltage to GND	GND − 0.3 V to DVDDIO + 0.3 V up to a maximum of 4.0 V
XTAL, XTAL1 Pins	−0.3 V to PVDD to +0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature	150°C
Infrared Reflow, Soldering (20 sec)	260°C

[1] The following inputs are 3.3 V inputs but are 5 V tolerant: DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, DDCC_SCL, DDCC_SDA, DDCD_SCL, DDCD_SDA, TXDDC_SDA, TXDDC_SCL, HP_CTRLA, HP_CTRLB, HP_CTRLC, HP_CTRLD, HPD_ARC−, 5V_DETA, 5V_DETB, 5V_DETC, 5V_DETD, PWRDN, CEC, ARC+.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7623, turn off the unused sections of the part.

Due to printed circuit board (PCB) metal variation and, thus, variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this eliminates the variance associated with the θ_{JA} value.

The maximum junction temperature ($T_{J\ MAX}$) of 125°C must not be exceeded. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on the DUT:

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:
T_S = the package surface temperature (°C).
Ψ_{JT} = 0.6°C/W for a 144-lead LQFP.

$$W_{TOTAL} = ((CVDD \times I_{CVDD}) + (DVDD \times I_{DVDD}) + (PVDD \times I_{PVDD}) + (DVDDIO \times I_{DVDDIO}) + (0.7 \times TVDD \times I_{TVDD}) + (TXAVDD \times I_{TXAVDD}) + (TXPVDD \times I_{TXPVDD}) + (TXPLVDD \times I_{TXPLVDD}))$$

Note that for W_{TOTAL}, 5% of TVDD power is dissipated on the part itself.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

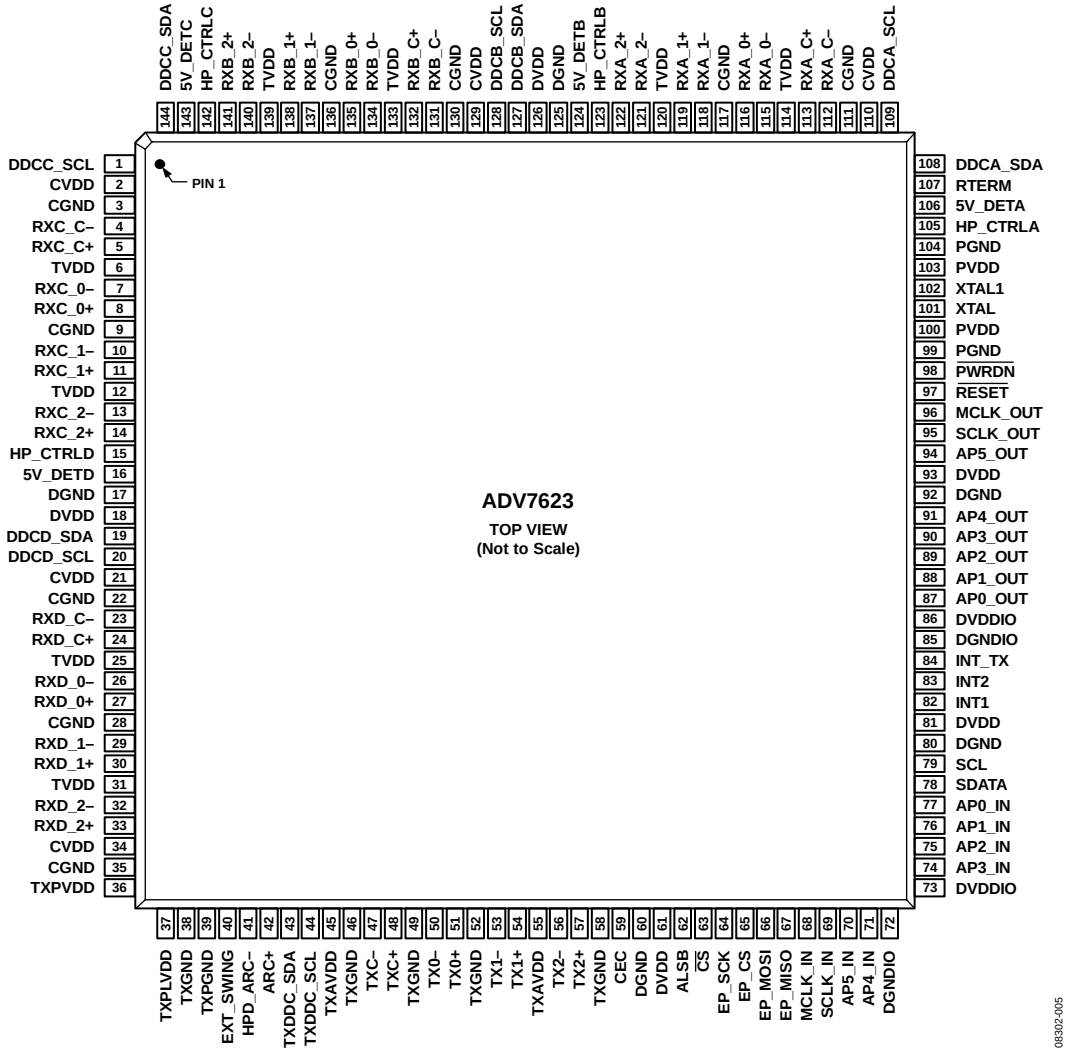


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DDCC_SCL	Digital input	HDCP Slave Serial Clock Port C. DDCC_SCL is a 3.3 V input that is 5 V tolerant.
2	CVDD	Power	Receiver Comparator Supply Voltage (1.8 V).
3	CGND	Ground	TVDD and CVDD Ground.
4	RXC_C–	HDMI input	Digital Input Clock Complement of Port C in the HDMI Interface.
5	RXC_C+	HDMI input	Digital Input Clock True of Port C in the HDMI Interface.
6	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
7	RXC_0–	HDMI input	Digital Input Channel 0 Complement of Port C in the HDMI Interface.
8	RXC_0+	HDMI input	Digital Input Channel 0 True of Port C in the HDMI Interface.
9	CGND	Ground	TVDD and CVDD Ground.
10	RXC_1–	HDMI input	Digital Input Channel 1 Complement of Port C in the HDMI Interface.
11	RXC_1+	HDMI input	Digital Input Channel 1 True of Port C in the HDMI Interface.
12	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).

Pin No.	Mnemonic	Type	Description
13	RXC_2−	HDMI input	Digital Input Channel 2 Complement of Port C in the HDMI Interface.
14	RXC_2+	HDMI input	Digital Input Channel 2 True of Port C in the HDMI Interface.
15	HP_CTRLD	Digital output	Hot Plug Detect for Port D.
16	5V_DETD	Digital input	5 V Detect Pin for Port D in the HDMI Interface.
17	DGND	Ground	DVDD Ground.
18	DVDD	Power	Digital Supply Voltage (1.8 V).
19	DDCD_SDA	Digital I/O	HDCP Slave Serial Data Port D. DDCD_SDA is a 3.3 V input/output that is 5 V tolerant.
20	DDCD_SCL	Digital input	HDCP Slave Serial Clock Port D. DDCD_SCL is a 3.3 V input that is 5 V tolerant.
21	CVDD	Power	Receiver Comparator Supply Voltage (1.8 V).
22	CGND	Ground	TVDD and CVDD Ground.
23	RXD_C−	HDMI input	Digital Input Clock Complement of Port D in the HDMI Interface.
24	RXD_C+	HDMI input	Digital Input Clock True of Port D in the HDMI Interface.
25	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
26	RXD_0−	HDMI input	Digital Input Channel 0 Complement of Port D in the HDMI Interface.
27	RXD_0+	HDMI input	Digital Input Channel 0 True of Port D in the HDMI Interface.
28	CGND	Ground	TVDD and CVDD Ground.
29	RXD_1−	HDMI input	Digital Input Channel 1 Complement of Port D in the HDMI Interface.
30	RXD_1+	HDMI input	Digital Input Channel 1 True of Port D in the HDMI Interface.
31	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
32	RXD_2−	HDMI input	Digital Input Channel 2 Complement of Port D in the HDMI Interface.
33	RXD_2+	HDMI input	Digital Input Channel 2 True of Port D in the HDMI Interface.
34	CVDD	Power	Receiver Comparator Supply Voltage (1.8 V).
35	CGND	Ground	TVDD and CVDD Ground.
36	TXPVDD	Power	1.8 V Power Supply for Digital and I/O Power Supply. This pin supplies power to the digital logic and I/Os. It should be filtered and as quiet as possible.
37	TXPLVDD	Power	1.8 V Power Supply.
38	TXGND	Ground	TXPVDD Ground.
39	TXPGND	Ground	TXPLVDD Ground.
40	EXT_SWING	Analog input	This pin sets the internal reference currents. Place an 887 Ω resistor (1% tolerance) between this pin and ground.
41	HPD_ARC−	Analog input	Hot Plug Detect Signal and Audio Return Channel Inverted Input. This pin indicates to the interface whether the receiver is connected.
42	ARC+	Analog input	Audio Return Channel (ARC) Input (5 V Tolerant).
43	TXDDC_SDA	Digital I/O	Serial Port Data I/O to Receiver. This pin serves as the master to the DDC bus. It supports a 5 V CMOS logic level.
44	TXDDC_SCL	Digital output	Serial Port Data Clock to Receiver. This pin serves as the master clock for the DDC bus. It supports a 5 V CMOS logic level.
45	TXAVDD	Power	1.8 V Power Supply for TMDS Outputs.
46	TXGND	Ground	TXAVDD Ground.
47	TXC−	HDMI output	Differential Clock Output. Differential clock output at the TMDS clock rate; supports TMDS logic level.
48	TXC+	HDMI output	Differential Clock Output. Differential clock output at the TMDS clock rate; supports TMDS logic level.
49	TXGND	Ground	TXAVDD Ground.
50	TX0−	HDMI output	Differential Output Channel 0 Complement. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
51	TX0+	HDMI output	Differential Output Channel 0 True. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
52	TXGND	Ground	TXAVDD Ground.
53	TX1−	HDMI output	Differential Output Channel 1 Complement. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
54	TX1+	HDMI output	Differential Output Channel 1 True. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
55	TXAVDD	Power	1.8 V Power Supply for TMDS Outputs.

Pin No.	Mnemonic	Type	Description
56	TX2−	HDMI output	Differential Output Channel 2 Complement. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
57	TX2+	HDMI output	Differential Output Channel 2 True. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
58	TXGND	Ground	TXAVDD Ground.
59	CEC	Digital I/O	Consumer Electronics Control Channel (5 V Tolerant).
60	DGND	Ground	DVDD Ground.
61	DVDD	Power	Digital Supply Voltage (1.8 V).
62	ALSB	Digital input	This pin is used to set the I^2C address of the Rx IO and the Tx main map.
63	$\overline{CS}$	Digital input	Chip Select Pin. This pin must be set low or left floating for the chip to process I^2C messages that are destined for the ADV7623. The ADV7623 ignores I^2C messages that it receives if this pin is high.
64	EP_SCK	Digital output	SPI Clock Interface for the EDID/OSD.
65	EP_CS	Digital output	SPI Chip Selected Interface for the EDID/OSD.
66	EP_MOSI	Digital output	SPI Master Out/Slave In for the EDID/OSD.
67	EP_MISO	Digital input	SPI Master In/Slave Out for the EDID/OSD.
68	MCLK_IN	Digital input	Audio Reference Clock. $128 \times N \times f_S$ with N = 1, 2, 3, or 4. Set to 128 × sampling frequency (f_S), $256 \times f_S$, $384 \times f_S$, or $512 \times f_S$. It supports CMOS logic levels from 1.8 V to 3.3 V.
69	SCLK_IN	Digital input	I^2S Audio Clock. It supports CMOS logic levels from 1.8 V to 3.3 V.
70	AP5_IN	Digital input	Audio Input Port 5. It supports CMOS logic levels from 1.8 V to 3.3 V.
71	AP4_IN	Digital input	Audio Input Port 4. It supports CMOS logic levels from 1.8 V to 3.3 V.
72	DGNDIO	Ground	DVDDIO Ground.
73	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
74	AP3_IN	Digital input	Audio Input Port 3. It supports CMOS logic levels from 1.8 V to 3.3 V.
75	AP2_IN	Digital input	Audio Input Port 2. It supports CMOS logic levels from 1.8 V to 3.3 V.
76	AP1_IN	Digital input	Audio Input Port 1. It supports CMOS logic levels from 1.8 V to 3.3 V.
77	AP0_IN	Digital input	Audio Input Port 0. It supports CMOS logic levels from 1.8 V to 3.3 V.
78	SDATA	Digital I/O	I^2C Port Serial Data Input/Output Pin. SDATA is the data line for the control port.
79	SCL	Digital input	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
80	DGND	Ground	DVDD Ground.
81	DVDD	Power	Digital Supply Voltage (1.8 V).
82	INT1 (AMUTE1)	Digital output	Interrupt Pin. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control. This pin can also output an audio mute signal.
83	INT2 (AMUTE2)	Digital output	Interrupt Pin. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control. This pin can also output an audio mute signal.
84	INT_TX	Digital output	Interrupt; Open Drain. A 2 kΩ pull-up resistor to the microcontroller I/O supply is recommended.
85	DGNDIO	Ground	DVDDIO Ground.
86	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
87	AP0_OUT	Digital output	Audio Output Port 0.
88	AP1_OUT	Digital output	Audio Output Port 1.
89	AP2_OUT	Digital output	Audio Output Port 2.
90	AP3_OUT	Digital output	Audio Output Port 3.
91	AP4_OUT	Digital output	Audio Output Port 4.
92	DGND	Ground	DVDD Ground.
93	DVDD	Power	Digital Supply Voltage (1.8 V).
94	AP5_OUT	Digital output	Audio Output Port 5.
95	SCLK_OUT	Digital output	Audio Serial Clock Output.
96	MCLK_OUT	Digital output	Audio Master Clock Output.
97	$\overline{RESET}$	Digital input	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7623 circuitry.
98	$\overline{PWRDN}$	Digital input	Active Low Power-Down Pin. If used, this pin should be pulled high to power up the ADV7623. This pin can also be used as an in system power detect where internal EDID can be powered from a 5 V signal of the HDMI port when it is connected to active equipment.

Pin No.	Mnemonic	Type	Description
99	PGND	Ground	PVDD Ground.
100	PVDD	Power	PLL Supply Voltage (1.8 V).
101	XTAL	Miscellaneous analog	Input pin for 28.63636 MHz crystal or an external 1.8 V 28.63636 MHz clock oscillator source to clock the ADV7623.
102	XTAL1	Miscellaneous analog	Crystal Output Pin. This pin should be left floating if a clock oscillator is used.
103	PVDD	Power	PLL Supply Voltage (1.8 V).
104	PGND	Ground	PVDD Ground.
105	HP_CTRLA	Digital output	Hot Plug Detect for Port A.
106	5V_DETA	Digital input	5 V Detect Pin for Port A in the HDMI Interface.
107	RTERM	Miscellaneous analog	This pin sets the internal termination resistance. A 500 Ω resistor between this pin and ground should be used.
108	DDCA_SDA	Digital I/O	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input/output that is 5 V tolerant.
109	DDCA_SCL	Digital input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
110	CVDD	Power	Receiver Comparator Supply Voltage (1.8 V).
111	CGND	Ground	TVDD and CVDD Ground.
112	RXA_C–	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
113	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
114	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
115	RXA_0–	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
116	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
117	CGND	Ground	TVDD and CVDD Ground.
118	RXA_1–	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
119	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.
120	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
121	RXA_2–	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
122	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
123	HP_CTRLB	Digital output	Hot Plug Detect for Port B.
124	5V_DETB	Digital input	5 V Detect Pin for Port B in the HDMI Interface.
125	DGND	Ground	DVDD Ground.
126	DVDD	Power	Digital Supply Voltage (1.8 V).
127	DDCB_SDA	Digital I/O	HDCP Slave Serial Data Port B. DDCB_SDA is a 3.3 V input/output that is 5 V tolerant.
128	DDCB_SCL	Digital input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
129	CVDD	Power	Receiver Comparator Supply Voltage (1.8 V).
130	CGND	Ground	TVDD and CVDD Ground.
131	RXB_C–	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.
132	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
133	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
134	RXB_0–	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
135	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
136	CGND	Ground	TVDD and CVDD Ground.
137	RXB_1–	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
138	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
139	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
140	RXB_2–	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
141	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
142	HP_CTRLC	Digital output	Hot Plug Detect for Port C.
143	5V_DETC	Digital input	5 V Detect Pin for Port C in the HDMI Interface.
144	DDCC_SDA	Digital I/O	HDCP Slave Serial Data Port C. DDCC_SDA is a 3.3 V input/output that is 5 V tolerant.

FUNCTIONAL OVERVIEW

HDMI RECEIVER

The ADV7623 front end incorporates a 4:1 multiplexed HDMI receiver boasting Xpressview fast switching technology and support for HDMI features including 3D TV, content type bits, and advanced features, such as capability discovery and control. Building on the feature set of existing Analog Devices HDMI devices, the ADV7623 also offers support for all HDTV formats up to 36-bit, 1080p Deep Color and all display resolutions up to UXGA (1600 × 1200 at 60 Hz).

Xpressview fast switching technology, using Analog Devices hardware-based HDCP engine that minimizes software overhead, allows switching between any two input ports in less than 1 second.

A key feature of the ADV7623 is the on-chip character-based OSD generator. The OSD generated can be converted to match the input format 4:2:2 or 4:4:4 in RGB or YCrCb color space. The OSD is overlaid at the output resolution for best performance. The OSD portion of the image is optionally semitransparent using a 5-bit alpha blend between the input video and the OSD. The OSD font characters are stored in either an external SPI flash or read directly into the RAM when instructed or can be loaded in to the on-chip RAM via the SPI or I^2C.

With the inclusion of HDCP 1.4, displays can receive encrypted video content. The HDMI interface of the ADV7623 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP 1.4 protocol. Repeater support is also offered by the ADV7623.

The HDMI receiver offers advanced audio functionality. It supports multichannel I^2S audio for up to eight channels. It also supports a 6-DSD channel interface with each channel carrying an over-sampled 1-bit representation of the audio signal as delivered on SACD. The ADV7623 can also receive HBR audio packet streams and output them through the HBR interface in an S/PDIF format conforming to the IEC 60958 standard. S/PDIF is supported via the HPD back channel. The receiver also contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. On detection of these conditions, the audio data can be ramped to prevent audio clicks or pops.

The ADV7623HDMI receiver incorporates active, programmable equalization of the HDMI data signals that compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. The receiver also contains a programmable data island packet interrupt generator.

HDMI TRANSMITTER

The ADV7623 features a single HDMI transmitter supporting ARC, 3D TV formats as well as all HDTV formats up to 1080p, 36-bit Deep Color.

Supporting both single-ended and differential modes, the ARC feature simplifies cabling by combining an upstream audio capability in a conventional HDMI cable.

The transmitter features an on-chip MPU with an I^2C master to perform HDCP operations and EDID reading operations.

I^2C INTERFACE

The ADV7623 supports a 2-wire serial (I^2C-compatible) micro-processor bus driving multiple peripherals. The ADV7623 is controlled by an external I^2C master device, such as a micro-controller.

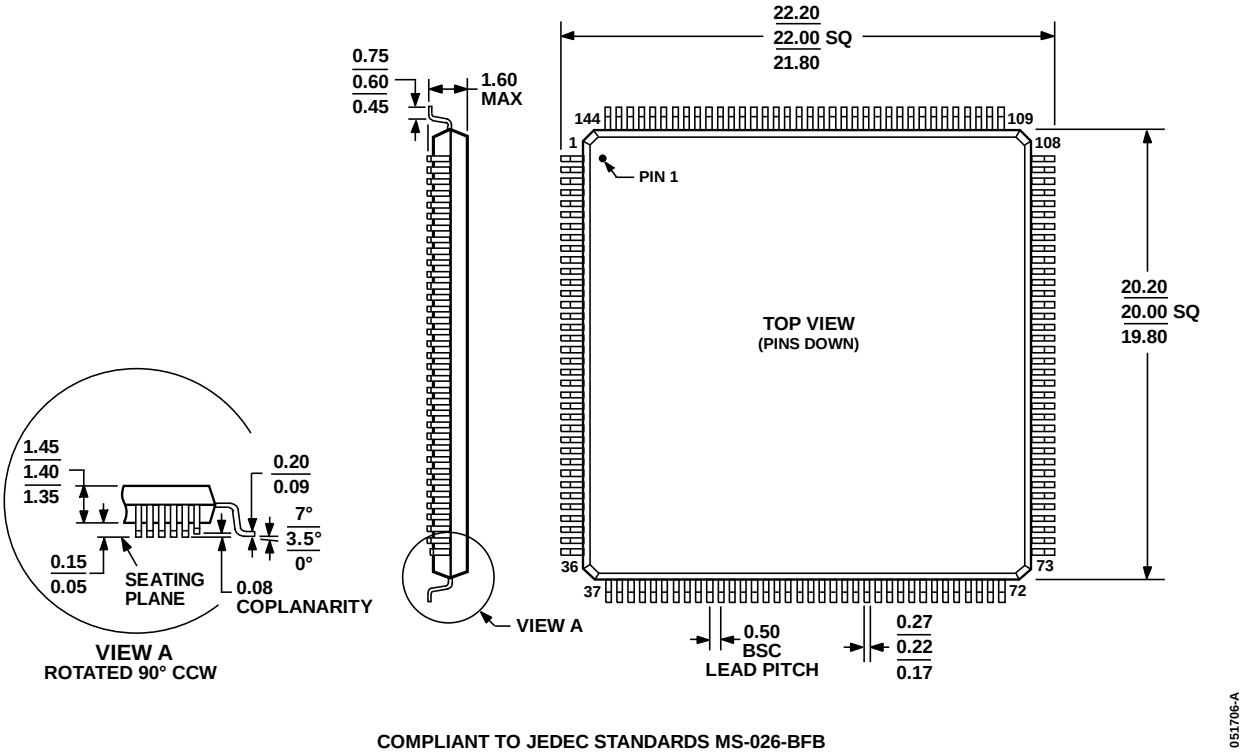
OTHER FEATURES

Other features include the following:

- Fully qualified software low level libraries, driver, and application
- Complete input and output audio support
- Programmable interrupt request output pins: INT1, INT2, and INT_TX
- Chip select
- Non-HDCP professional variant available (ADV7623BSTZ-P). No evaluation board is available for this variant.
- Low power consumption: 1.8 V digital core, 1.8 V analog, and 3.3 V digital input/output, low power power-down mode, and green PC mode
- Temperature range: 0°C to 70°C
- 20 mm × 20 mm, Pb-free, 144-lead LQFP

For more detailed product information about the ADV7623, contact your local Analog Devices sales office.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BFB

Figure 6. 144-Lead Low Profile Quad Flat Package [LQFP]
(ST-144)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Model Description	Temperature Range	Package Description	Package Option
ADV7623BSTZ	HDCP Transceiver	0°C to 70°C	144-Lead Low Profile Quad Flat Package [LQFP]	ST-144
ADV7623BSTZ-RL	HDCP Transceiver (Reel)	0°C to 70°C	144-Lead Low Profile Quad Flat Package [LQFP]	ST-144
ADV7623BSTZ-P	Non-HDCP Transceiver	0°C to 70°C	144-Lead Low Profile Quad Flat Package [LQFP]	ST-144
ADV7623BSTZ-P-RL	Non-HDCP Transceiver (Reel)	0°C to 70°C	144-Lead Low Profile Quad Flat Package [LQFP]	ST-144
EVAL-ADV7623EB1Z	HDCP Transceiver Evaluation Board		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).

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