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REVISION HISTORY

5/2018—Rev. 0 to Rev. A

Changes to General Description Section ... 1

9/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

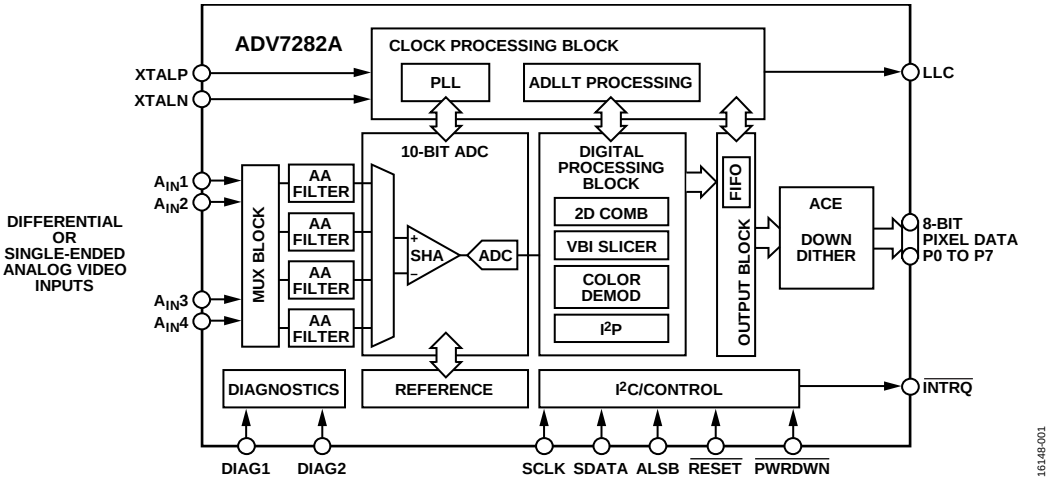

Figure 1. ADV7282A Functional Block Diagram

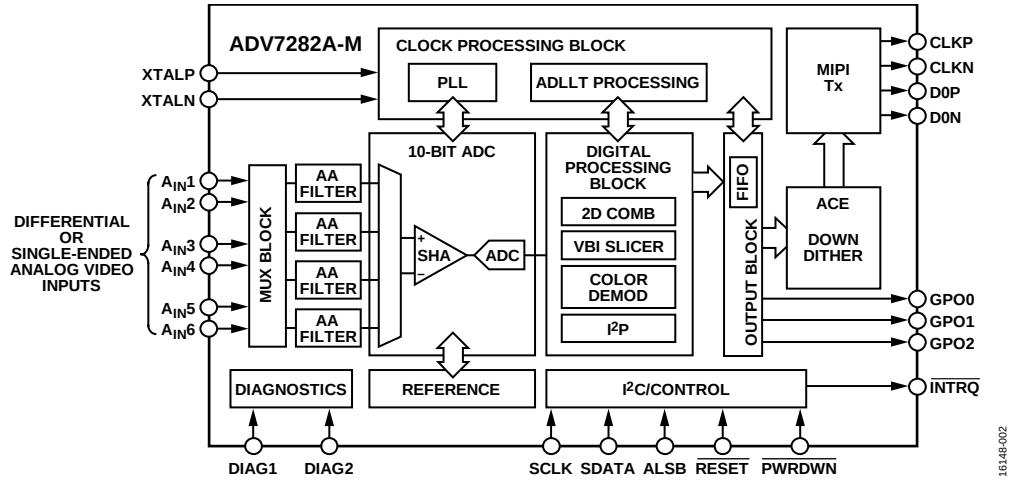

Figure 2. ADV7282A-M Functional Block Diagram

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

P_{VDD}, A_{VDD}, D_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at the operating temperature range, unless otherwise noted. M_{VDD} only applies to the ADV7282A-M.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
ADC Resolution	N				10	Bits
Integral Nonlinearity	INL	CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		±0.6		LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}	D_{VDDIO} = 3.3 V	2			V
		D_{VDDIO} = 1.8 V, ADV7282A only	1.2			V
Input Low Voltage	V_{IL}	D_{VDDIO} = 3.3 V			0.8	V
		D_{VDDIO} = 1.8 V, ADV7282A only			0.4	V
Input Leakage Current	I_{IN}	$\overline{\text{RESET}}$ pin	−10		+10	µA
		SDATA, SCLK pins	−10		+15	µA
		$\overline{\text{PWRDWN}}$, ALSB pins	−10		+50	µA
Input Capacitance	C_{IN}				10	pF
CRYSTAL INPUT						
Input High Voltage	V_{IH}	XTALN pin	1.2			V
Input Low Voltage	V_{IL}	XTALN pin			0.4	V
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	D_{VDDIO} = 3.3 V, I_{SOURCE} = 0.4 mA	2.4			V
		D_{VDDIO} = 1.8 V, I_{SOURCE} = 0.4 mA, ADV7282A only	1.4			V
Output Low Voltage	V_{OL}	D_{VDDIO} = 3.3 V, I_{SINK} = 3.2 mA			0.4	V
		D_{VDDIO} = 1.8 V, I_{SINK} = 1.6 mA, ADV7282A only			0.2	V
High Impedance Leakage Current	I_{LEAK}				10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[1, 2, 3]						
Digital Input/Output (I/O) Power Supply	D_{VDDIO}	ADV7282A-M	2.97	3.3	3.63	V
		ADV7282A	1.62	3.3	3.63	V
PLL Power Supply	P_{VDD}		1.71	1.8	1.89	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
Digital Power Supply	D_{VDD}		1.71	1.8	1.89	V
MIPI Transmitter (Tx) Power Supply	M_{VDD}	ADV7282A-M only	1.71	1.8	1.89	V
Digital I/O Supply Current	I_{DVDDIO}	ADV7282A-M		1.5		mA
		ADV7282A		5		mA
PLL Supply Current	I_{PVDD}			12		mA
MIPI Tx Supply Current	I_{MVDD}	ADV7282A-M only		14		mA
Analog Supply Current	I_{AVDD}					
Single-Ended CVBS Input				47		mA
Differential CVBS Input		Fully differential and pseudo differential CVBS		69		mA
Y/C Input				60		mA
YPrPb Input				75		mA
Digital Supply Current	I_{DVDD}					
Single-Ended CVBS Input				70		mA
Differential CVBS Input		Fully differential and pseudo differential CVBS		70		mA
Y/C Input				70		mA
YPrPb Input				70		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN CURRENTS[1]						
Digital I/O Supply	I_{DVDDIO_PD}			73		µA
PLL Supply	I_{PVDD_PD}			46		µA
Analog Supply	I_{AVDD_PD}			0.2		µA
Digital Supply	I_{DVDD_PD}			420		µA
MIPI Tx Supply	I_{MVDD_PD}			4.5		µA
Total Power Dissipation in Power-Down Mode				1		mW
CRYSTAL OSCILLATOR[1]						
Transconductance	g_M			30		mA/V

[1] Guaranteed by characterization.
[2] Typical current consumption values are measured with nominal voltage supply levels and a Society of Motion Picture and Television Engineers (SMPTE) bar test pattern.
[3] All specifications apply when the I²P core is activated, unless otherwise stated.

VIDEO SPECIFICATIONS

P_{VDD}, A_{VDD}, D_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization. M_{VDD} only applies to the ADV7282A-M.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS[1]						
Differential Phase	DP	CVBS input, modulated five-step		0.9		Degrees
Differential Gain	DG	CVBS input, modulated five-step		0.5		%
Luma Nonlinearity	LNL	CVBS input, five-step		2.0		%
NOISE SPECIFICATIONS						
Signal-to-Noise Ratio, Unweighted	SNR	Luma ramp		57.1		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
Common-Mode Rejection Ratio[2]	CMRR			73		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
Subcarrier Lock Range	f_{SC}			±1.3		kHz
Color Lock In Time				60		Lines
Synchronization Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed[3]				100		Lines
Fast Switch Speed[4]				100		ms
LUMA SPECIFICATIONS		CVBS, 1 V input				
Luma Brightness Accuracy				1		%
Luma Contrast Accuracy				1		%

[1] These specifications apply for all CVBS input types (NTSC, PAL, and SECAM), as well as for single-ended and differential CVBS inputs.
[2] The CMRR of this circuit design is critically dependent on the external resistor matching on the circuit inputs (see the Input Networks section). The CMRR measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.
[3] Autodetection switch speed is the time required for the ADV7282A to detect which video format is present at its input, for example, PAL I or NTSC M.
[4] Fast switch speed is the time required for the ADV7282A to switch from one analog input (single-ended or differential) to another, for example, switching from $A_{IN}1$ to $A_{IN}2$.

ANALOG SPECIFICATIONS

P_{VDD}, A_{VDD}, D_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization. M_{VDD} only applies to the ADV7282A-M.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance	Clamps switched off		10		MΩ
Large Clamp Source Current			0.4		mA
Large Clamp Sink Current			0.4		mA
Fine Clamp Source Current			10		µA
Fine Clamp Sink Current			10		µA

CLOCK AND I²C TIMING SPECIFICATIONS

A_{VDD}, D_{VDD}, P_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization. M_{VDD} only applies to the ADV7282A-M.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL					
Nominal Frequency			28.63636		MHz
Frequency Stability				±50	ppm
I²C PORT					
SCLK Frequency				400	kHz
SCLK Minimum Pulse Width High	t_1	0.6			µs
SCLK Minimum Pulse Width Low	t_2	1.3			µs
Hold Time (Start Condition)	t_3	0.6			µs
Setup Time (Start Condition)	t_4	0.6			µs
SDATA Setup Time	t_5	100			ns
SCLK and SDATA Rise Times	t_6			300	ns
SCLK and SDATA Fall Times	t_7			300	ns
Setup Time (Stop Condition)	t_8		0.6		µs
$\overline{\text{RESET}}$ INPUT					
$\overline{\text{RESET}}$ Pulse Width		5			ms

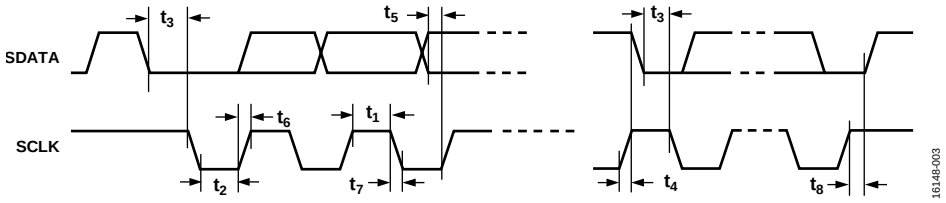

Figure 3. I²C Timing Diagram

MIPI Tx VIDEO OUTPUT AND TIMING SPECIFICATIONS (ADV7282A-M ONLY)

P_{VDD}, A_{VDD}, D_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. The ADV7282A MIPI Tx conforms to the MIPI D-PHY Version 1.00.00 specification by characterization. The MIPI Tx clock lane of the ADV7282A-M remains in high speed mode even when the data lane enters low power (LP) mode. For this reason, some measurements on the clock lane that pertain to low power mode are not applicable. Unless otherwise stated, all high speed measurements were performed with the ADV7282A-M operating in progressive mode and with a nominal 432 Mbps output data rate. Specifications guaranteed by characterization.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
UNIT INTERVAL	UI					
Interlaced Output				4.63		ns
Progressive Output				2.31		ns
DATA LANE LP MIPI Tx DC SPECIFICATIONS[1]						
Thevenin Output High Level	V_{OH}		1.1	1.2	1.3	V
Thevenin Output Low Level	V_{OL}		−50	0	+50	mV
DATA LANE LP MIPI Tx AC SPECIFICATIONS[1]						
Rise Time, 15% to 85%					25	ns
Fall Time, 85% to 15%					25	ns
Rise Time, 30% to 85%					35	ns
Data Lane LP Slew Rate vs. Load Capacitance (C_{LOAD})						
Maximum Slew Rate over Entire Vertical Edge Region		Rising edge			150	mV/ns
		Falling edge			150	mV/ns
Minimum Slew Rate						
400 mV ≤ V_{OUT} ≤ 930 mV		Falling edge	30			mV/ns
400 mV ≤ V_{OUT} ≤ 700 mV		Rising edge	30			mV/ns
700 mV ≤ V_{OUT} ≤ 930 mV		Rising edge	>0			mV/ns
Pulse Width of LP Exclusive OR Clock		First clock pulse after stop state or last pulse before stop state	40			ns
		All other clock pulses	20			ns
Period of LP Exclusive OR Clock			90			ns
CLOCK LANE LP MIPI Tx DC SPECIFICATIONS[1]						
Thevenin Output High Level	V_{OH}		1.1	1.2	1.3	V
Thevenin Output Low Level	V_{OL}		−50	0	+50	mV
CLOCK LANE LP MIPI Tx AC SPECIFICATIONS[1]						
Rise Time, 15% to 85%					25	ns
Fall Time, 85% to 15%					25	ns
Clock Lane LP Slew Rate						
Maximum Slew Rate over Entire Vertical Edge Region		Rising edge			150	mV/ns
		Falling edge			150	mV/ns
Minimum Slew Rate						
400 mV ≤ V_{OUT} ≤ 930 mV		Falling edge	30			mV/ns
400 mV ≤ V_{OUT} ≤ 700 mV		Rising edge	30			mV/ns
700 mV ≤ V_{OUT} ≤ 930 mV		Rising edge	>0			mV/ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DATA LANE HIGH SPEED MIPI Tx SIGNALING REQUIREMENTS		See Figure 4				
LP to High Speed Transition Stage	t_9	Time that the D0P pin is at V_{OL} and the D0N pin is at V_{OH}	50			ns
	t_{10}	Time that the D0P and D0N pins are at V_{OL}	40 + (4 × UI)		85 + (6 × UI)	ns
	t_{11}	t_{10} plus the high speed zero period	145 + (10 × UI)			ns
High Speed Differential Voltage Swing	$\|V_1\|$		140	200	270	mV p-p
Differential Voltage Mismatch					10	mV
Single-Ended Output High Voltages					360	mV
Static Common-Mode Voltage Level			150	200	250	mV
Static Common-Mode Voltage Mismatch					5	mV
Dynamic Common Level Variations						
50 MHz to 450 MHz					25	mV
Above 450 MHz					15	mV
Rise Time, 20% to 80%			0.15		0.3 × UI	ns
Fall Time, 80% to 20%			0.15		0.3 × UI	ns
High Speed to LP Transition Stage	t_{12}	Time that the ADV7282A-M drives the flipped last data bit after sending the last payload data bit of a high speed transmission burst	60 + (4 × UI)			ns
	t_{13}	Post end of transmission rise time (30% to 85%)			35	ns
	t_{14}	Time from start of t_{12} to start of low power state following a high speed transmission burst			105 + (12 × UI)	ns
	t_{15}	Time that a low power state is transmitted after a high speed transmission burst			100	ns
CLOCK LANE HIGH SPEED MIPI Tx SIGNALING REQUIREMENTS		See Figure 4				
LP to High Speed Transition Stage[2]		Time that the CLKP pin is at V_{OL} and the CLKN pin is at V_{OH}	50			ns
		Time that the CLKP and CLKN pins are at V_{OL}	38		95	ns
		Clock high speed zero period	300	500		ns
High Speed Differential Voltage Swing	$\|V_2\|$		140	200	270	mV p-p
Differential Voltage Mismatch					10	mV
Single-Ended Output High Voltages					360	mV
Static Common-Mode Voltage Level			150	200	250	mV
Static Common-Mode Voltage Mismatch					5	mV
Dynamic Common Level Variations						
50 MHz to 450 MHz					25	mV
Above 450 MHz					15	mV
Rise Time, 20% to 80%			0.15		0.3 × UI	ns
Fall Time, 80% to 20%			0.15		0.3 × UI	ns
HIGH SPEED MIPI Tx CLOCK TO DATA LANE TIMING REQUIREMENTS						
Data to Clock Skew			0.35 × UI		0.65 × UI	ns

[1] These measurements were performed with C_{LOAD} = 50 pF.
[2] The clock lane remains in high speed mode throughout normal operation. These results apply only to the ADV7282A-M during startup.

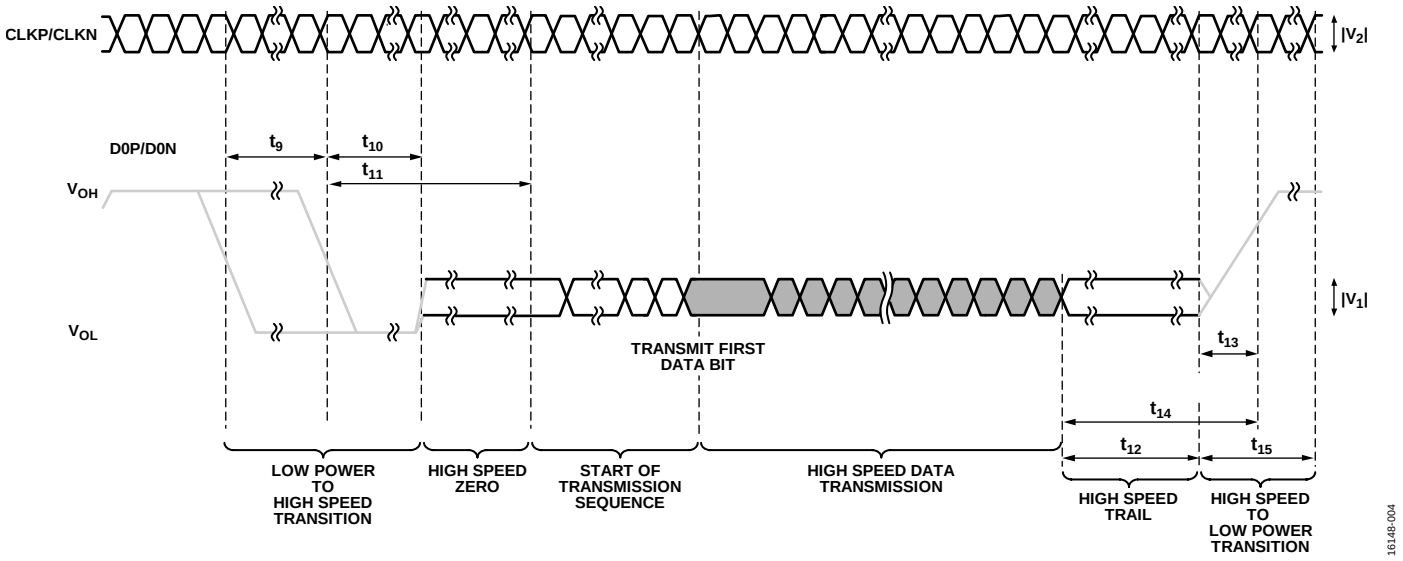

Figure 4. ADV7282A-M Output Timing Diagram (Conforms with MIPI Tx Specification)

PIXEL PORT TIMING SPECIFICATIONS (ADV7282A ONLY)

A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_{16}:t_{17}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{18}	Negative clock edge to start of valid data ($t_{SETUP} = t_{17} - t_{18}$)			3.8	ns
	t_{19}	End of valid data to negative clock edge ($t_{HOLD} = t_{16} - t_{19}$)			6.9	ns

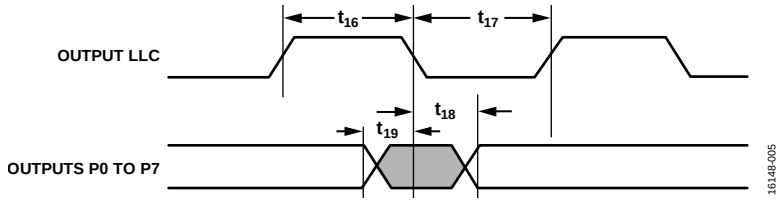

Figure 5. ADV7282A Pixel Port and Control Output Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter[1]	Rating
A_{VDD} to GND	2.2 V
D_{VDD} to GND	2.2 V
P_{VDD} to GND	2.2 V
M_{VDD} to GND[2]	2.2 V
D_{VDDIO} to GND	4 V
P_{VDD} to D_{VDD}	−0.9 V to +0.9 V
M_{VDD} to D_{VDD}[2]	−0.9 V to +0.9 V
A_{VDD} to D_{VDD}	−0.9 V to +0.9 V
Digital Inputs Voltage	GND − 0.3 V to D_{VDDIO} + 0.3 V
Digital Outputs Voltage	GND − 0.3 V to D_{VDDIO} + 0.3 V
Analog Inputs to Ground	GND − 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering (20 sec)	JEDEC J-STD-020

[1] The absolute maximum ratings assume that the DGND pins and the exposed pad of the ADV7282A are connected together to a common ground plane (GND). This is part of the recommended layout scheme. See the PCB Layout Recommendations section for more information. The absolute maximum ratings are stated in relation to this common ground plane.
[2] M_{VDD} only applies to the ADV7282A-M.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure as per JEDEC JESD51. Ψ_{JT} is the junction to top thermal characterization parameter measured on a standard test board, as per JEDEC JESD51, allowing the heat generated in the ADV7282A die to flow normally along preferred thermal conduction paths that more closely represent the thermal flows in a typical application board.

Table 8. Thermal Resistance

Package	θ_{JA}	Ψ_{JT}	Unit
CP-32-12[1]	39.6	0.86	°C/W

[1] JEDEC JESD51 2s2p 4-layer PCB with two signal layers and two buried solid ground planes (GND), and with nine thermal vias connecting the exposed pad to the ground plane (GND).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

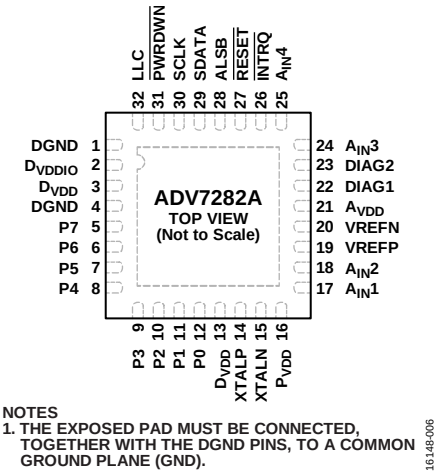

Figure 6. ADV7282A Pin Configuration

Table 9. Pin Function Descriptions, ADV7282A

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply.
2	D_{VDDIO}	Power	Digital I/O Power Supply (1.8 V or 3.3 V).
3, 13	D_{VDD}	Power	Digital Power Supply (1.8 V).
5 to 12	P7 to P0	Output	Video Pixel Output Ports.
14	XTALP	Output	Output Pin for the Crystal Oscillator Amplifier. Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7282A. The crystal used with the ADV7282A must be a fundamental mode crystal.
15	XTALN	Input	Input Pin for the Crystal Oscillator Amplifier. The crystal used with the ADV7282A must be a fundamental mode crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7282A, the output of the oscillator is fed into the XTALN pin.
16	P_{VDD}	Power	PLL Power Supply (1.8 V).
17, 18, 24, 25	$A_{IN}1$ to $A_{IN}4$	Input	Analog Video Input Channels.
19	VREFP	Output	Positive Internal Voltage Reference Output.
20	VREFN	Output	Negative Internal Voltage Reference Output.
21	A_{VDD}	Power	Analog Power Supply (1.8 V).
22	DIAG1	Input	Diagnostic Input 1.
23	DIAG2	Input	Diagnostic Input 2.
26	$\overline{\text{INTRQ}}$	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
27	$\overline{\text{RESET}}$	Input	System Reset Input (Active Low). A minimum low reset pulse width of 5 ms is required to reset the ADV7282A circuitry.
28	ALSB	Input	Address Least Significant Bit. This pin selects the I^2C write address for the ADV7282A. When ALSB is set to Logic 0, the write address is 0x40; when ALSB is set to Logic 1, the write address is 0x42.
29	SDATA	Input/output	I^2C Port Serial Data Input/Output.
30	SCLK	Input	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
31	$\overline{\text{PWRDWN}}$	Input	Power-Down. A logic low on this pin places the ADV7282A in power-down mode.
32	LLC	Output	Line Locked Clock for Output Pixel Data. The clock output is nominally 27 MHz, but it increases or decreases according to the video line length.
	EPAD (EP)		Exposed Ground Pad. The exposed pad must be connected, together with the DGND pins, to a common ground plane (GND).

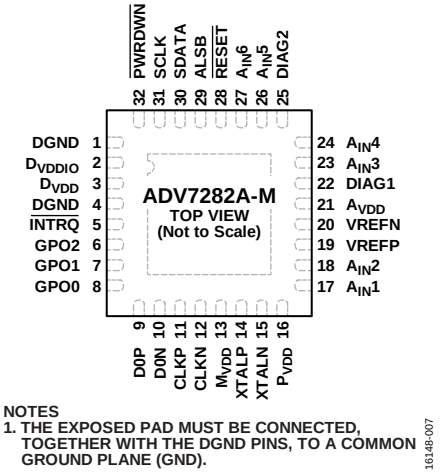

Figure 7. Pin Configuration, ADV7282A-M

Table 10. Pin Function Descriptions, ADV7282A-M

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply.
2	D_{VDDIO}	Power	Digital I/O Power Supply (3.3 V).
3	D_{VDD}	Power	Digital Power Supply (1.8 V).
5	$\overline{INTRQ}$	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
6 to 8	GPO2 to GPO0	Output	General-Purpose Outputs. These pins can be configured via I^2C to allow control of external devices.
9	D0P	Output	Positive MIPI Differential Data Output.
10	D0N	Output	Negative MIPI Differential Data Output.
11	CLKP	Output	Positive MIPI Differential Clock Output.
12	CLKN	Output	Negative MIPI Differential Clock Output.
13	M_{VDD}	Power	MIPI Digital Power Supply (1.8 V).
14	XTALP	Output	Output Pin for the Crystal Oscillator Amplifier. Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7282A-M. The crystal used with the ADV7282A-M must be a fundamental mode crystal.
15	XTALN	Input	Input Pin for the Crystal Oscillator Amplifier. The crystal used with the ADV7282A-M must be a fundamental mode crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7282A-M, the output of the oscillator is fed into the XTALN pin.
16	P_{VDD}	Power	PLL Power Supply (1.8 V).
17, 18, 23, 24, 26, 27	$A_{IN}1$ to $A_{IN}6$	Input	Analog Video Input Channels.
19	VREFP	Output	Positive Internal Voltage Reference Output.
20	VREFN	Output	Negative Internal Voltage Reference Output.
21	A_{VDD}	Power	Analog Power Supply (1.8 V).
22	DIAG1	Input	Diagnostic Input 1.
25	DIAG2	Input	Diagnostic Input 2.
28	$\overline{RESET}$	Input	System Reset Input (Active Low). A minimum low reset pulse width of 5 ms is required to reset the ADV7282A-M circuitry.
29	ALSB	Input	Address Least Significant Bit. This pin selects the I^2C write address for the ADV7282A-M. When ALSB is set to Logic 0, the write address is 0x40; when ALSB is set to Logic 1, the write address is 0x42.
30	SDATA	Input/output	I^2C Port Serial Data Input/Output.
31	SCLK	Input	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
32	$\overline{PWRDWN}$	Input	Power-Down. A logic low on this pin places the ADV7282A-M in power-down mode.
	EPAD (EP)		Exposed Ground Pad. The exposed pad must be connected, together with the DGND pins, to a common ground plane (GND).

THEORY OF OPERATION

The ADV7282A is a versatile one-chip, multiformat video decoder that automatically detects standard analog baseband video signals and converts them into a YCbCr 4:2:2 component video data stream. The ADV7282A supports video signals compatible with worldwide NTSC, PAL, and SECAM standards.

The analog front ends of the ADV7282A feature an input mux (4-channel for ADV7282A, 6-channel for ADV7282A-M), a differential to single-ended converter and a single 10-bit ADC. The analog video inputs accept single-ended, pseudo differential, and fully differential composite video signals as well as S-Video (Y/C) and YPbPr video signals, supporting a wide range of automotive and consumer video sources.

The incoming analog video is converted into a digital 8-bit YCrCb 4:2:2 video stream that is output either via a digital 8-bit ITU-R BT.656 video stream (ADV7282A) or via a MIPI Tx interface (ADV7282A-M). External horizontal sync (HS), vertical sync (VS), and field sync signals are available for the ITU-R BT.656 interface to provide timing references for LCD controllers and other video ASICs.

The ADV7282A features an advanced I^2P function to convert interlaced input video to a progressive video output with no requirement for external memory. The I^2P conversion uses edge adaptive technology to minimize video defects on low angle lines.

The ac-coupled connection of input video signals to the ADV7282A provides STB protection; two diagnostic sense inputs are available. The ADV7282A also offers a downdither mode, adaptive contrast enhancement (ACE) and general-purpose outputs (ADV7282A-M only).

The ADV7282A is programmed via a 2-wire, serial bidirectional port (I^2C compatible) and can communicate with other devices via a hardware interrupt pin, $\overline{\text{INTRQ}}$.

The ADV7282A is fabricated in a low power 1.8 V CMOS process and are provided in a space-saving LFCSP surface-mount, RoHS compliant package.

The ADV7282A is available in an automotive grade rated over the −40°C to +105°C temperature range, making them ideal for automotive applications.

ANALOG FRONT END

The analog front end (AFE) of the ADV7282A is composed of an input mux, a differential to single-ended converter with clamp circuitry, a set of four antialiasing filters, and a single 10-bit ADC.

The input mux (4-channel for ADV7282A, 6-channel for ADV7282A-M) enables multiple composite video signals to be applied to the SDP and is software controlled.

The next stage in the AFE features the differential to single-ended converter and the clamp circuitry. The incorporation of a differential front end allows differential video to connect directly to the ADV7282A. The differential front end enables small and large signal noise rejection, improved electromagnetic interference (EMI), and the ability to absorb ground bounce. The architecture can support true differential, pseudo differential, and single-ended signals.

In conjunction with an external resistor divider, the ADV7282A can provide a common-mode input range of 4 V, facilitating the removal of large signal, common-mode transients present on both video inputs.

The external resistor divider is required before each analog input channel to ensure that the input signal is kept within the range of the ADC. Current and voltage clamps in the circuit ensure that the video signal remains within the range on the ADC.

The single 10-bit ADC digitizes the analog video before it is applied to the SDP. Table 11 shows the three ADC clocking rates that are determined by the video input format to be processed. These clock rates ensure 4× oversampling per channel for CVBS, Y/C, and YPrPb modes.

Table 11. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS	57.27	4×
S-Video (Y/C)[2]	114	4×
YPrPb[2]	172	4×

[1] Based on a 28.63636 MHz clock input to the ADV7282A.
[2] Configuration writes are required for the different S-Video (Y/C) and YPrPb modes.

STANDARD DEFINITION PROCESSOR (SDP)

The SDP in the ADV7282A is capable of decoding a large selection of baseband video signals in composite (both single-ended and differential), S-Video (Y/C), and component formats. The video standards supported by the video processor include

- PAL B, PAL D, PAL G, PAL H, PAL I, PAL M, PAL N, PAL Nc, PAL 60
- NTSC J, NTSC M, NTSC 4.43
- SECAM B, SECAM D, SECAM G, SECAM K, SECAM L

The SDP in the ADV7282A can automatically detect the video standard and process it accordingly.

The ADV7282A has a five-line, superadaptive, 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without requiring user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available in the ADV7282A.

The ADV7282A implements a patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7282A to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs, VCD players, and

camcorders. The ADV7282A contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ADV7282A features an automatic gain control (AGC) algorithm to ensure that the optimum luma gain is selected as the input video varies in brightness.

ACE is an algorithm that automatically varies the contrast level applied across an image to enhance the picture detail visible. This automatic variation enables the contrast in the dark areas of an image to be increased without saturating the bright areas, which is particularly useful in automotive applications where it can be important to be able to clearly discern objects in shaded areas.

Downdithering from eight bits to six bits enables ease of design for standard LCD panels.

The SDP can handle a variety of vertical blanking interval (VBI) data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management system (CGMS), and teletext data slicing for world standard teletext (WST). Data is transmitted via the 8-bit video output port as ancillary data packets (ANC).

The ADV7282A is fully Rovi™ (formerly Macrovision® and now rebranded as TiVo upon acquisition of the same) compliant; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The SDP is fully robust to all Rovi signal inputs.

POWER SUPPLY SEQUENCING

OPTIMAL POWER-UP SEQUENCE

The optimal power-up sequence for the ADV7282A is guaranteed by production testing.

The optimal power-up sequence for the ADV7282A is to first power up the 3.3 V D_{VDDIO} supply, followed by the 1.8 V supplies: D_{VDD}, P_{VDD}, A_{VDD}, and M_{VDD} (for the ADV7282A-M).

When powering up the ADV7282A, follow these steps. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

1. Assert the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins (pull the pins low).
2. Power up the D_{VDDIO} supply.
3. After D_{VDDIO} is fully asserted, power up the 1.8 V supplies.
4. After the 1.8 V supplies are fully asserted, pull the $\overline{\text{PWRDWN}}$ pin high.
5. Wait 5 ms and then pull the $\overline{\text{RESET}}$ pin high.
6. After all power supplies and the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins are powered up and stable, wait an additional 5 ms before initiating I^2C communication with the ADV7282A-M.

SIMPLIFIED POWER-UP SEQUENCE

The simplified power-up sequence is guaranteed by characterization.

Alternatively, the ADV7282A can be powered up by asserting all supplies and the $\overline{\text{PWRDWN}}$ pin simultaneously. During this operation, the $\overline{\text{RESET}}$ pin must remain low. After the supplies and $\overline{\text{PWRDWN}}$ are fully asserted, wait for at least 5 ms before bringing the $\overline{\text{RESET}}$ pin high. After the $\overline{\text{RESET}}$ pin is fully asserted wait a further 5 ms before initiating I^2C communication with the ADV7282A.

While the supplies are established, ensure that a lower rated supply does not go above a higher rated supply level. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

POWER-DOWN SEQUENCE

The ADV7282A supplies can be deasserted simultaneously if D_{VDDIO} does not go below a lower rated supply.

D_{VDDIO} SUPPLY VOLTAGE

For correct operation of the ADV7282A-M, the D_{VDDIO} supply must be from 2.97 V to 3.63 V.

The ADV7282A, however, can operate with a nominal D_{VDDIO} voltage of 1.8 V. In this case, apply the power-up sequences described in the Optimal Power-Up Sequence section. The only change is that D_{VDDIO} is powered up to 1.8 V instead of 3.3 V, and the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins of the ADV7282A are powered up to 1.8 V instead of 3.3 V.

When the ADV7282A operates with a nominal D_{VDDIO} voltage of 1.8 V, set the drive strength of all digital outputs to the maximum values.

When D_{VDDIO} is 1.8 V, do not pull any pin of the ADV7282A up to 3.3 V. For example, the I^2C pins of the ADV7282A (SCLK and SDATA) must also be pulled up to 1.8 V instead of 3.3 V.

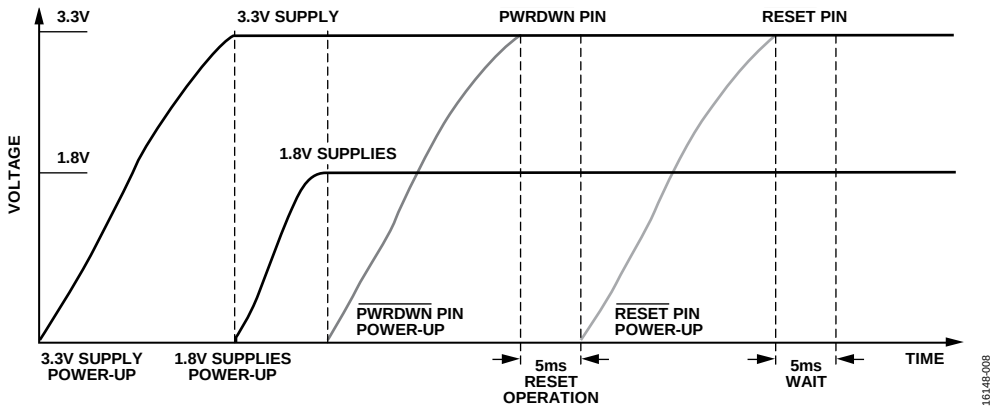

Figure 8. Optimal Power-Up Sequence

CRYSTAL OSCILLATOR DESIGN

The ADV7282A needs a stable and accurate clock source to guarantee their operation. This clock is typically provided by a crystal resonator (XTAL) but can also be provided by a clock oscillator.

The required circuitry for an XTAL is illustrated in Figure 18 and Figure 19. A damping resistor (R_{DAMP}) is required on the output of the ADV7282A XTAL amplifier (XTALP). The purpose of this damping resistor is to limit the current flowing through the XTAL and to limit the voltage across the XTAL amplifier. To define the appropriate value of the damping resistor R_{DAMP} (see the Typical Circuit Connections section), consult the accompanying calculator tool (visit the design resources section at www.analog.com/ADV7282A to download).

The other components in the XTAL circuit must be chosen carefully, for example, incorrectly selected load capacitors may result in an offset to the crystal oscillation frequency. For more information on such considerations, see the AN-1260 Application Note, *Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers*. After the XTAL circuit is defined, it is recommended to consult with the XTAL vendor to ensure that the design operates with sufficient margin across all conditions.

The evaluation of the ADV7282A was completed using an XTAL with typical characteristics (see Table 12).

Table 12. Reference XTAL Characteristics

Characteristic	Value	Unit
Package	3.2 × 2.5 × 0.8	mm
Nominal Frequency	28.63636	MHz
Mode of Oscillation	Fundamental	
Frequency Calibration (at 25°C)	±20	ppm
Frequency Temperature Stability Tolerance	±50	ppm
Operating Temperature Range	−40 to +125	°C
Maximum Equivalent Series Resistance	25	Ω
Load Capacitance	12	pF
Drive Level	200	µW
Shunt Capacitance (Maximum)	5	pF
Aging per Year	±3	ppm

The values in Table 12 are provided for reference only. It is recommended to characterize the operation of the XTAL circuit thoroughly across the operating temperature range of the application, in conjunction with the XTAL vendor, prior to releasing any new design.

INPUT NETWORKS

An input network (external resistor and capacitor circuit) is required on the AINx input pins of the ADV7282A. The components of the input network depend on the video format selected for the analog input.

SINGLE-ENDED INPUT NETWORK

Figure 9 shows the input network to use on each AINx input pin of the ADV7282A when using any of the following video input formats:

- Single-ended CVBS
- YC (S-Video)
- YPrPb

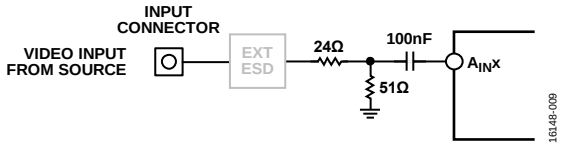

Figure 9. Single-Ended Input Network

The 24 Ω and 51 Ω resistors supply the 75 Ω end termination required for the analog video input. These resistors also create a resistor divider with a gain of 0.68. The resistor divider attenuates the amplitude of the input analog video and scales the input to the ADC range of the ADV7282A. This resistor divider allows an input range to the ADV7282A of up to 1.47 V p-p. Amplifiers within the ADC restore the amplitude of the input signal so that SNR performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into an AINx pin. The clamping circuitry within the ADV7282A restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the ADV7282A.

DIFFERENTIAL INPUT NETWORK

Figure 10 shows the input network to use when differential CVBS video is input on the AINx input pins of the ADV7282A.

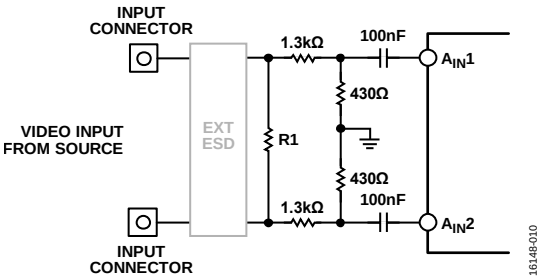

Figure 10. Differential Input Network

Fully differential video transmission involves transmitting two complementary CVBS signals. Pseudo differential video transmission involves transmitting a CVBS signal and a source ground signal.

Differential video transmission has several key advantages over single-ended transmission, including the following:

- Inherent small signal and large signal noise rejection
- Improved EMI performance
- Ability to absorb ground bounce

Resistor R1 provides the radio frequency (RF) end termination for the differential CVBS input lines. For a pseudo differential CVBS input, a value of 75 Ω is recommended for R1. For a fully differential CVBS input, a value of 150 Ω is recommended for R1.

The 1.3 kΩ and 430 Ω resistors create a resistor divider with a gain of 0.25. The resistor divider attenuates the amplitude of the input analog video, but increases the input common-mode range of the ADV7282A to 4 V p-p. Amplifiers within the ADC restore the amplitude of the input signal to maintain SNR performance.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into an AINx pin of the ADV7282A. The clamping circuitry within the ADV7282A restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the ADV7282A.

The combination of the 1.3 kΩ and 430 Ω resistors and the 100 nF ac coupling capacitors limits the current flow into the ADV7282A during STB events (see the STB Protection section).

To achieve optimal performance, the 1.3 kΩ and 430 Ω resistors must be closely matched; that is, all 1.3 kΩ and 430 Ω resistors must have the same resistance tolerance, and this tolerance must be as low as possible.

STB PROTECTION

In differential mode, the ADV7282A is protected against STB events by the external 100 nF ac coupling capacitors (see Figure 10). The external input network resistors are sized to be large enough to reduce the current flow during an STB event but small enough not to affect the operation of the ADV7282A.

The power rating of the input network resistors must be chosen to withstand the high voltages of STB events. Similarly, the breakdown voltage of the ac coupling capacitors must be chosen to be robust to STB events. The R1 resistor is protected because no current or limited current flows through it during an STB event.

The ADV7282A provides two STB diagnostic pins that generate an interrupt when an STB event occurs. For more information, see the STB Diagnostics section.

APPLICATIONS INFORMATION

INPUT CONFIGURATION

The input format of the ADV7282A is specified using the INSEL[4:0] bits (see Table 13). These bits also configure the SDP core to process CVBS, differential CVBS, S-Video (Y/C), or component (YPrPb) format. The INSEL[4:0] bits are located in the user sub map at Address 0x00, Bits[4:0]. For more information about the registers, see the Register Maps section.

The INSEL[4:0] bits specify predefined analog input routing schemes, eliminating the need for manual mux programming and allowing the user to route the various video signal types to the decoder. For example, if the CVBS input is selected, the remaining channels are powered down.

STB DIAGNOSTICS

The ADV7282A senses an STB event via the DIAG1 and DIAG2 pins. The DIAG1 and DIAG2 pins can sense an STB event on either the positive or the negative differential input because of the negligible voltage drop across Resistor R1.

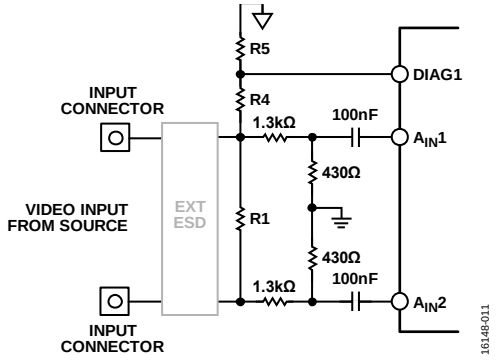

Figure 11. Diagnostic Connections

Resistors R4 and R5 divide down the voltage at the input connector to protect a DIAGx pin from an STB event. The DIAGx pin circuitry compares this voltage to a programmable reference voltage, known as the diagnostic slice level. When the diagnostic slice level is exceeded, an STB event occurs.

Table 13. Input Format Specified by the INSEL[4:0] Bits

INSEL[4:0] Bit Value	Video Format	Analog Inputs	
		ADV7282A	ADV7282A-M
00000	CVBS	CVBS input on $A_{IN}1$	CVBS input on $A_{IN}1$
00001	CVBS	CVBS input on $A_{IN}2$	CVBS input on $A_{IN}2$
00010	CVBS	Reserved	CVBS input on $A_{IN}3$
00011	CVBS	Reserved	CVBS input on $A_{IN}4$
00100	Reserved	Reserved	Reserved
00101	Reserved	Reserved	Reserved
00110	CVBS	CVBS input on $A_{IN}3$	CVBS input on $A_{IN}5$
00111	CVBS	CVBS input on $A_{IN}4$	CVBS input on $A_{IN}6$
01000	S-Video (Y/C)	Y input on $A_{IN}1$; C input on $A_{IN}2$	Y input on $A_{IN}1$; C input on $A_{IN}2$
01001	S-Video (Y/C)	Reserved	Y input on $A_{IN}3$; C input on $A_{IN}4$
01010	Reserved	Reserved	Reserved
01011	S-Video (Y/C)	Y input on $A_{IN}3$; C input on $A_{IN}4$	Y input on $A_{IN}5$; C input on $A_{IN}6$
01100	YPrPb	Reserved[1]	Y input on $A_{IN}1$; Pb input on $A_{IN}2$; Pr input on $A_{IN}3$
01101	Reserved	Reserved	Reserved
01110	Differential CVBS	Positive input on $A_{IN}1$; negative input on $A_{IN}2$	Positive input on $A_{IN}1$; negative input on $A_{IN}2$
01111	Differential CVBS	Reserved	Positive input on $A_{IN}3$; negative input on $A_{IN}4$
10000	Reserved	Reserved	Reserved
10001	Differential CVBS	Positive input on $A_{IN}3$; negative input on $A_{IN}4$	Positive input on $A_{IN}5$; negative input on $A_{IN}6$
10010 to 11111	Reserved	Reserved	Reserved

[1] Note that it is possible for the ADV7282A to receive YPbPr formats; however, a manual muxing scheme is required. In this case luma (Y) is fed in on $A_{IN}1$ or $A_{IN}3$, blue chroma (Pb) is fed in on $A_{IN}4$, and red chroma (Pr) is fed in on $A_{IN}2$.

When a DIAGx pin voltage exceeds the diagnostic slice level voltage, a hardware interrupt is triggered and indicated by the INTRQ pin. A readback register is also provided, allowing the user to determine the DIAGx pin on which the STB event occurred.

Use Equation 1 to find the trigger voltage for a selected diagnostic slice level.

$$V_{STB\_TRIGGER} = \frac{R5+R4}{R5} \times DIAGNOSTIC\_SLICE\_LEVEL \quad (1)$$

where:
$V_{STB\_TRIGGER}$ is the minimum voltage required at the input connector to trigger the STB interrupt on the ADV7282A.
DIAGNOSTIC_SLICE_LEVEL is the programmable reference voltage.

PROGRAMMING THE STB DIAGNOSTIC FUNCTION

By default, the STB diagnostic function is disabled on the ADV7282A. To enable the diagnostic function, follow the instructions in this section.

DIAG1 Pin

DIAG1_SLICER_PWRDN, Address 0x5D, Bit 6, User Sub Map

This bit powers up or powers down the diagnostic circuitry for the DIAG1 pin.

Table 14. DIAG1_SLICER_PWRDN Function

DIAG1_SLICER_PWRDN Setting	Diagnostic Slice Level
0	Power up the diagnostic circuitry for the DIAG1 pin.
1 (Default)	Power down the diagnostic circuitry for the DIAG1 pin.

DIAG1_SLICE_LEVEL[2:0], Address 0x5D, Bits[4:2], User Sub Map

The DIAG1_SLICE_LEVEL[2:0] bits allow the user to set the diagnostic slice level for the DIAG1 pin. When a voltage greater than the diagnostic slice level is seen on the DIAG1 pin, an STB interrupt is triggered.

For the diagnostic slice level to be set correctly, the diagnostic circuitry for the DIAG1 pin must be powered up (see Table 14).

Table 15. DIAG1_SLICE_LEVEL[2:0] Settings

DIAG1_SLICE_LEVEL[2:0] Setting	Diagnostic Slice Level
000	75 mV
001	225 mV
010	375 mV
011 (Default)	525 mV
100	675 mV
101	825 mV
110	975 mV
111	1.125 V

DIAG2 Pin

DIAG2_SLICER_PWRDN, Address 0x5E, Bit 6, User Sub Map

This bit powers up or powers down the diagnostic circuitry for the DIAG2 pin.

Table 16. DIAG2_SLICER_PWRDN Function

DIAG2_SLICER_PWRDN Setting	Diagnostic Slice Level
0	Power up the diagnostic circuitry for the DIAG2 pin.
1 (Default)	Power down the diagnostic circuitry for the DIAG2 pin.

DIAG2_SLICE_LEVEL[2:0], Address 0x5E, Bits[4:2], User Sub Map

The DIAG2_SLICE_LEVEL[2:0] bits allow the user to set the diagnostic slice level for the DIAG2 pin. When a voltage greater than the diagnostic slice level is seen on the DIAG2 pin, an STB interrupt is triggered.

For the diagnostic slice level to be set correctly, the diagnostic circuitry for the DIAG2 pin must be powered up (see Table 16).

Table 17. DIAG2_SLICE_LEVEL[2:0] Settings

DIAG2_SLICE_LEVEL[2:0] Setting	Diagnostic Slice Level
000	75 mV
001	225 mV
010	375 mV
011 (Default)	525 mV
100	675 mV
101	825 mV
110	975 mV
111	1.125 V

ADAPTIVE CONTRAST ENHANCEMENT (ACE)

The ADV7282A can increase the contrast of an image depending on the content of the picture, brightening and darkening areas. The optional ACE feature enables the contrast within dark areas to increase without significantly affecting the bright areas. The ACE feature is particularly useful in automotive applications, where it can be important to discern objects in shaded areas.

The ACE function is disabled by default. To enable the ACE function, execute the register writes shown in Table 18. To disable the ACE function, execute the register writes shown in Table 19.

I²P FUNCTION

The advanced I²P function allows the ADV7282A to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. The ADV7282A uses edge adaptive technology to minimize video defects on low angle lines.

The I²P function is disabled by default. To enable the I²P function, use the recommended scripts from Analog Devices, Inc., available at www.analog.com/ADV7282A.

ITU-R BT.656 Tx CONFIGURATION (ADV7282A ONLY)

The ADV7282A receives analog video and outputs digital video according to the ITU-R BT.656 specification. The ADV7282A outputs the ITU-R BT.656 video data stream over the P0 to P7 data pins and has an LLC pin.

Video data is output over the P0 to P7 pins in YCrCb 4:2:2 format. Synchronization signals are automatically embedded in the video data signal in accordance with the ITU-R BT.656 specification.

The LLC output clocks the output data on the P0 to P7 pins at a nominal frequency of 27 MHz.

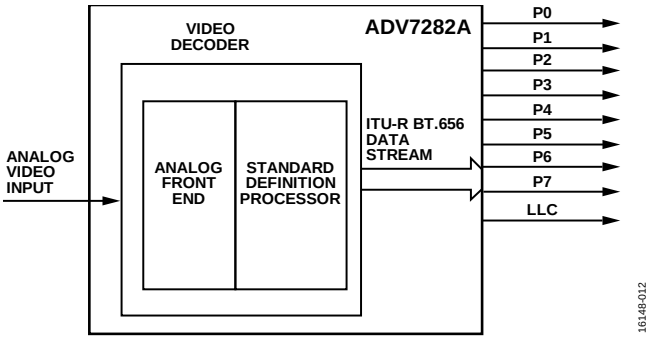

Figure 12. ITU-R BT.656 Output Stage of the ADV7282A

Table 18. Register Writes to Enable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x80	Enable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter user sub map

Table 19. Register Writes to Disable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x00	Disable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter user sub map

MIPI Tx OUTPUT (ADV7282A-M ONLY)

The decoder in the ADV7282A-M outputs an ITU-R BT.656 data stream. The ITU-R BT.656 data stream is connected into a CSI-2 Tx module. Data from the CSI-2 Tx module is fed into a D-PHY physical layer and output serially from the device.

The output of the ADV7282A-M consists of a single data channel on the D0P and D0N lanes and a clock channel on the CLKP and CLKN lanes.

Video data is output over the data lanes in high speed mode. The data lanes enter low power mode during the horizontal and vertical blanking periods.

The clock lanes clock the output video. After the ADV7282A-M is programmed, the clock lanes exit low power mode and remain in high speed mode until the device is reset or powered down.

The ADV7282A-M outputs video data in an 8-bit, YCrCb, 4:2:2 format. When the I²P core is disabled, the video data is output in an interlaced format at a nominal data rate of 216 Mbps. When the I²P core is enabled, the video data is output in a progressive format at a nominal data rate of 432 Mbps (see the I²P Function section for more information).

I²C PORT DESCRIPTION

The ADV7282A supports a 2-wire, I²C-compatible serial interface. Two inputs, serial data (SDATA) and serial clock (SCLK), carry information between the ADV7282A and the system I²C master controller. The I²C port of the ADV7282A allows the user to set up and configure the decoder and to read back captured VBI data.

The ADV7282A has a variety of possible I²C slave addresses and subaddresses (see the Register Maps section). The main map of the ADV7282A has four possible slave addresses for read and write operations, depending on the logic level of the ALSB pin (see Table 20).

Table 20. Main Map I²C Addresses

ALSB Pin	R/$\overline{W}$ Bit	Slave Address
0	0	0x40 (write)
0	1	0x41 (read)
1	0	0x42 (write)
1	1	0x43 (read)

The ALSB pin controls Bit 1 of the slave address. By changing the logic level of the ALSB pin, it is possible to control two ADV7282A devices in an application without using the same I²C slave address. The LSB (Bit 0) specifies either a read or write operation: Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation.

To control the device on the bus, use the following protocol:

1. The master initiates a data transfer by establishing a start condition, defined as a high to low transition on SDATA while SCLK remains high, and indicates that an address/data stream follows.
2. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit). The bits are transferred from MSB to LSB.
3. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge (ACK) bit.
4. All other devices withdraw from the bus and maintain an idle condition. In the idle condition, the device monitors the SDATA and SCLK lines for the start condition and the correct transmitted address.

The R/$\overline{W}$ bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

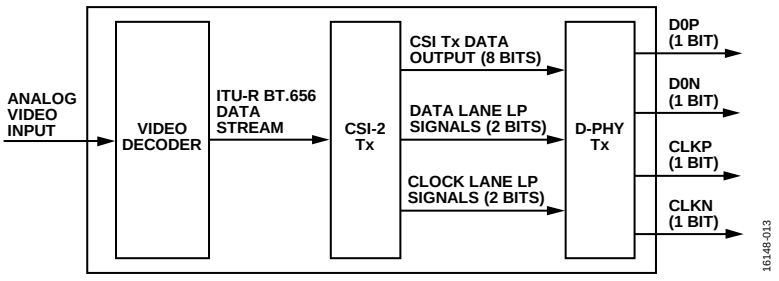

Figure 13. MIPI Tx Output Stage of the ADV7282A-M

The ADV7282A acts as standard I²C slave devices on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit address plus the R/$\overline{W}$ bit. The device has subaddresses to enable access to the internal registers; therefore, it interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register individually without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7282A does not issue an acknowledge, and returns to the idle condition.

If the highest subaddress is exceeded in auto-increment mode, take one of the following actions:

- In read mode, the register contents of the highest subaddress continue to output until the master device issues a no acknowledge, indicating the end of a read. A no acknowledge condition occurs when the SDATA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into a subaddress register. A no acknowledge is issued by the ADV7282A, and the device returns to the idle condition.

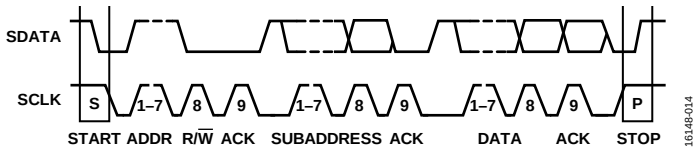

Figure 14. Bus Data Transfer

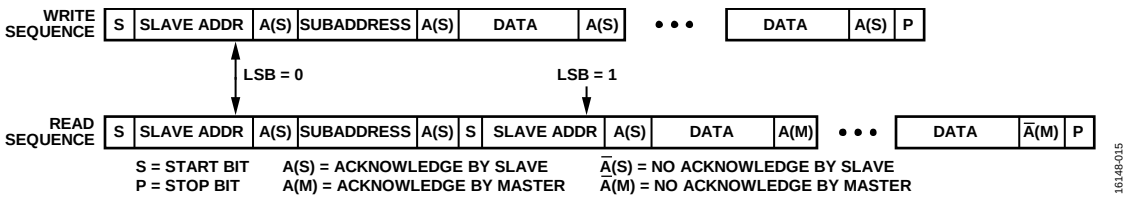

Figure 15. Read and Write Sequence

REGISTER MAPS

The ADV7282A contains three register maps: the main register map, the video postprocessor (VPP) map, and the CSI map.

The main register map contains three sub maps: the user sub map, the interrupt/VDP sub map, and User Sub Map 2 (see Figure 16).

For more information about the ADV7282A registers, see the ADV7280A/ADV7281A/ADV7282A Device Manual.

Main Map

The I²C slave address of the main map of the ADV7282A is set by the ALSB pin (see Table 20). The main map allows the user to program the I²C slave addresses of the VPP and CSI maps. The three sub maps are accessed by writing to the SUB_USR_EN[1:0] bits (Address 0x0E, Bits[6:5]) within the user sub map (see Figure 16 and Table 21).

User Sub Map

The user sub map contains registers that program the AFE and digital core of the ADV7282A. The user sub map has the same I²C slave address as the main map. To access the user sub map, set the SUB_USR_EN[1:0] bits in the user sub map (Address 0x0E, Bits[6:5]) to 00.

Interrupt/VDP Sub Map

The interrupt/VDP sub map contains registers that program internal interrupts, control the INTRQ pin, and decode VBI data.

The interrupt/VDP sub map has the same I²C slave address as the main map. To access the interrupt/VDP sub map, set the SUB_USR_EN[1:0] bits in the main map (Address 0x0E, Bits[6:5]) to 01.

User Sub Map 2

User Sub Map 2 contains registers that control the ACE, down-dither, and fast lock functions. It also contains controls that set the acceptable input luma and chroma limits before the ADV7282A enters free run and color kill modes.

User Sub Map 2 has the same I²C slave address as the main map. To access User Sub Map 2, set the SUB_USR_EN[1:0] bits in the user sub map (Address 0x0E, Bits[6:5]) to 10.

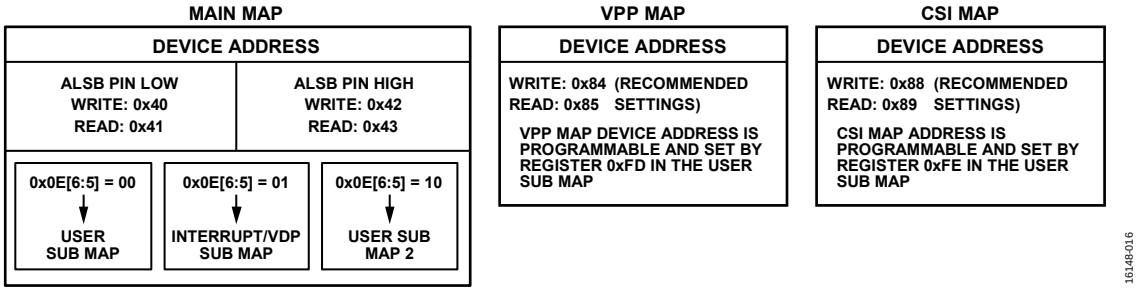

Figure 16. Register Map and Sub Map Access

Table 21. I²C Register Map and Sub Map Addresses

ALSB Pin	R/W Bit	Slave Address	SUB_USR_EN[1:0] Bits (Address 0x0E, Bits[6:5])	Register Map or Sub Map
0	0 (write)	0x40	00	User sub map
0	1 (read)	0x41	00	User sub map
0	0 (write)	0x40	01	Interrupt/VDP sub map
0	1 (read)	0x41	01	Interrupt/VDP sub map
0	0 (write)	0x40	10	User Sub Map 2
0	1 (read)	0x41	10	User Sub Map 2
1	0 (write)	0x42	00	User sub map
1	1 (read)	0x43	00	User sub map
1	0 (write)	0x42	01	Interrupt/VDP sub map
1	1 (read)	0x43	01	Interrupt/VDP sub map
1	0 (write)	0x42	10	User Sub Map 2
1	1 (read)	0x43	10	User Sub Map 2
X[1]	0 (write)	0x84	XX[1]	VPP map
X[1]	1 (read)	0x85	XX[1]	VPP map
X[1]	0 (write)	0x88	XX[1]	CSI map (ADV7282A-M only)
X[1]	1 (read)	0x89	XX[1]	CSI map (ADV7282A-M only)

[1] X and XX mean don't care.

VPP Map

The video postprocessor (VPP) map contains registers that control the I²P core (interlaced to progressive converter).

The VPP map has a programmable I²C slave address, which is programmed using Register 0xFD in the user sub map of the main map. The default value for the VPP map address is 0x00; however, the VPP map cannot be accessed until the I²C slave address is reset. The recommended I²C slave address for the VPP map is 0x84.

To reset the I²C slave address of the VPP map, write to the VPP_SLAVE_ADDR[7:1] bits in the main register map (Address 0xFD, Bits[7:1]). Set these bits to a value of 0x84 (I²C write address; I²C read address is 0x85).

CSI Map (ADV7282A-M Only)

The CSI map contains registers that control the MIPI Tx output stream from the ADV7282A-M.

The CSI map has a programmable I²C slave address, which is programmed using Register 0xFE in the user sub map. The default value for the CSI map address is 0x00; however, the CSI map cannot be accessed until the I²C slave address is reset. The recommended I²C slave address for the CSI map is 0x88.

To reset the I²C slave address of the CSI map, write to the CSI_TX_SLAVE_ADDR[7:1] bits in the user sub map (Address 0xFE, Bits[7:1]). Set these bits to a value of 0x88 (I²C write address; I²C read address is 0x89).

SUB_USR_EN[1:0] Bits, Address 0x0E, Bits[6:5]

The user sub map is available by default. The other two sub maps are accessed using the SUB_USR_EN[1:0] bits. When programming of the interrupt/VDP map or User Sub Map 2 is completed, it is necessary to write to the SUB_USR_EN[1:0] bits to return to the user sub map.

PCB LAYOUT RECOMMENDATIONS

The ADV7282A is a high precision, high speed, mixed-signal device. To achieve maximum performance from the device, it is important to use a well designed PCB. This section provides guidelines for designing a PCB for use with the ADV7282A.

ANALOG INTERFACE INPUTS

When routing the analog interface inputs on the PCB, keep track lengths to a minimum. Use 75 Ω trace impedances when possible; trace impedances other than 75 Ω increase the chance of reflections.

POWER SUPPLY DECOUPLING

It is recommended that each power supply pin be decoupled with 100 nF and 10 nF capacitors. The basic principle is to place a decoupling capacitor within approximately 0.5 cm of the P_{VDD}, A_{VDD}, D_{VDD}, and M_{VDD} pins. Avoid placing the decoupling capacitors on the opposite side of the PCB from the ADV7282A because doing so introduces inductive vias in the path.

Place the decoupling capacitors between the power plane and the power pin. Current flows from the power plane to the capacitor and then to the power pin. Do not apply the power connection between the capacitor and the power pin. The best approach is to place a via near, or beneath, the decoupling capacitor pads down to the power plane (see Figure 17).

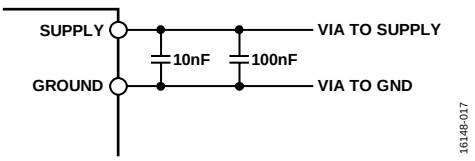

Figure 17. Recommended Power Supply Decoupling

Ensure that the power supplies connected to the ADV7282A, P_{VDD} and M_{VDD} (M_{VDD} only applies to the ADV7282A-M model) in particular, are well regulated and filtered. For optimum performance of the ADV7282A, it is recommended to isolate each supply and to use decoupling on each pin, located as physically close to the ADV7282A package as possible.

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This disparity can result in a measurable change in the voltage supplied to the analog supply regulator, which can, in turn, produce changes in the regulated analog supply voltage. This problem can be mitigated by regulating the analog supply, or at least the P_{VDD} supply, from a different, cleaner power source, for example, from a 12 V supply.

Using a single ground plane for the entire board is also recommended. Experience has shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

VREFN AND VREFP PINS

Place the circuit associated with the VREFN and VREFP pins as close as possible to the ADV7282A and on the same side of the PCB as the device.

DIGITAL OUTPUTS

The ADV7282A digital outputs are $\overline{\text{INTRQ}}$, LLC, and P0 to P7. The ADV7282A-M digital outputs are $\overline{\text{INTRQ}}$ and GPO0 to GPO2.

Minimize the trace length that the digital outputs must drive. Longer traces have higher capacitance, requiring more current and, in turn, causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a 30 Ω to 50 Ω series resistor can suppress reflections, reduce EMI, and reduce current spikes inside the ADV7282A. If using series resistors, place them as close as possible to the pins of the ADV7282A. However, try not to add vias or extra length to the output trace in an attempt to place the resistors closer.

If possible, limit the capacitance that each digital output must drive to less than 15 pF. This recommendation can be easily accommodated by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV7282A, creating more digital noise on the power supplies.

EXPOSED METAL PAD

The ADV7282A has an exposed metal pad on the bottom of the package. This pad must be soldered to ground. The exposed pad is used for proper heat dissipation, noise suppression, and mechanical strength.

DIGITAL INPUTS

The digital inputs of the ADV7282A are designed to work with 1.8 V signals (3.3 V for D_{VDDIO}) and are not tolerant of 5 V signals. Extra components are required if 5 V logic signals must be applied to the decoder.

MIPI Tx OUTPUTS (ADV7282A-M ONLY)

It is recommended that the MIPI Tx output traces be kept as short as possible and on the same side of the PCB as the ADV7282A-M device. It is also recommended that a solid plane (preferably a ground plane) be placed on the layer adjacent to the MIPI Tx traces to provide a solid reference plane.

MIPI Tx transmission operates in both differential and single-ended modes. During high speed transmission, the pair of outputs operates in differential mode; in low power mode, the pair operates as two independent single-ended traces. Therefore, it is recommended that each output pair be routed as two loosely coupled 50 Ω single-ended traces to reduce the risk of crosstalk between the two traces in low power mode.

TYPICAL CIRCUIT CONNECTIONS

Figure 18 provides an example of how to connect the ADV7282A. Figure 19 provides an example of how to connect the ADV7282A-M.

For detailed schematics of the ADV7282A evaluation boards, visit the ADV7282A product page at www.analog.com/ADV7282A.

See the XTAL data sheet (from the XTAL vendor), the AN-1260 Application Note, and the calculator tool (visit the design resources section at www.analog.com/ADV7282A to download) for the correct values for C1, C2, and R_{DAMP}.

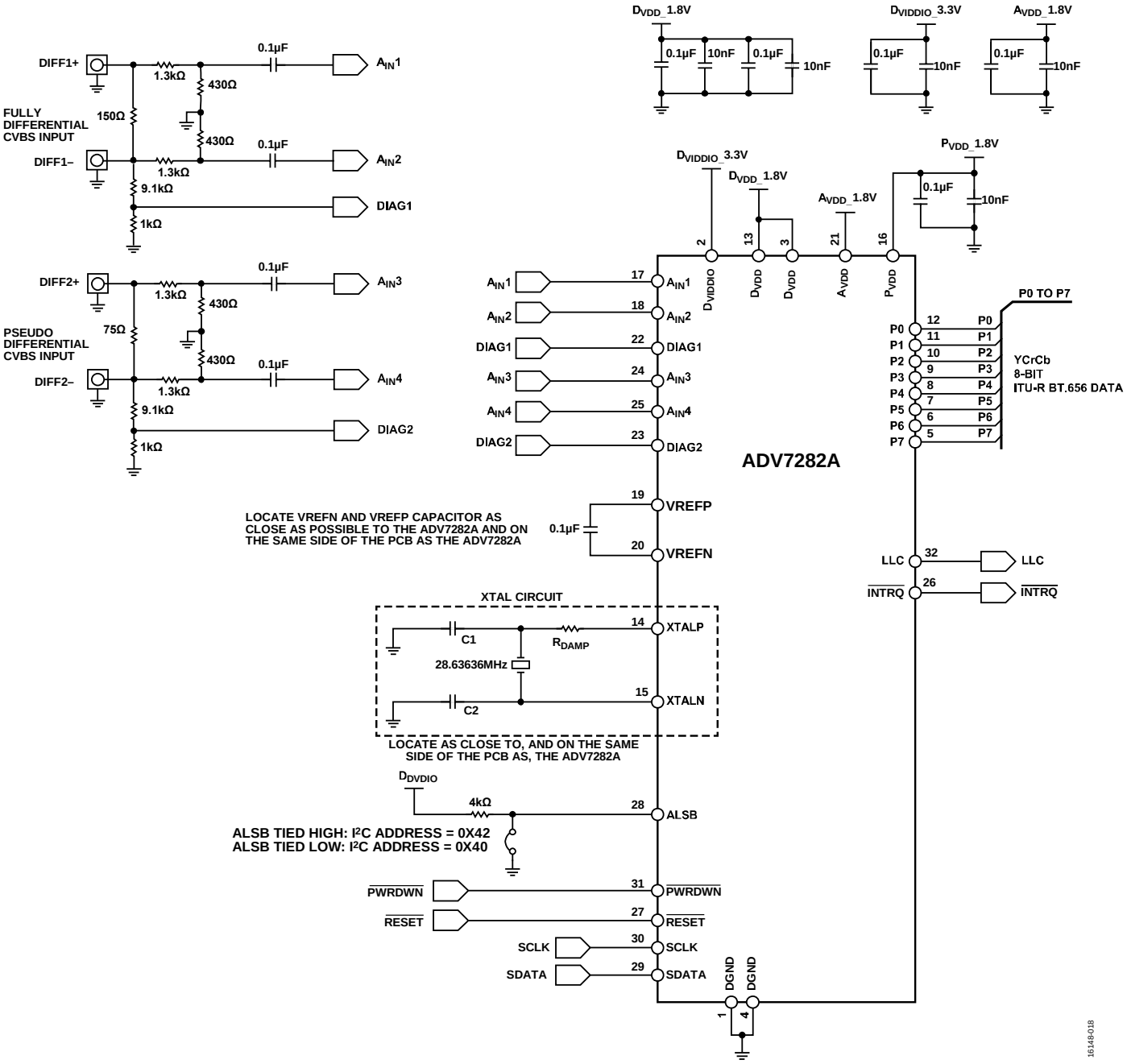

Figure 18. ADV7282A Typical Connection Diagram

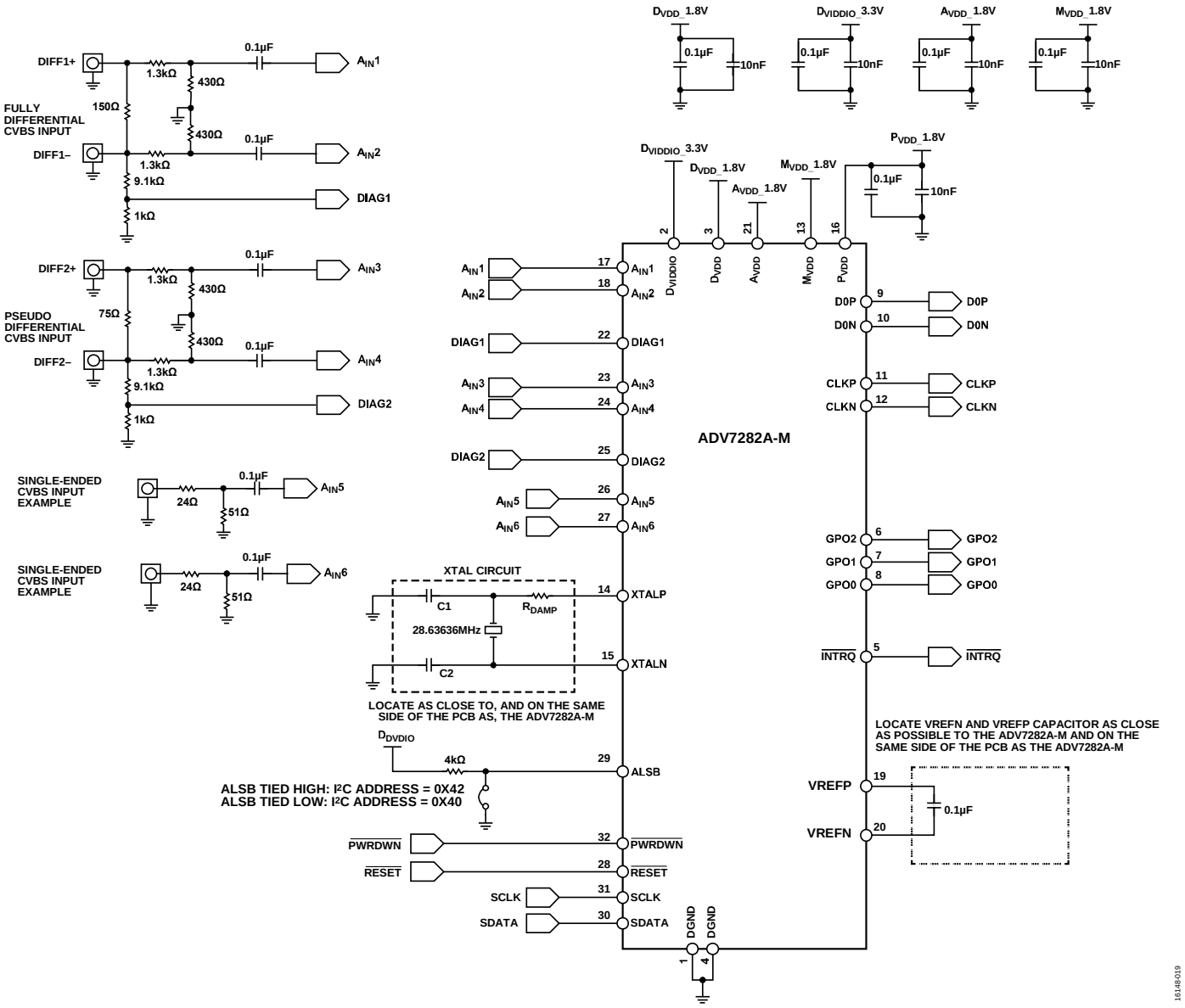

Figure 19. ADV7282A-M Typical Connection Diagram

OUTLINE DIMENSIONS

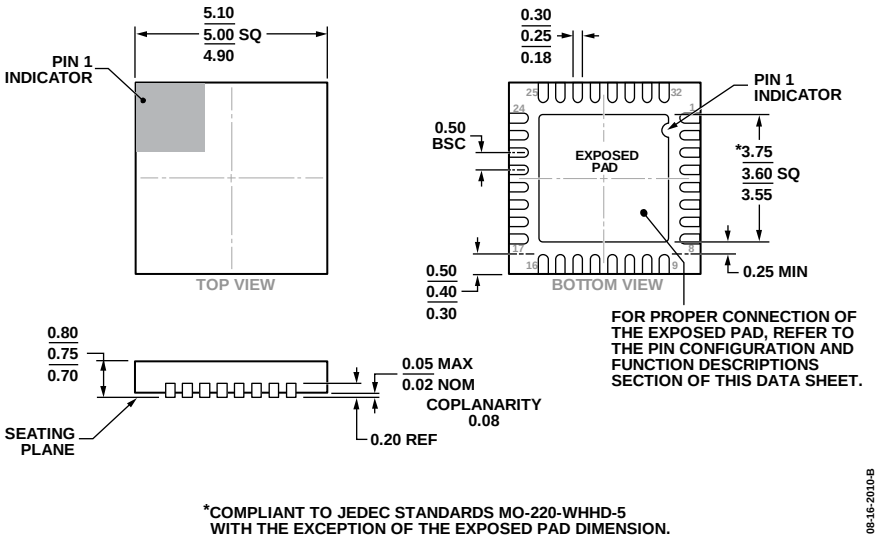

Figure 20. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADV7282AWBCPZ	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADV7282AWBCPZ-RL	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADV7282AWBCPZ-M	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADV7282AWBCPZ-M-RL	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
EVAL-ADV7282AEBZ		Evaluation Board for the ADV7282A	
EVAL-ADV7282AMEBZ		Evaluation Board for the ADV7282A-M	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADV7282AW models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).