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REVISION HISTORY

11/2016—Rev. C to Rev. D

Changes to Figure 3 and Table 7 11
Updated Outline Dimensions 19
Changes to Ordering Guide 20

9/2014—Rev. B to Rev. C

Moved Terminology Section 15
Updated Outline Dimensions 19
Changes to Ordering Guide 20

2/2009—Rev. A to Rev. B

Changes to Ordering Guide 20

7/2004—Rev. 0 to Rev. A

Updated Format ..... Universal
Added QSOP Package Outline 20
Changes to Ordering Guide 20

3/03—Rev. 0: Initial Version

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SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to+125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance (R_{ON})	45			Ω typ	V_S = ±4.5 V, I_S = 1 mA; see Figure 21
	75	90	100	Ω max	
On Resistance Match between	1.3			Ω typ	
Channels (ΔR_{ON})	3	3.2	3.5	Ω max	V_S = 3.5 V, I_S = 1 mA
On Resistance Flatness ($R_{FLAT(ON)}$)	10			Ω typ	V_{DD} = +5 V, V_{SS} = −5 V;
	16	17	18	Ω max	V_S = ±3 V, I_S = 1 mA
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source OFF Leakage I_S (OFF)	±0.005			nA typ	V_D = ±4.5 V, V_S = ∓ 4.5 V; see Figure 22
	±0.2		±5	nA max	
Drain OFF Leakage I_D (OFF)	±0.005			nA typ	V_D = ±4.5 V, V_S = ∓ 4.5 V; see Figure 23
ADG658	±0.2		±5	nA max	
ADG659	±0.1		±2.5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.005			nA typ	V_D = V_S = ±4.5 V; see Figure 24
ADG658	±0.2		±5	nA max	
ADG659	±0.1		±2.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[1]					
$t_{TRANSITION}$	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	115	140	165	ns max	V_S = 3 V; see Figure 25
t_{ON} ($\overline{EN}$)	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	115	140	165	ns max	V_S = 3 V; see Figure 27
t_{OFF} ($\overline{EN}$)	30			ns typ	R_L = 300 Ω, C_L = 35 pF
	45	50	55	ns max	V_S = 3 V; see Figure 27
Break-Before-Make Time Delay, t_{BBM}	50			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 3 V; see Figure 26
Charge Injection	2			pC typ	V_S = 0 V, R_S = 0 Ω,
	4			pC max	C_L = 1 nF; see Figure 28
Off Isolation	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Total Harmonic Distortion, THD + N	0.025			% typ	R_L = 600 Ω, 2 V p-p, f = 20 Hz to 20 kHz
Channel-to-Channel Crosstalk (ADG659)	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
−3 dB Bandwidth					
ADG658	210			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 30
ADG659	400			MHz typ	

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Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to+125°C	Unit	Test Conditions/Comments
C_S (OFF)	4			pF typ	f = 1 MHz
C_D (OFF)					
ADG658	23			pF typ	f = 1 MHz
ADG659	12			pF typ	f = 1 MHz
C_D, C_S (ON)					
ADG658	28			pF typ	f = 1 MHz
ADG659	16			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.01			µA typ	Digital Inputs = 0 V or 5.5 V
			1	µA max	
I_{SS}	0.01			µA typ	Digital Inputs = 0 V or 5.5 V
			1	µA max	

[1] Guaranteed by design; not subject to production test.

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5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance (R_{ON})	85			Ω typ	V_S = 0 V to 4.5 V, I_S = 1 mA; see Figure 21
	150	160	200	Ω max	
On Resistance Match between	4.5			Ω typ	V_S = 3.5 V, I_S = 1 mA
Channels (ΔR_{ON})	8	9	10	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	13	14	16	Ω typ	V_{DD} = 5 V, V_{SS} = 0 V, V_S = 1.5 V to 4 V, I_S = 1 mA
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.005			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 22
	±0.2		±5	nA max	
Drain OFF Leakage I_D (OFF)	±0.005			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 23
ADG658	±0.2		±5	nA max	
ADG659	±0.1		±2.5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.005			nA typ	V_S = V_D = 1 V or 4.5 V, see Figure 24
ADG658	±0.2		±5	nA max	
ADG659	±0.1		±2.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[1]					
$t_{TRANSITION}$	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	200	270	300	ns max	V_S = 3 V; see Figure 25
t_{ON} ($\overline{EN}$)	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	190	245	280	ns max	V_S = 3 V; see Figure 27
t_{OFF} ($\overline{EN}$)	35			ns typ	R_L = 300 Ω, C_L = 35 pF
	50	60	70	ns max	V_S = 3 V; see Figure 27
Break-Before-Make Time Delay, t_{BBM}	100			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 3 V; see Figure 26
Charge Injection	0.5			pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 28
	1			pC max	
Off Isolation	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; see Figure 31
(ADG659)					
−3 dB Bandwidth					
ADG658	180			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 30
ADG659	330			MHz typ	
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)					
ADG658	29			pF typ	f = 1 MHz
ADG659	15			pF typ	f = 1 MHz

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Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to +125°C	Unit	Test Conditions/Comments
C_D, C_S (ON)					
ADG658	30			pF typ	f = 1 MHz
ADG659	16			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.01			µA typ	Digital Inputs = 0 V or 5.5 V
			1	µA max	

[1] Guaranteed by design; not subject to production test.

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2.7 V TO 3.6 V SINGLE SUPPLY

V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	V_{DD} = 2.7 V, V_{SS} = 0 V
On Resistance (R_{ON})	185			Ω typ	V_S = 0 V to 2.7 V, I_S = 0.1 mA; see Figure 21
	300	350	400	Ω max	
On Resistance Match between	2			Ω typ	V_S = 1.5 V, I_S = 0.1 mA
Channels (ΔR_{ON})	4.5	6	7	Ω max	
LEAKAGE CURRENTS					V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.005			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V; see Figure 22
	±0.2		±5	nA max	
Drain OFF Leakage I_D (OFF)	±0.005			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V; see Figure 23
ADG658	±0.2		±5	nA max	
ADG659	±0.1		±2.5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.005			nA typ	V_S = V_D = 1 V or 3 V, see Figure 24
ADG658	±0.2		±5	nA max	
ADG659	±0.1		±2.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.5	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[1]					
$t_{TRANSITION}$	200			ns typ	R_L = 300 Ω, C_L = 35 pF
	370	440	490	ns max	V_S = 1.5 V; see Figure 25
t_{ON} ($\overline{EN}$)	230			ns typ	R_L = 300 Ω, C_L = 35 pF
	370	440	490	ns max	V_S = 1.5 V; see Figure 27
t_{OFF} ($\overline{EN}$)	50			ns typ	R_L = 300 Ω, C_L = 35 pF
	80	90	110	ns max	V_S = 1.5 V; see Figure 27
Break-Before-Make Time Delay, t_{BBM}	200			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 1.5 V; see Figure 26
Charge Injection	1			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 28
	2			pC max	
Off Isolation	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk (ADG659)	−90			dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; see Figure 31
−3 dB Bandwidth					
ADG658	160			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 30
ADG659	300			MHz typ	
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)					
ADG658	29			pF typ	f = 1 MHz
ADG659	15			pF typ	f = 1 MHz

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Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to +125°C	Unit	Test Conditions/Comments
C_D, C_S (ON)					
ADG658	30			pF typ	f = 1 MHz
ADG659	16			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.01			μA typ	Digital Inputs = 0 V or 3.6 V
			1	μA max	

[1] Guaranteed by design; not subject to production test.

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	13 V
V_{DD} to GND	−0.3 V to +13 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 10 mA, whichever occurs first
Peak Current, S or D	40 mA
(Pulsed at 1 ms, 10% duty cycle max)	
Continuous Current, S or D	20 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
16-Lead QSOP	104°C/W
16-Lead TSSOP	150.4°C/W
16-Lead LFCSP (4-Layer Board)	70°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	5.5 kV

[1] Over voltages at A_x, $\overline{EN}$, S, or D are clamped by internal diodes. Current must be limited to the maximum ratings.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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Table 5. ADG658 Truth Table

A2	A1	A0	$\overline{EN}$	Switch Condition
X[1]	X[1]	X[1]	1	None
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8

[1] X = Don't Care

Table 6. ADG659 Truth Table

A1	A0	$\overline{EN}$	On Switch Pair
X[1]	X[1]	1	None
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

[1] X = Don't Care

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

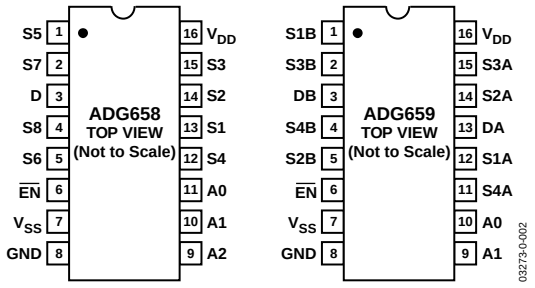
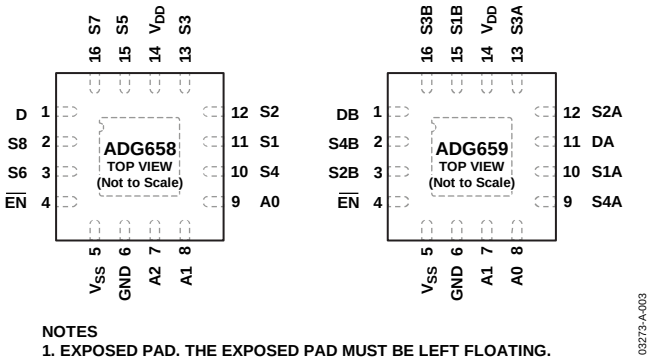


Figure 2. 16-Lead TSSOP/QSOP Pin Configuration



NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE LEFT FLOATING.

Figure 3. 16-Lead, 4 mm × 4 mm LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Parameter	Description
V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply Potential.
I_{DD}	Positive Supply Current.
I_{SS}	Negative Supply Current.
GND	Ground (0 V) Reference.
S	Source Terminal. Can be an input or output.
D	Drain Terminal. Can be an input or output.
A_X	Logic Control Input.
$\overline{EN}$	Active Low Digital Input. When high, device is disabled and all switches are OFF. When low, A_X logic inputs determine ON switch.
EPAD (LFCSP Only)	Exposed Pad. The exposed pad must be left floating.

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TYPICAL PERFORMANCE CHARACTERISTICS

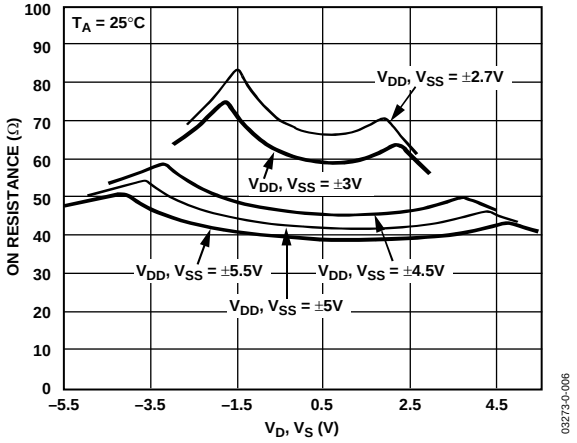

Figure 4. On Resistance vs. V_D (V_S) for Dual Supply

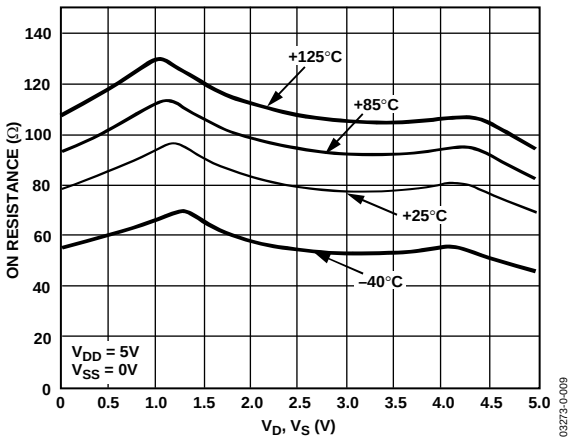

Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)

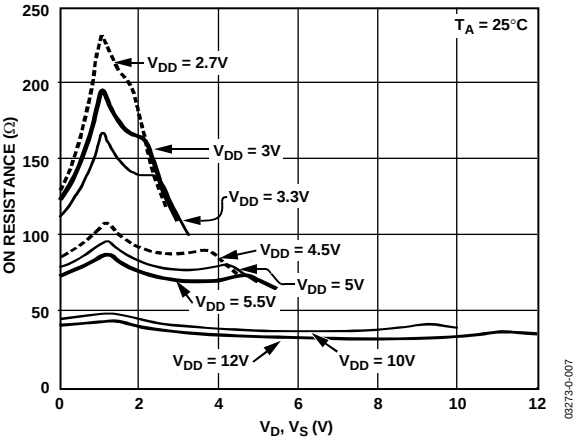

Figure 5. On Resistance vs. V_D (V_S) for Single Supply

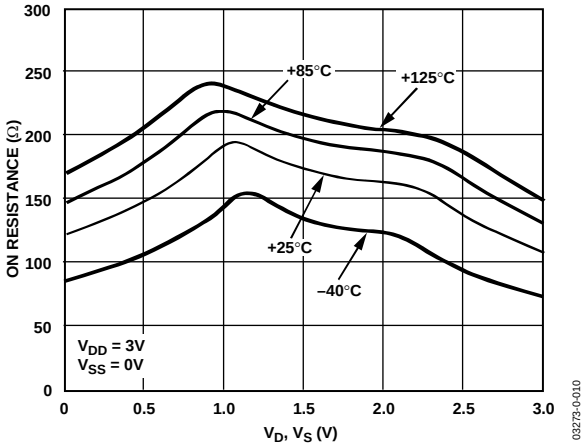

Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)

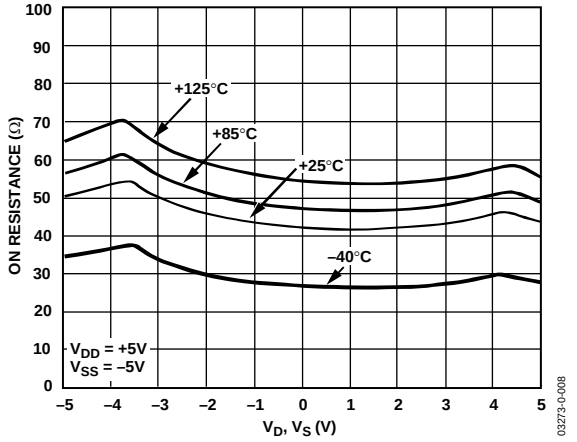

Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures (Dual Supply)

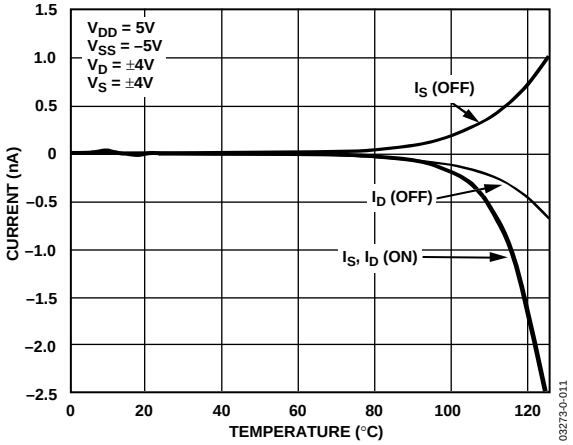

Figure 9. Leakage Current vs. Temperature (Dual Supply)

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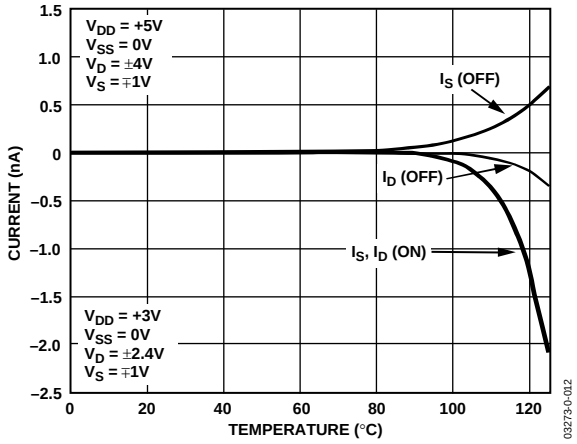

Figure 10. Leakage Current vs. Temperature (Single Supply)

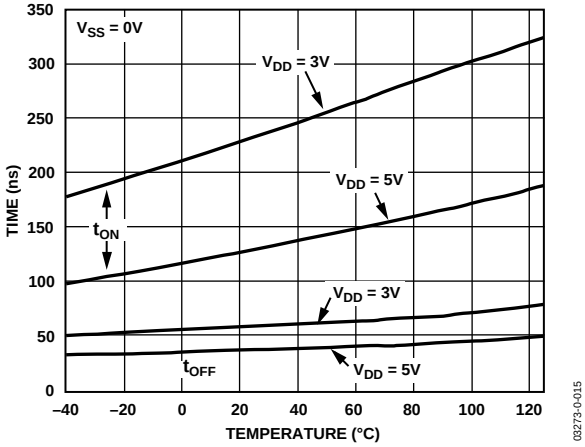

Figure 13. t_{ON}/t_{OFF} Times vs. Temperature (Single Supply)

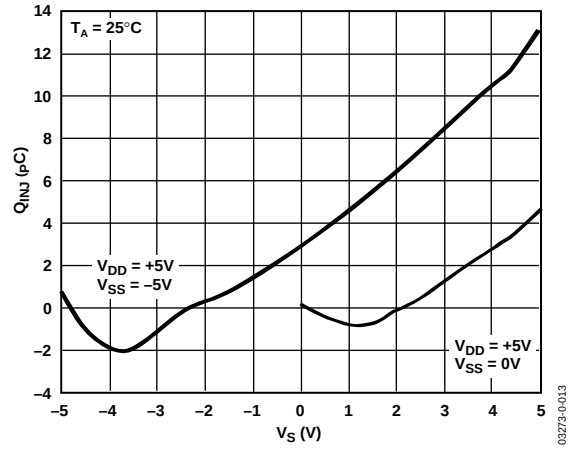

Figure 11. Charge Injection vs. Source Voltage

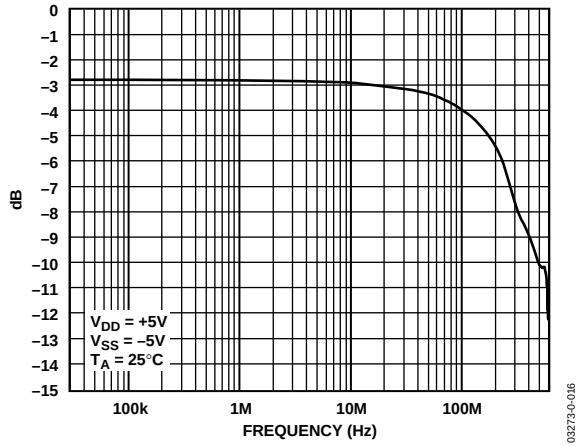

Figure 14. ON Response vs. Frequency (ADG658)

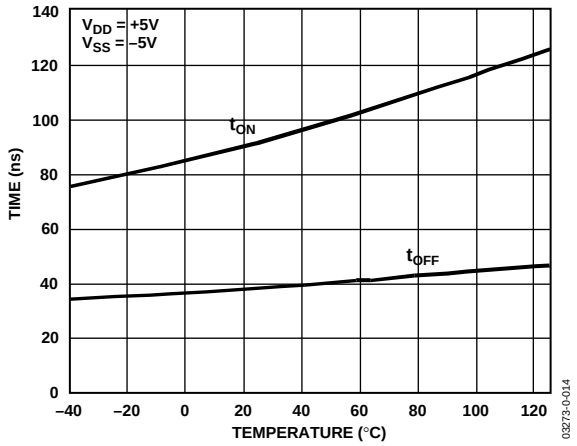

Figure 12. t_{ON}/t_{OFF} Times vs. Temperature (Dual Supply)

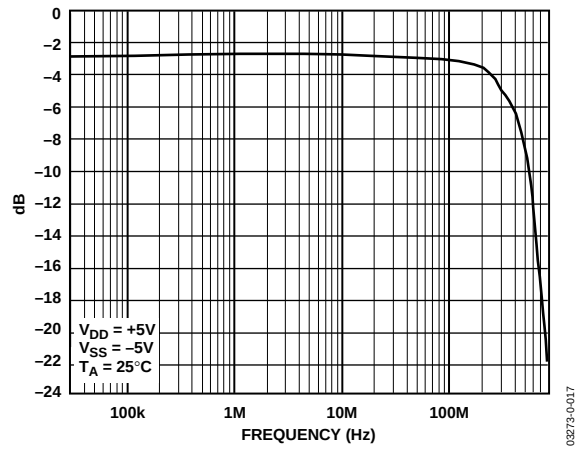

Figure 15. ON Response vs. Frequency (ADG659)

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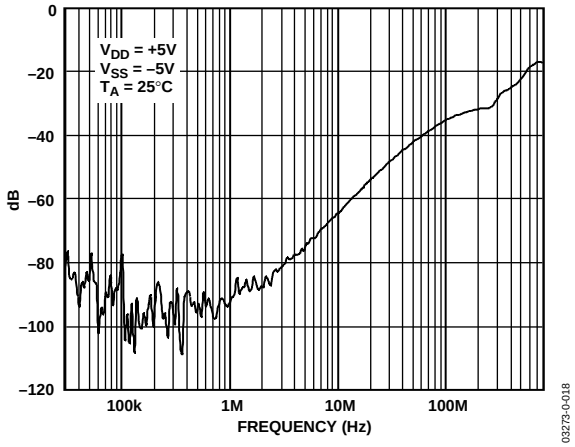

Figure 16. OFF Isolation vs. Frequency

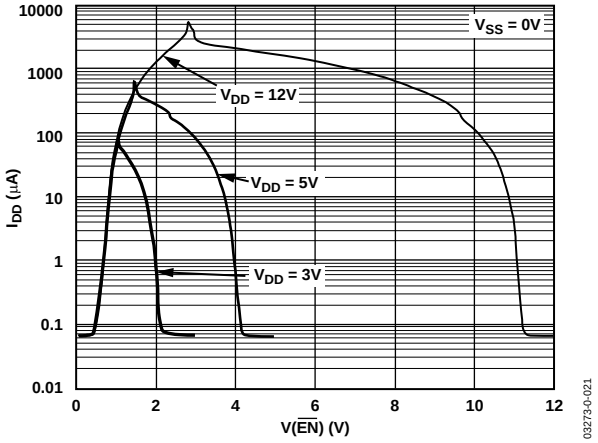

Figure 19. V_{DD} Current vs. Logic Level

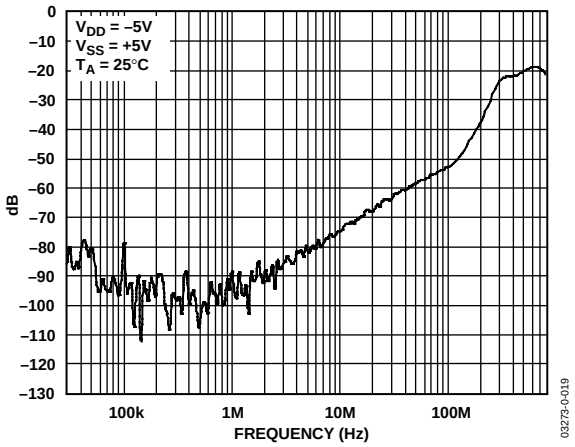

Figure 17. Crosstalk vs. Frequency

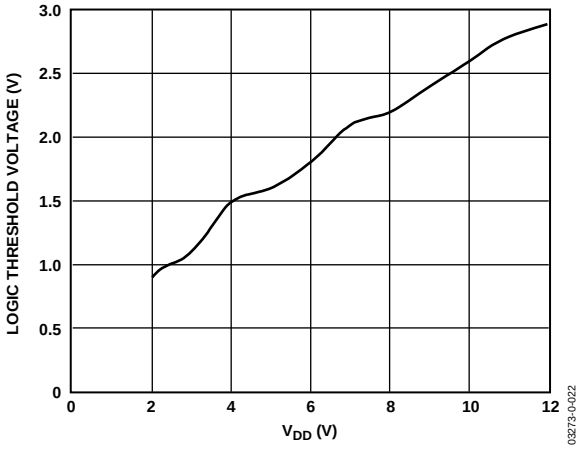

Figure 20. Logic Threshold Voltage vs. Supply Voltage

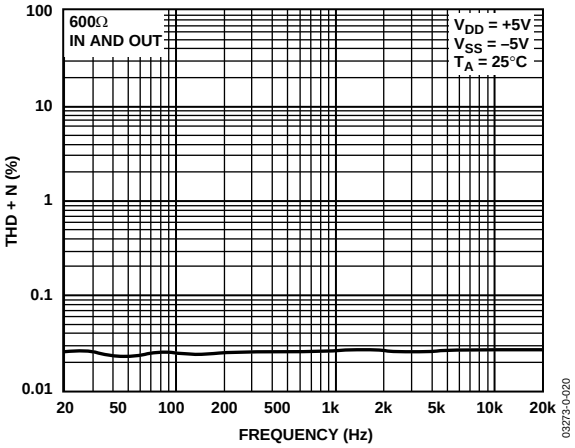

Figure 18. THD + Noise

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TERMINOLOGY

V_D (V_S)
Analog Voltage on Terminals D, S.

R_{ON}
Ohmic Resistance between D and S.

ΔR_{ON}
On Resistance Match between Any Two Channels, i.e., R_{ON}max − R_{ON}min.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of ON Resistance as measured over the specified analog signal range.

I_S (OFF)
Source Leakage Current with the Switch OFF.

I_D (OFF)
Drain Leakage Current with the Switch OFF.

I_D, I_S (ON)
Channel Leakage Current with the Switch ON.

V_{INL}
Maximum Input Voltage for Logic 0.

V_{INH}
Minimum Input Voltage for Logic 1.

I_{INL} (I_{INH})
Input Current of the Digital Input.

C_S (OFF)
OFF Switch Source Capacitance. Measured with reference to ground.

C_D (OFF)
OFF Switch Drain Capacitance. Measured with reference to ground.

C_D, C_S (ON)
ON Switch Capacitance. Measured with reference to ground.

C_{IN}
Digital Input Capacitance.

t_{ON}
Delay between Applying the Digital Control Input and the Output Switching ON. See Figure 27.

t_{OFF}
Delay between Applying the Digital Control Input and the Output Switching OFF.

t_{BBM}
ON Time. Measured between 80% points of both switches when switching from one address state to another.

Charge Injection
Measure of the Glitch Impulse Transferred from the Digital Input to the Analog Output during Switching.

Off Isolation
Measure of Unwanted Signal Coupling through an OFF Switch.

Crosstalk
Measure of Unwanted Signal Coupled through from One Channel to Another as a Result of Parasitic Capacitance.

Bandwidth
The Frequency at which the Output is Attenuated by 3 dB.

On Response
The Frequency Response of the ON Switch.

Insertion Loss
The Loss Due to the ON Resistance of the Switch.

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TEST CIRCUITS

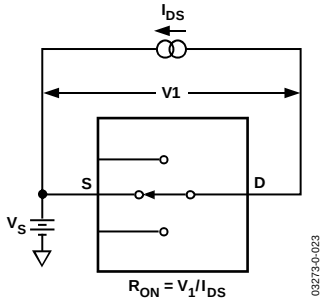


Figure 21. ON Resistance

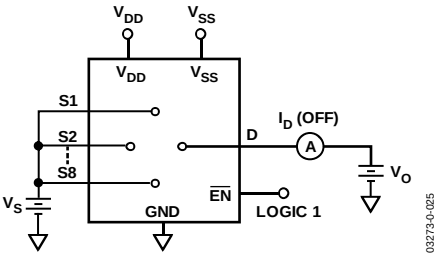


Figure 23. I_D (OFF)

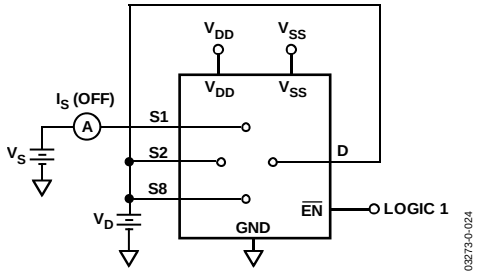


Figure 22. I_S (OFF)

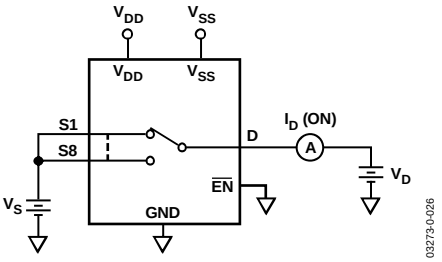
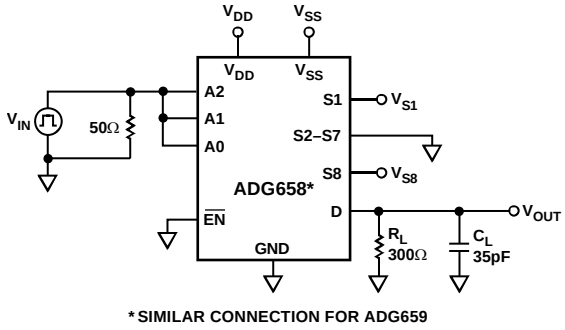


Figure 24. I_D (ON)



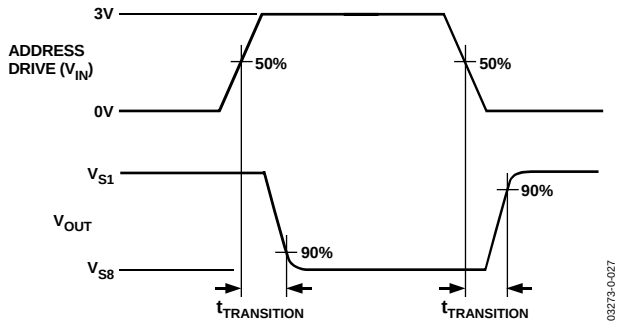
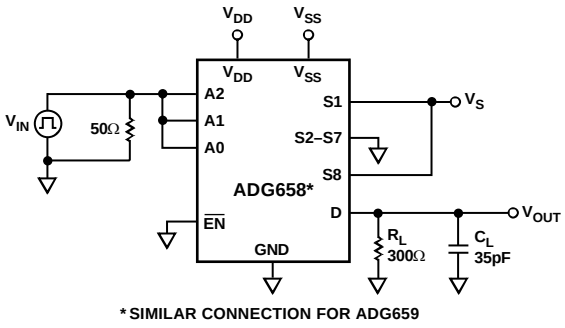


Figure 25. Switching Time of Multiplexer, $t_{TRANSITION}$



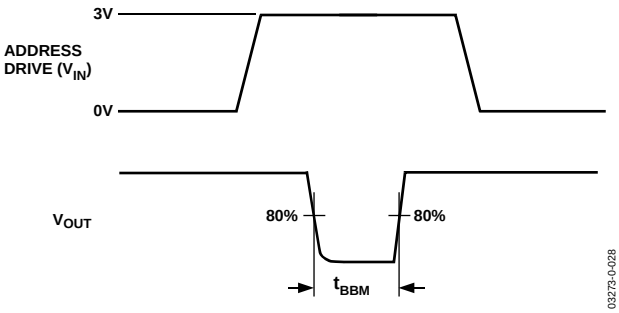


Figure 26. Break-Before-Make Delay, t_{BBM}

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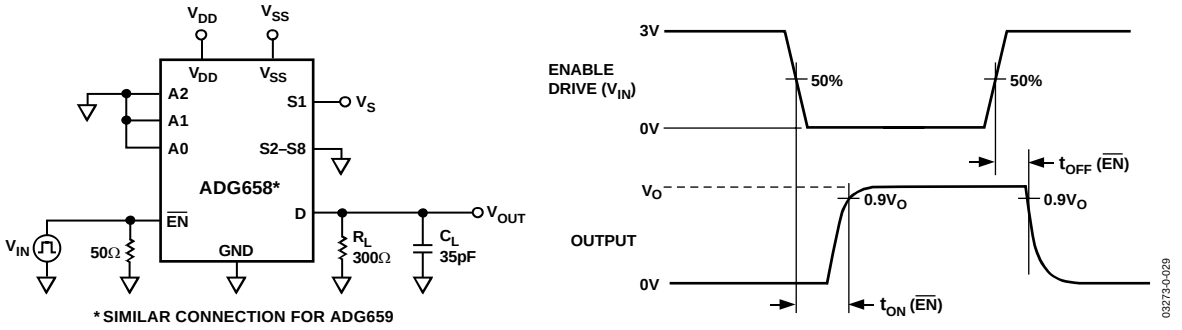

Figure 27. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)

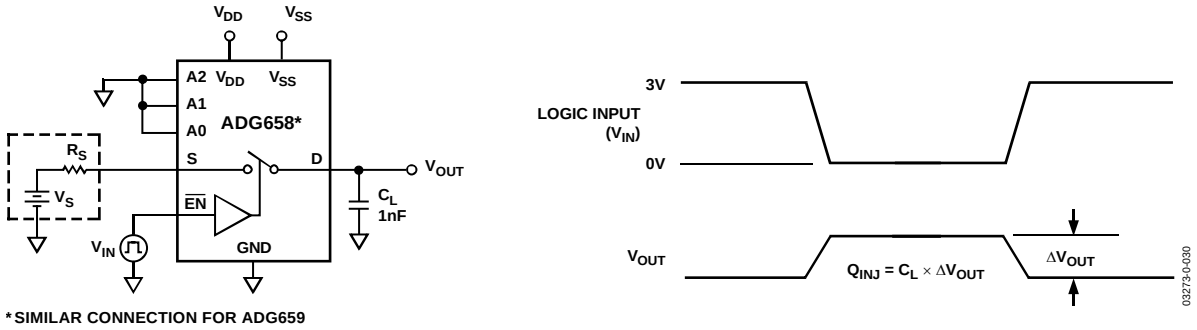

Figure 28. Charge Injection

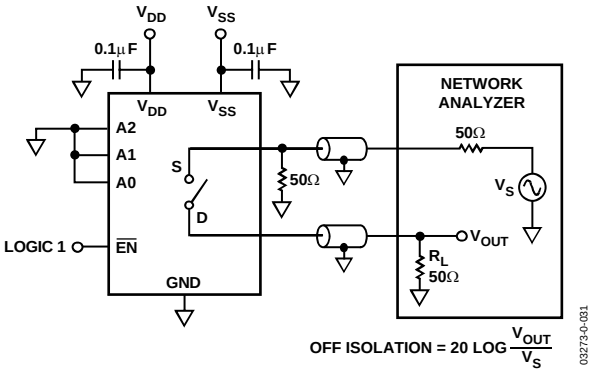

Figure 29. Off Isolation

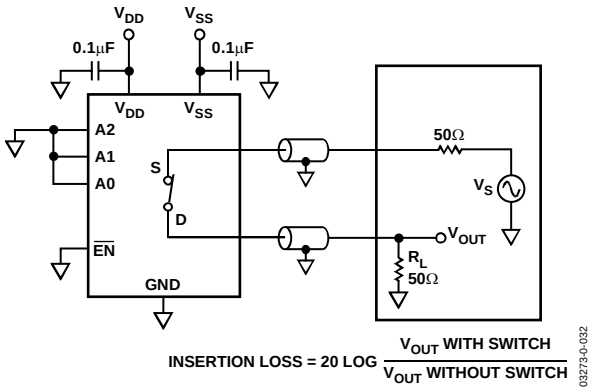

Figure 30. Bandwidth

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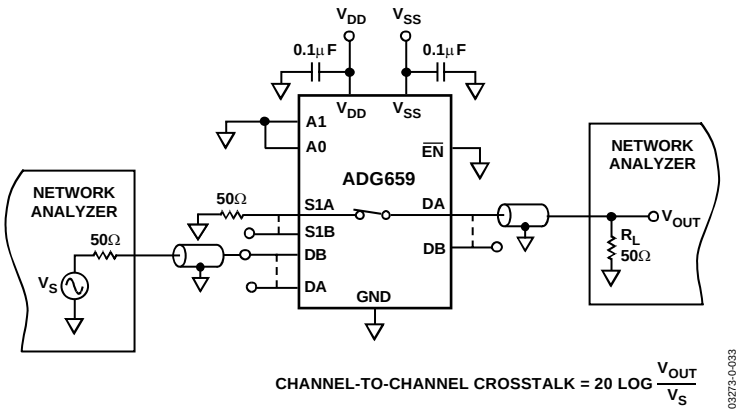

Figure 31. Channel-to-Channel Crosstalk

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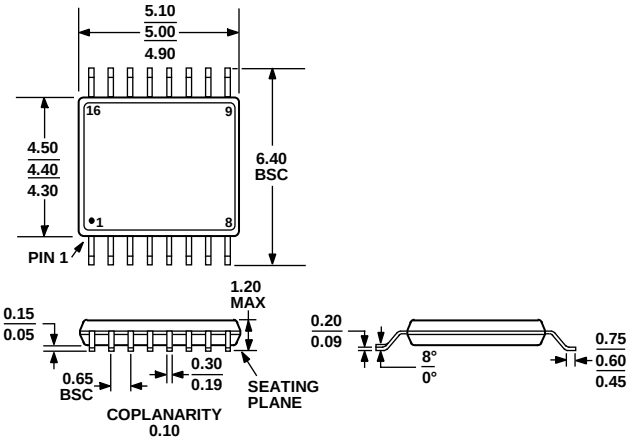
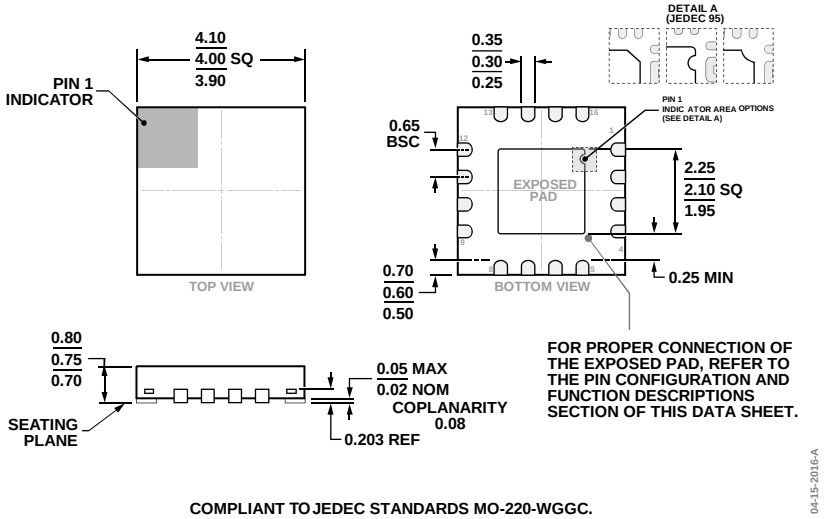
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 32. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 33. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-23)
Dimensions shown in millimeters

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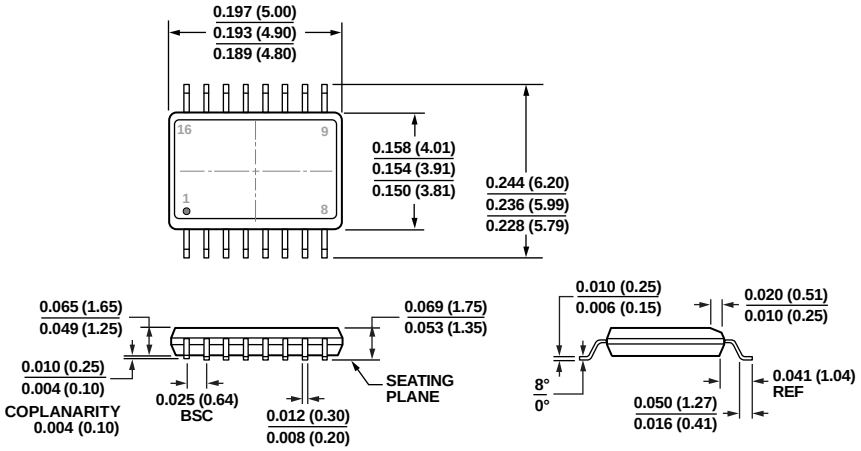

COMPLIANT TO JEDEC STANDARDS MO-137-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

09-12-2014-A

Figure 34. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADG658YRU	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG658YRU-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG658YRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG658YRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG658YCPZ	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADG658YCPZ-REEL7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADG658YRQ	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG658YRQZ	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG658YRQZ-REEL7	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADW54003-0	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADW54003-0RL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659YRU	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659YRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659YRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659WYRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659YCPZ	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADG659YCPZ-REEL7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADG659YRQZ	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADW54003 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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