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REVISION HISTORY

6/08—Rev. B to Rev. C.

Updated Format.....	Universal
ADG526A LCCC Package Removed	Universal
Changes to Features.....	1
Added Applications Section.....	1
Changes to Absolute Maximum Ratings	7
Added Table 4, Renumbered Sequentially	8
Added Table 5.....	9
Changes to Figure 7 and Figure 8.....	11
Updated Outline Dimensions	17
Changes to Ordering Guide	19

2/02—Rev. A to Rev. B.

Edits to Specifications Table, Dual Supply	2
Edits to Specifications Table, Single Supply	3
Edits to Ordering Guide	4
Removal of one Pin Configuration and Diagram	6

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 10.8 \text{ V}$ to 16.5 V , $V_{SS} = -10.8 \text{ V}$ to -16.5 V , unless otherwise noted.

Table 1.

Parameter	ADG526A/ADG527A				ADG526A		Unit	Comments
	K Version		B Version		T Version			
	25°C	−40°C to +85°C	25°C	−40°C to +85°C	25°C	−55°C to +125°C		
ANALOG SWITCH								
Analog Signal Range	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V min	
	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V max	
R _{ON}	280		280		280		Ω typ	−10 V ≤ V _S ≤ +10 V, I _{DS} = 1 mA; see Figure 15
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V _{DD} = +15 V (±10%), V _{SS} = −15 V (±10%)
					300	400	Ω max	V _{DD} = +15 V (±5%), V _{SS} = −15 V (±5%)
R _{ON} Drift	0.6		0.6		0.6		%/°C typ	−10 V ≤ V _S ≤ +10 V, I _{DS} = 1 mA
R _{ON} Match	5		5		5		% typ	−10 V ≤ V _S ≤ +10 V, I _{DS} = 1 mA
I _S (Off), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10 V, V2 = ∓10 V; see Figure 16
	1	50	1	50	1	50	nA max	
I _D (Off), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10 V, V2 = ∓10 V; see Figure 17
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100			nA max	
I _D (On), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10 V, V2 = ∓10 V; see Figure 18
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100			nA max	
I _{DIFF} , Differential Off Output Leakage (ADG527A Only)		25		25			nA max	V1 = ±10 V, V2 = ∓10 V; see Figure 19
DIGITAL CONTROL								
V _{INH} , Input High Voltage		2.4		2.4		2.4	V min	
V _{INL} , Input Low Voltage		0.8		0.8		0.8	V max	
I _{INL} or I _{INH}		1		1		1	μA max	V _{IN} = 0 to V _{DD}
C _{IN} , Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS ¹								
t _{TRANSITION}	200		200		200		ns typ	V1 = ±10 V, V2 = ∓10 V; see Figure 20
	300	400	300	400	300	400	ns max	
t _{OPEN}	50		50		50		ns typ	See Figure 21
	25	10	25	10	25	10	ns min	
t _{ON} (EN, $\overline{WR}$)	200		200		200		ns typ	See Figure 22 and Figure 23
	300	400	300	400	300	400	ns max	
t _{OFF} (EN, $\overline{RS}$)	200		200		200		ns typ	See Figure 22 and Figure 24
	300	400	300	400	300	400	ns max	
t _W , Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 13
t _S , Address Enable Setup Time		100		100		100	ns min	See Figure 13
t _H , Address Enable Hold Time		10		10		10	ns min	See Figure 13
t _{RS} , Reset Pulse Width		100		100		100	ns min	See Figure 14

ADG526A/ADG527A

Parameter	ADG526A/ADG527A				ADG526A		Unit	Comments
	K Version		B Version		T Version			
	25°C	−40°C to +85°C	25°C	−40°C to +85°C	25°C	−55°C to +125°C		
Off Isolation	68		68		68		dB typ	V _{EN} = 0.8 V, R _L = 1 kΩ, C _L = 15 pF, V _S = 7 V rms, f = 100 kHz
C _S (Off) C _D (Off)	50		50		50		dB min	V _S = 7 V rms, f = 100 kHz
	5		5		5		pF typ	V _{EN} = 0.8 V
	ADG526A	44		44		44	pF typ	V _{EN} = 0.8 V
ADG527A	22		22				pF typ	
Q _{INJ} , Charge Injection	4		4		4		pC typ	R _S = 0 Ω, V _S = 0 V; see Figure 25
POWER SUPPLY								
I _{DD}	0.6		0.6		0.6		mA typ	V _{IN} = V _{INL} or V _{INH}
		1.5		1.5		1.5	mA max	
I _{SS}	20		20		20		μA typ	V _{IN} = V _{INL} or V _{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

¹ Sample tested at 25°C to ensure compliance.

SINGLE SUPPLY

$V_{DD} = 10.8 \text{ V}$ to 16.5 V , $V_{SS} = \text{GND}$ to 0 V , unless otherwise noted.

Table 2.

Parameter	ADG526A/ADG527A				ADG526A		Unit	Comments
	K Version		B Version		T Version			
	25°C	−40°C to +85°C	25°C	−40°C to +85°C	25°C	−55°C to +125°C		
ANALOG SWITCH								
Analog Signal Range	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V min	0 V ≤ V _S ≤ 10 V, I _{DS} = 0.5 mA; see Figure 15
R _{ON}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V max	
R _{ON}	500		500		500		Ω typ	
R _{ON} Drift	700	1000	700	1000	700	1000	Ω max	0 V ≤ V _S ≤ 10 V, I _{DS} = 0.5 mA
R _{ON} Match	0.6		0.6		0.6		%/°C typ	
I _S (Off), Off Input Leakage	5		5		5		% typ	
I _S (Off), Off Input Leakage	0.02		0.02		0.02		nA typ	0 V ≤ V _S ≤ 10 V, I _{DS} = 0.5 mA
I _D (Off), Off Output Leakage	1	50	1	50	1	50	nA max	
ADG526A	0.04		0.04		0.04		nA typ	
ADG527A	1	200	1	200	1	200	nA max	V1 = 10 V/0 V, V2 = 0 V/10 V; see Figure 17
I _D (On), On Channel Leakage	1	100	1	100			nA max	
ADG526A	0.04		0.04		0.04		nA typ	
ADG527A	1	200	1	200	1	200	nA max	V1 = 10 V/0 V, V2 = 0 V/10 V; see Figure 18
I _{DIFF} , Differential Off Output Leakage (ADG527A Only)	1	100	1	100			nA max	
		25		25			nA max	
DIGITAL CONTROL								
V _{INH} , Input High Voltage		2.4		2.4		2.4	V min	V _{IN} = 0 to V _{DD}
V _{INL} , Input Low Voltage		0.8		0.8		0.8	V max	
I _{INL} or I _{INH}		1		1		1	μA max	
C _{IN} , Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS ¹								
t _{TRANSITION}	300		300		300		ns typ	V1 = 10 V/0 V, V2 = 0 V/10 V; see Figure 20
t _{OPEN}	450	600	450	600	450	600	ns max	
t _{ON} (EN, $\overline{WR}$)	50		50		50		ns typ	
t _{OFF} (EN, $\overline{RS}$)	25	10	25	10	25	10	ns min	See Figure 21
t _W Write Pulse Width	250		250		250		ns typ	
t _S Address Enable Setup Time	450	600	450	600	450	600	ns max	
t _H Address Enable Hold Time	250		250		250		ns typ	See Figure 22 and Figure 23
t _{RS} Reset Pulse Width	450	600	450	600	450	600	ns max	
Off Isolation	100	120	100	120	100	130	ns min	
		100		100		100	ns min	See Figure 13
		10		10		10	ns min	
		100		100		100	ns min	
	68		68		68		dB typ	See Figure 14
	50		50		50		dB min	

ADG526A/ADG527A

Parameter	ADG526A/ADG527A				ADG526A		Unit	Comments
	K Version		B Version		T Version			
	25°C	−40°C to +85°C	25°C	−40°C to +85°C	25°C	−55°C to +125°C		
C _S (Off)	5		5		5		pF typ	V _{EN} = 0.8 V
C _D (Off)								
ADG526A	44		44		44		pF typ	V _{EN} = 0.8 V
ADG527A	22		22				pF typ	
Q _{INJ} , Charge Injection	4		4		4		pC typ	R _S = 0 Ω, V _S = 0 V; see Figure 25
POWER SUPPLY								
I _{DD}	0.6		0.6		0.6		mA typ	V _{IN} = V _{INL} or V _{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	11		11		11		mW typ	
		25		25		25	mW max	

¹ Sample tested at 25°C to ensure compliance.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_{DD} to GND	25 V
V_{SS} to GND	-25 V
Analog Inputs ¹	
Voltage at Sx or Dx Pins	$V_{SS} - 2\text{ V}$ to $V_{DD} + 2\text{ V}$ or 20 mA, whichever occurs first
Continuous Current, Sx or Dx Pins	20 mA
Pulsed Current, Sx or Dx Pins 1 ms Duration, 10% Duty Cycle	40 mA
Digital Inputs ¹	
Voltage at A, EN, $\overline{WR}$, $\overline{RS}$	$V_{SS} - 4\text{ V}$ to $V_{DD} + 4\text{ V}$ or 20 mA, whichever occurs first
Power Dissipation (Any Package)	
Up to 75°C	470 mW
Derates Above 75°C	6 mW/ $^\circ\text{C}$
Operating Temperature Range	
Commercial (K Version)	-40°C to $+85^\circ\text{C}$
Industrial (B Version)	-40°C to $+85^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C

¹ Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, Sx, or Dx pins are clamped by diodes. Limit current to the maximum rating in Table 3.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG526A/ADG527A

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

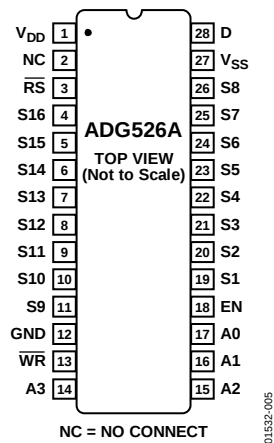


Figure 3. ADG526A PDIP, SOIC, and CERDIP Pin Configuration

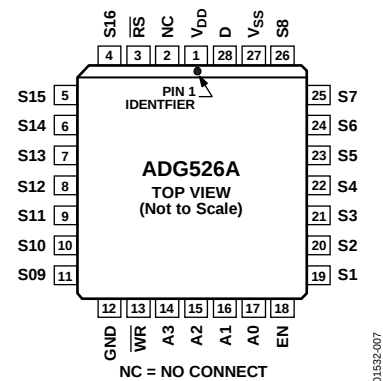


Figure 4. ADG526A PLCC Pin Configuration

Table 4. ADG526A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD}	Most Positive Power Supply Potential.
2	NC	No Connect.
3	$\overline{RS}$	Reset. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off).
4	S16	Source Terminal. This pin can be an input or output.
5	S15	Source Terminal. This pin can be an input or output.
6	S14	Source Terminal. This pin can be an input or output.
7	S13	Source Terminal. This pin can be an input or output.
8	S12	Source Terminal. This pin can be an input or output.
9	S11	Source Terminal. This pin can be an input or output.
10	S10	Source Terminal. This pin can be an input or output.
11	S9	Source Terminal. This pin can be an input or output.
12	GND	Ground (0 V) Reference.
13	$\overline{WR}$	Write. The $\overline{WR}$ signal latches the state of the address control lines and the enable line.
14	A3	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
15	A2	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
16	A1	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
17	A0	Logic control inputs. Selects which source terminal is connected to the drain (D).
18	EN	Enable. Active high logic control input.
19	S1	Source Terminal. This pin can be an input or output.
20	S2	Source Terminal. This pin can be an input or output.
21	S3	Source Terminal. This pin can be an input or output.
22	S4	Source Terminal. This pin can be an input or output.
23	S5	Source Terminal. This pin can be an input or output.
24	S6	Source Terminal. This pin can be an input or output.
25	S7	Source Terminal. This pin can be an input or output.
26	S8	Source Terminal. This pin can be an input or output.
27	V _{SS}	Most Negative Power Supply Potential.
28	D	Drain Terminal. This pin can be an input or output.

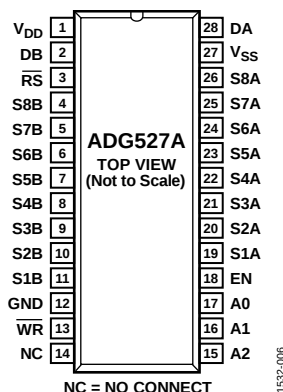


Figure 5. ADG527A PDIP, SOIC Pin Configuration

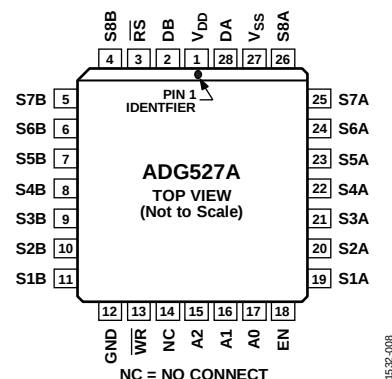


Figure 6. ADG527A PLCC Pin Configuration

Table 5. ADG527A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD}	Most Positive Power Supply Potential.
2	DB	Drain Terminal. This pin can be an input or output.
3	$\overline{RS}$	Reset. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off).
4	S8B	Source Terminal. This pin can be an input or output.
5	S7B	Source Terminal. This pin can be an input or output.
6	S6B	Source Terminal. This pin can be an input or output.
7	S5B	Source Terminal. This pin can be an input or output.
8	S4B	Source Terminal. This pin can be an input or output.
9	S3B	Source Terminal. This pin can be an input or output.
10	S2B	Source Terminal. This pin can be an input or output.
11	S1B	Source Terminal. This pin can be an input or output.
12	GND	Ground (0 V) Reference.
13	$\overline{WR}$	Write. The $\overline{WR}$ signal latches the state of the address control lines and the enable line.
14	NC	No Connect.
15	A2	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
16	A1	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
17	A0	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
18	EN	Enable. Active high logic control input.
19	S1A	Source Terminal. This pin can be an input or output.
20	S2A	Source Terminal. This pin can be an input or output.
21	S3A	Source Terminal. This pin can be an input or output.
22	S4A	Source Terminal. This pin can be an input or output.
23	S5A	Source Terminal. This pin can be an input or output.
24	S6A	Source Terminal. This pin can be an input or output.
25	S7A	Source Terminal. This pin can be an input or output.
26	S8A	Source Terminal. This pin can be an input or output.
27	V _{SS}	Most Negative Power Supply Potential.
28	DA	Drain Terminal. This pin can be an input or output.

ADG526A/ADG527A

Table 6. ADG526A Truth Table¹

A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	X	$\overline{1}$	1	Retains previous switch condition
X	X	X	X	X	X	0	None (address and enable latches cleared)
X	X	X	X	0	0	1	None
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

¹ X = don't care.

Table 7. ADG527A Truth Table¹

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	$\overline{1}$	1	Retains previous switch condition
X	X	X	X	X	0	None (address and enable latches cleared)
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

¹ X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5 V.

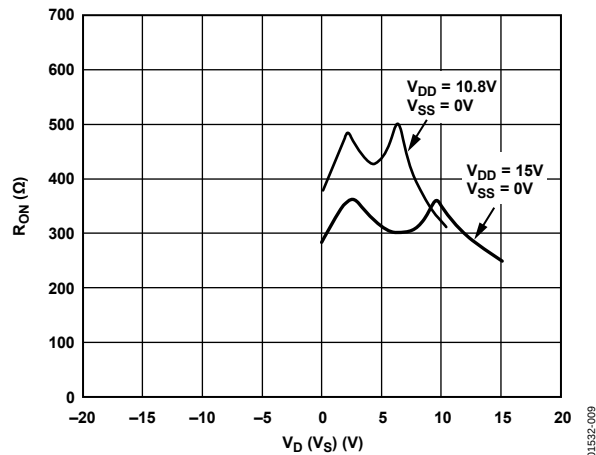


Figure 7. R_{ON} as a Function of V_D (V_S): Single-Supply Voltage, $T_A = 25^\circ\text{C}$

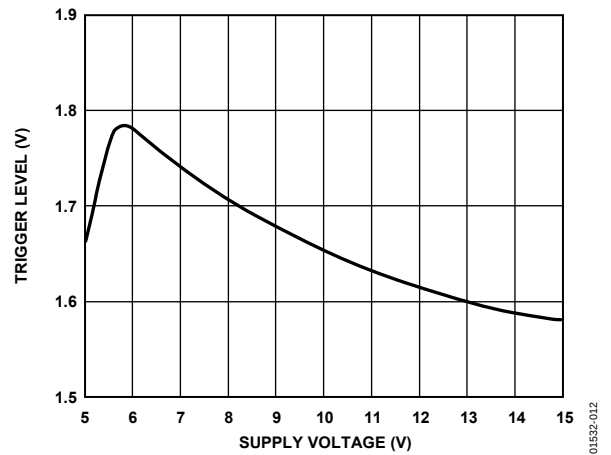


Figure 10. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, $T_A = 25^\circ\text{C}$

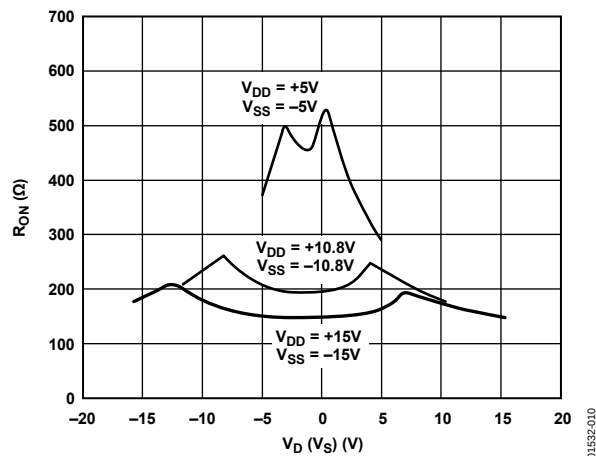


Figure 8. R_{ON} as a Function of V_D (V_S): Dual-Supply Voltage, $T_A = 25^\circ\text{C}$

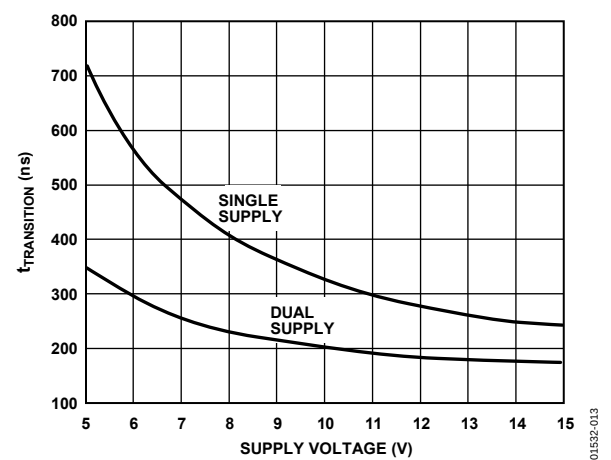


Figure 11. $t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, $T_A = 25^\circ\text{C}$
(Note: For V_{DD} and $V_{SS} < 10\text{ V}$; $V_1 = V_{DD}/V_{SS}$, $V_2 = V_{SS}/V_{DD}$; See Figure 20)

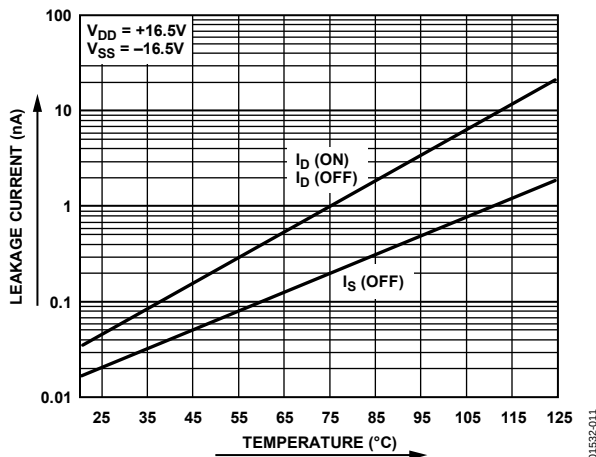


Figure 9. Leakage Current as a Function of Temperature (Leakage Currents Reduce as the Supply Voltages Reduce)

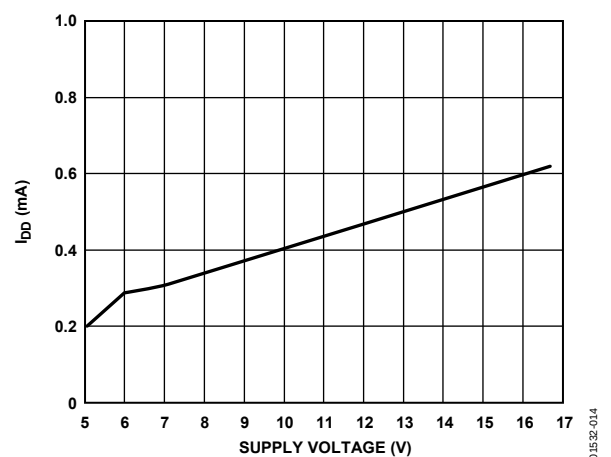


Figure 12. I_{DD} vs. Supply Voltage: Dual or Single Supply, $T_A = 25^\circ\text{C}$

TERMINOLOGY

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

R_{ON} Match

Difference between the R_{ON} of any two channels.

R_{ON} Drift

Change in R_{ON} vs. temperature.

I_S (Off)

Source terminal leakage current when the switch is off.

I_D (Off)

Drain terminal leakage current when the switch is off.

I_D (On)

Leakage current that flows from the closed switch into the body.

V_S (V_D)

Analog voltage on Terminal S or Terminal D.

C_S (Off)

Channel input capacitance for off condition.

C_D (Off)

Channel output capacitance for off condition.

C_{IN}

Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)

Delay time between the 50% and 10% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and switch on condition when switching from one address state to another.

t_{OPEN}

Off time measured between 50% points of both switches when switching from one address state to another.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

V_{DD}

Most positive voltage supply.

V_{SS}

Most negative voltage supply.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

TIMING

Figure 13 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{\text{WR}}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{\text{WR}}$.

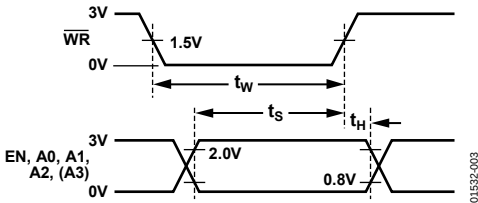


Figure 13. Timing Sequence

Figure 14 shows the reset pulse width, t_{RS} , and reset turn-off time, $t_{OFF}(\overline{\text{RS}})$.

Note that all digital input signal rise and fall times are measured from 10% to 90% of 3 V, $t_R = t_F = 20$ ns.

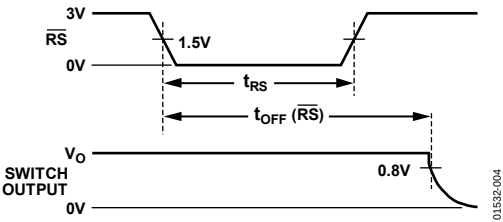


Figure 14. Reset Pulse

TEST CIRCUITS

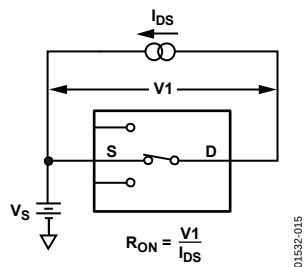


Figure 15. R_{ON}

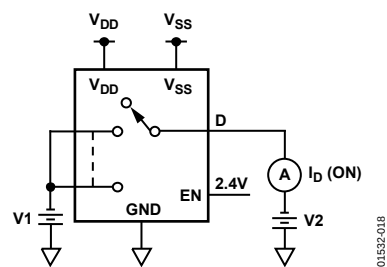


Figure 18. I_D (On)

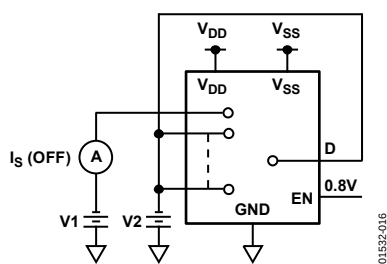


Figure 16. I_S (Off)

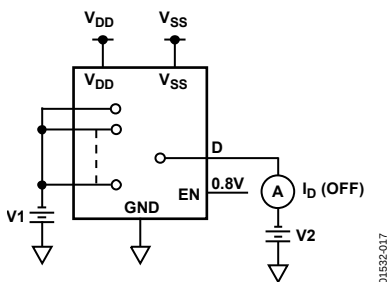


Figure 17. I_D (Off)

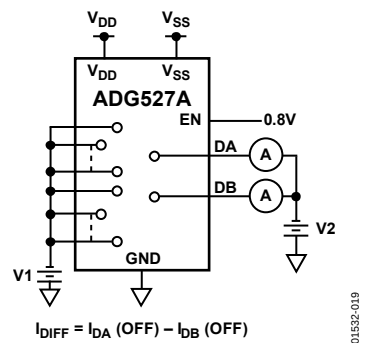
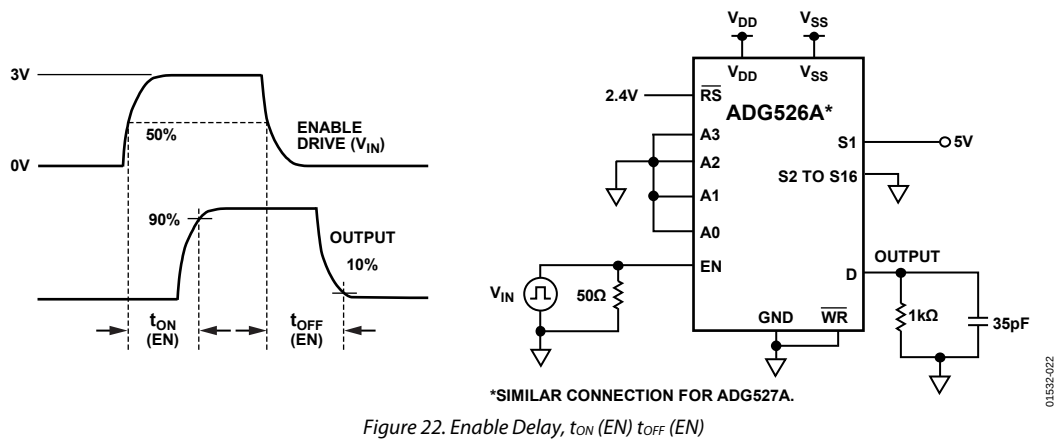
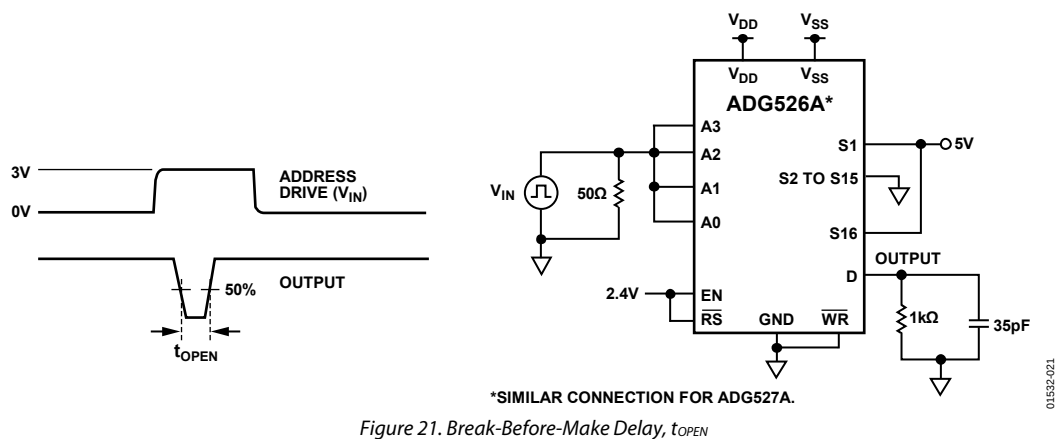
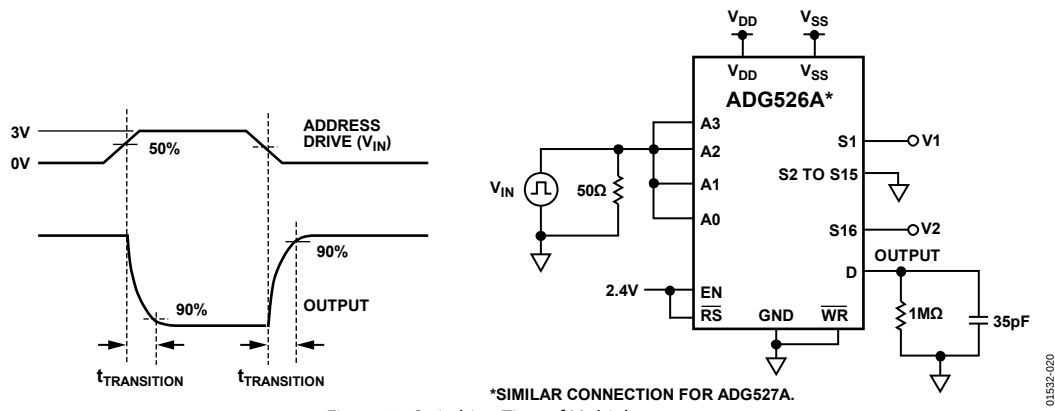


Figure 19. I_{DIFF}



ADG526A/ADG527A

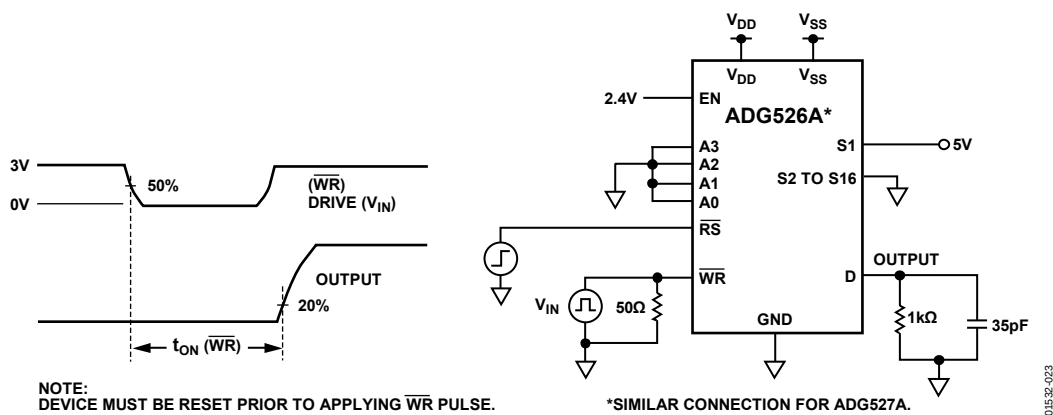


Figure 23. Write Turn-On Time, $t_{ON}(\overline{WR})$

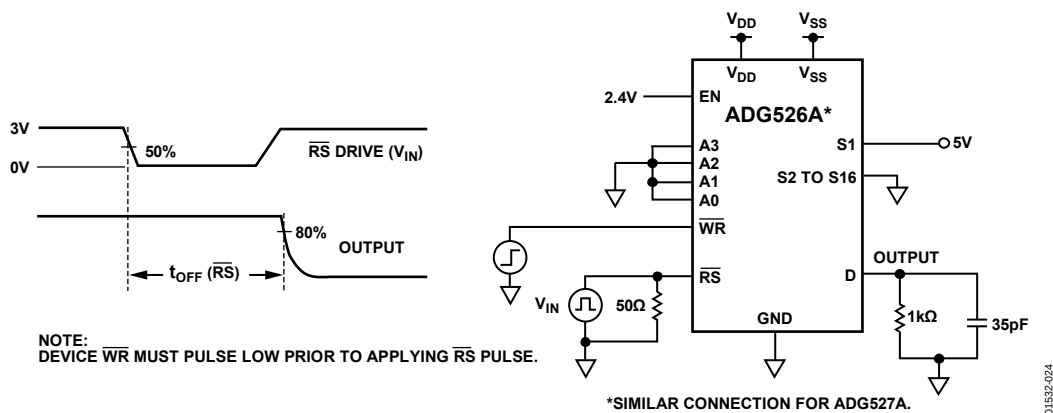


Figure 24. Reset Turn-Off, $t_{OFF}(\overline{RS})$

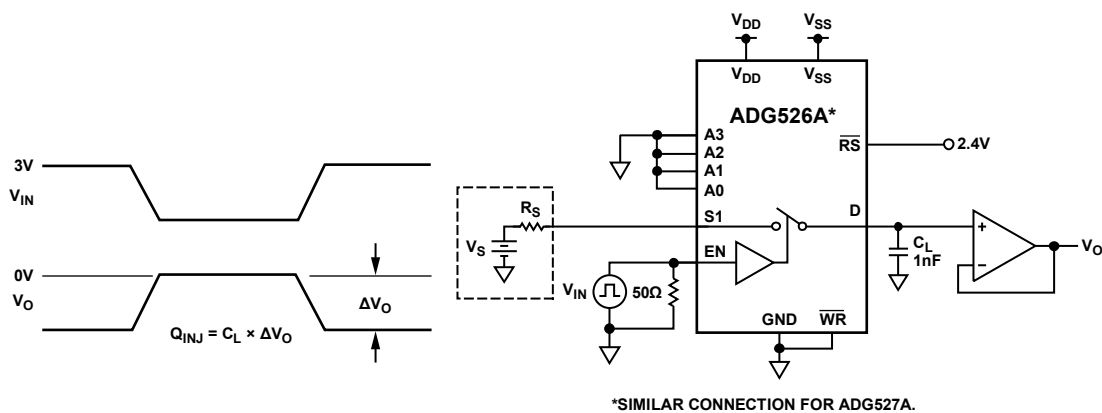
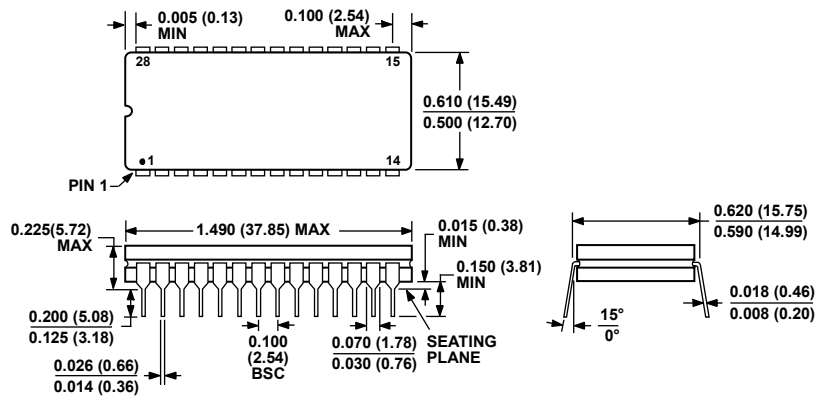


Figure 25. Charge Injection

OUTLINE DIMENSIONS

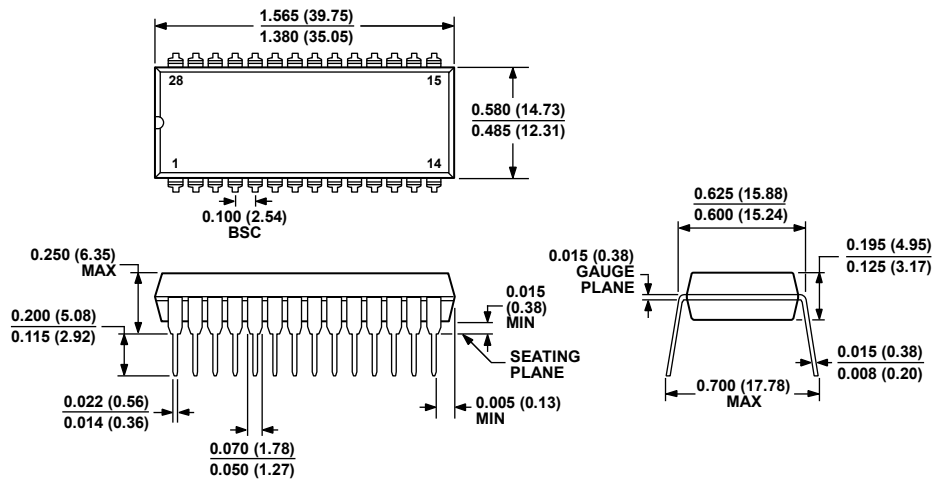


CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 28-Lead Ceramic Dual In-Line Package [CERDIP] (Q-28)

Dimensions shown in inches and (millimeters)

030106-A



COMPLIANT TO JEDEC STANDARDS MS-011

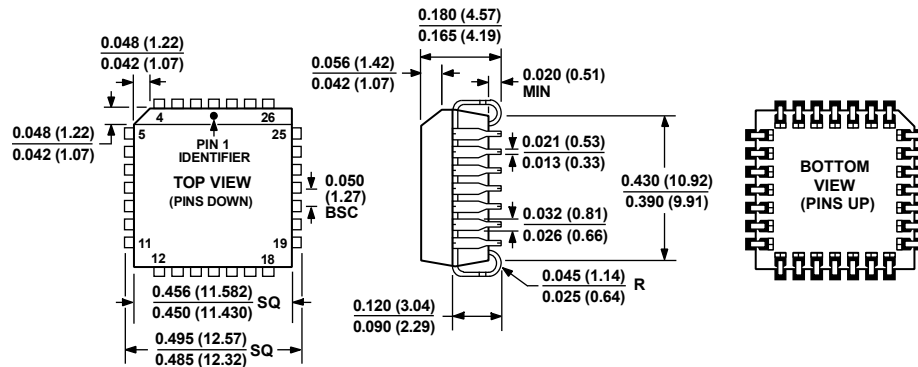
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE LEADS.

Figure 27. 28-Lead Plastic Dual In-Line Package [PDIP] (N-28)

Dimensions shown in inches and (millimeters)

071005-A

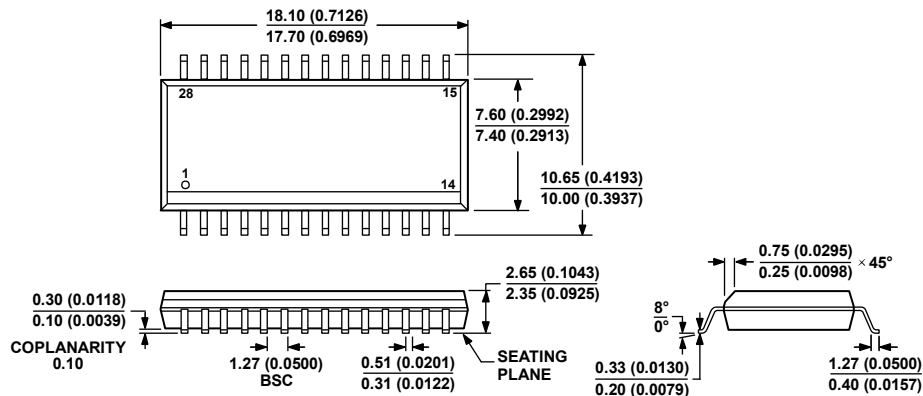
ADG526A/ADG527A



COMPLIANT TO JEDEC STANDARDS MO-047-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 28-Lead Plastic Leaded Chip Carrier [PLCC]
(P-28A)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 29. 28-Lead Standard Small Outline Package [SOIC] Wide Body
(RW-28)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG526AKN	–40°C to +85°C	28-Lead PDIP	N-28
ADG526AKNZ ¹	–40°C to +85°C	28-Lead PDIP	N-28
ADG526AKR	–40°C to +85°C	28-Lead SOIC	RW-28
ADG526AKR-REEL	–40°C to +85°C	28-Lead SOIC	RW-28
ADG526AKRZ ¹	–40°C to +85°C	28-Lead SOIC	RW-28
ADG526AKRZ-REEL ¹	–40°C to +85°C	28-Lead SOIC	RW-28
ADG526AKP	–40°C to +85°C	28-Lead PLCC	P-28A
ADG526AKP-REEL	–40°C to +85°C	28-Lead PLCC	P-28A
ADG526AKPZ ¹	–40°C to +85°C	28-Lead PLCC	P-28A
ADG526AKPZ-REEL ¹	–40°C to +85°C	28-Lead PLCC	P-28A
ADG526ATQ	–55°C to +125°C	28-Lead CERDIP	Q-28
ADG526ABQ	–40°C to +85°C	28-Lead CERDIP	Q-28
ADG526ATCHIPS			DIE
ADG527AKN	–40°C to +85°C	28-Lead PDIP	N-28
ADG527AKNZ ¹	–40°C to +85°C	28-Lead PDIP	N-28
ADG527AKR	–40°C to +85°C	28-Lead SOIC	RW-28
ADG527AKR-REEL	–40°C to +85°C	28-Lead SOIC	RW-28
ADG527AKRZ ¹	–40°C to +85°C	28-Lead SOIC	RW-28
ADG527AKP	–40°C to +85°C	28-Lead PLCC	P-28A
ADG527AKPZ ¹	–40°C to +85°C	28-Lead PLCC	P-28A

¹ Z = RoHS Compliant Part, # denotes RoHS complaint product, may be top or bottom marked.

NOTES