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## REVISION HISTORY

### 2/2017—Rev. A to Rev. B

|                                      |   |
|--------------------------------------|---|
| Changes to Figure 4 and Table 4..... | 6 |
| Changes to Figure 5 and Table 5..... | 7 |
| Changes to Figure 6 and Table 6..... | 8 |

### 8/2016—Rev. 0 to Rev. A

|                                      |            |
|--------------------------------------|------------|
| Changed CP-16-3 to CP-16-27 .....    | Throughout |
| Changes to Figure 4 and Table 4..... | 6          |
| Changes to Figure 5 and Table 5..... | 7          |
| Changes to Figure 6 and Table 6..... | 8          |
| Updated Outline Dimensions.....      | 15         |
| Changes to Ordering Guide .....      | 15         |

### 8/2007—Revision 0: Initial Version

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

Typical (Typ) values are given for  $V_{CC} - V_{EE} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted. Minimum (Min) and maximum (Max) values are given over the full  $V_{CC} - V_{EE} = 3.3\text{ V} \pm 10\%$  and  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  variation, unless otherwise noted.

Table 1.

| Parameter                                             | Symbol    | Min             | Typ                | Max             | Unit   | Test Conditions/Comments                                                                                                                      |
|-------------------------------------------------------|-----------|-----------------|--------------------|-----------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| DC INPUT CHARACTERISTICS                              |           |                 |                    |                 |        |                                                                                                                                               |
| Input Voltage High Level                              | $V_{IH}$  | $V_{EE} + 1.6$  |                    | $V_{CC}$        | V      | −40°C to +85°C<br>(±1.7 V between input pins)<br>85°C to 125°C<br>(±1.4 V between input pins)                                                 |
| Input Voltage Low Level                               | $V_{IL}$  | $V_{EE}$        |                    | $V_{CC} - 0.7$  | V      |                                                                                                                                               |
| Input Differential Range                              | $V_{ID}$  | 0.2             |                    | 3.4             | V p-p  |                                                                                                                                               |
|                                                       | $V_{ID}$  | 0.2             |                    | 2.8             | V p-p  |                                                                                                                                               |
|                                                       | $C_{IN}$  |                 | 0.4                |                 | pF     |                                                                                                                                               |
| Input Capacitance                                     |           |                 | 0.4                |                 | pF     | Open $V_T$                                                                                                                                    |
| Input Resistance, Single-Ended Mode                   |           |                 | 50                 |                 | Ω      |                                                                                                                                               |
| Input Resistance, Differential Mode                   |           |                 | 100                |                 | Ω      |                                                                                                                                               |
| Input Resistance, Common Mode                         |           |                 | 50                 |                 | kΩ     |                                                                                                                                               |
| Input Bias Current                                    |           |                 | 20                 |                 | μA     |                                                                                                                                               |
| DC OUTPUT CHARACTERISTICS                             |           |                 |                    |                 |        |                                                                                                                                               |
| Output Voltage High Level                             | $V_{OH}$  | $V_{CC} - 1.26$ |                    | $V_{CC} - 0.76$ | V      | 50 Ω to ( $V_{CC} - 2.0$ V)                                                                                                                   |
| Output Voltage Low Level                              | $V_{OL}$  | $V_{CC} - 1.99$ |                    | $V_{CC} - 1.54$ | V      | 50 Ω to ( $V_{CC} - 2.0$ V)                                                                                                                   |
| Output Voltage Differential                           | $V_{OD}$  | 610             |                    | 1040            | mV     | 50 Ω to ( $V_{CC} - 2.0$ V)                                                                                                                   |
| Reference Voltage                                     | $V_{REF}$ |                 |                    |                 |        |                                                                                                                                               |
| Output Voltage                                        |           |                 | ( $V_{CC} + 1$ )/2 |                 | V      | −500 μA to +500 μA                                                                                                                            |
| Output Resistance                                     |           |                 | 250                |                 | Ω      |                                                                                                                                               |
| AC PERFORMANCE                                        |           |                 |                    |                 |        |                                                                                                                                               |
| Propagation Delay                                     | $t_{PD}$  | 70              | 95                 | 125             | ps     | $V_{CC} = 3.3$ V ± 10%,<br>$V_{ICM} = V_{REF}$ , $V_{ID} = 0.5$ V p-p<br>$V_{CC} = 2.5$ V ± 5%,<br>$V_{ICM} = V_{REF}$ , $V_{ID} = 0.5$ V p-p |
|                                                       |           | 70              | 95                 | 125             | ps     |                                                                                                                                               |
| Propagation Delay Temperature Coefficient             |           |                 | 50                 |                 | fs/°C  |                                                                                                                                               |
| Propagation Delay Skew (Output to Output)<br>ADCLK907 |           |                 |                    | 15              | ps     | $V_{ID} = 0.5$ V                                                                                                                              |
| Propagation Delay Skew (Output to Output)<br>ADCLK925 |           |                 |                    | 10              | ps     | $V_{ID} = 0.5$ V                                                                                                                              |
| Propagation Delay Skew (Device to Device)             |           |                 |                    | 35              | ps     | $V_{ID} = 0.5$ V                                                                                                                              |
| Toggle Rate                                           |           | 6               | 7.5                |                 | GHz    | >0.8 V differential output swing,<br>$V_{CC} = 3.3$ V ± 10%                                                                                   |
|                                                       |           |                 | 6.5                |                 | GHz    | >0.8 V differential output swing,<br>$V_{CC} = 2.5$ V ± 5%                                                                                    |
| Random Jitter                                         | RJ        |                 | 60                 |                 | fs rms | $V_{ID} = 1600$ mV, 8 V/ns, $V_{ICM} = 1.85$ V                                                                                                |
| Rise/Fall Time                                        | $t_R/t_F$ | 30              |                    | 85              | ps     | 20%/80%                                                                                                                                       |
| Additive Phase Noise                                  |           |                 |                    |                 |        |                                                                                                                                               |
| 622.08 MHz                                            |           |                 | −138               |                 | dBc/Hz | @10 Hz offset                                                                                                                                 |
|                                                       |           |                 | −144               |                 | dBc/Hz | @100 Hz offset                                                                                                                                |
|                                                       |           |                 | −152               |                 | dBc/Hz | @1 kHz offset                                                                                                                                 |
|                                                       |           |                 | −159               |                 | dBc/Hz | @10 kHz offset                                                                                                                                |
|                                                       |           |                 | −161               |                 | dBc/Hz | @100 kHz offset                                                                                                                               |
|                                                       |           |                 | −161               |                 | dBc/Hz | >1 MHz offset                                                                                                                                 |
| 122.88 MHz                                            |           |                 | −135               |                 | dBc/Hz | @10 Hz offset                                                                                                                                 |
|                                                       |           |                 | −145               |                 | dBc/Hz | @100 Hz offset                                                                                                                                |
|                                                       |           |                 | −153               |                 | dBc/Hz | @1 kHz offset                                                                                                                                 |
|                                                       |           |                 | −160               |                 | dBc/Hz | @10 kHz offset                                                                                                                                |
|                                                       |           |                 | −161               |                 | dBc/Hz | @100 kHz offset                                                                                                                               |
|                                                       |           |                 | −161               |                 | dBc/Hz | >1 MHz offset                                                                                                                                 |

| Parameter                                  | Symbol            | Min   | Typ | Max  | Unit | Test Conditions/Comments                  |
|--------------------------------------------|-------------------|-------|-----|------|------|-------------------------------------------|
| POWER SUPPLY                               |                   |       |     |      |      |                                           |
| Supply Voltage Requirement                 | $V_{CC} - V_{EE}$ | 2.375 |     | 3.63 | V    | 2.5 V – 5% to 3.3 V + 10%                 |
| Power Supply Current                       |                   |       |     |      |      | Static                                    |
| ADCLK905                                   |                   |       |     |      |      |                                           |
| Negative Supply Current                    | $I_{VEE}$         |       | 24  |      | mA   | $V_{CC} - V_{EE} = 2.5\text{ V}$          |
|                                            |                   |       | 25  | 40   | mA   | $V_{CC} - V_{EE} = 3.3\text{ V} \pm 10\%$ |
| Positive Supply Current                    | $I_{VCC}$         |       | 47  |      | mA   | $V_{CC} - V_{EE} = 2.5\text{ V}$          |
|                                            |                   |       | 48  | 63   | mA   | $V_{CC} - V_{EE} = 3.3\text{ V} \pm 10\%$ |
| ADCLK907                                   |                   |       |     |      |      |                                           |
| Negative Supply Current                    | $I_{VEE}$         |       | 48  |      | mA   | $V_{CC} - V_{EE} = 2.5\text{ V}$          |
|                                            |                   |       | 50  | 80   | mA   | $V_{CC} - V_{EE} = 3.3\text{ V} \pm 10\%$ |
| Positive Supply Current                    | $I_{VCC}$         |       | 94  |      | mA   | $V_{CC} - V_{EE} = 2.5\text{ V}$          |
|                                            |                   |       | 96  | 126  | mA   | $V_{CC} - V_{EE} = 3.3\text{ V} \pm 10\%$ |
| ADCLK925                                   |                   |       |     |      |      |                                           |
| Negative Supply Current                    | $I_{VEE}$         |       | 29  |      | mA   | $V_{CC} - V_{EE} = 2.5\text{ V}$          |
|                                            |                   |       | 31  | 51   | mA   | $V_{CC} - V_{EE} = 3.3\text{ V} \pm 10\%$ |
| Positive Supply Current                    | $I_{VCC}$         |       | 76  |      | mA   | $V_{CC} - V_{EE} = 2.5\text{ V}$          |
|                                            |                   |       | 77  | 97   | mA   | $V_{CC} - V_{EE} = 3.3\text{ V} \pm 10\%$ |
| Power Supply Rejection <sup>1</sup>        | $PSR_{VCC}$       |       | 3   |      | ps/V | $V_{CC} - V_{EE} = 3.0\text{ V} \pm 20\%$ |
| Output Swing Supply Rejection <sup>2</sup> | $PSR_{VCC}$       |       | 26  |      | dB   | $V_{CC} - V_{EE} = 3.0\text{ V} \pm 20\%$ |

<sup>1</sup> Change in  $T_{PD}$  per change in  $V_{CC}$ .<sup>2</sup> Change in output swing per change in  $V_{CC}$ .

## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter                                                                                    | Rating                                          |
|----------------------------------------------------------------------------------------------|-------------------------------------------------|
| Supply Voltage<br>$V_{CC} - V_{EE}$                                                          | 6.0 V                                           |
| Input Voltage<br>D (D1, D2), $\overline{D}$ ( $\overline{D1}$ , $\overline{D2}$ )            | $V_{EE} - 0.5$ V to<br>$V_{CC} + 0.5$ V         |
| D1, D2, $\overline{D1}$ , $\overline{D2}$ to $V_T$ Pin<br>(CML or PECL Termination)          | $\pm 40$ mA                                     |
| D (D1, D2) to $\overline{D}$ ( $\overline{D1}$ , $\overline{D2}$ )                           | $\pm 1.8$ V                                     |
| Maximum Voltage on Output Pins                                                               | $V_{CC} + 0.5$ V                                |
| Maximum Output Current                                                                       | 35 mA                                           |
| Input Termination, $V_T$ to D (D1, D2), $\overline{D}$ ( $\overline{D1}$ , $\overline{D2}$ ) | $\pm 2$ V                                       |
| Voltage Reference, $V_{REF}$                                                                 | $V_{CC} - V_{EE}$                               |
| Temperature                                                                                  |                                                 |
| Operating Temperature Range, Ambient                                                         | $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |
| Operating Temperature, Junction                                                              | $150^{\circ}\text{C}$                           |
| Storage Temperature Range                                                                    | $-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

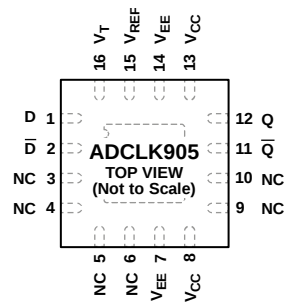
| Package Type  | $\theta_{JA}$ | Unit                        |
|---------------|---------------|-----------------------------|
| 16-Lead LFCSP | 70            | $^{\circ}\text{C}/\text{W}$ |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



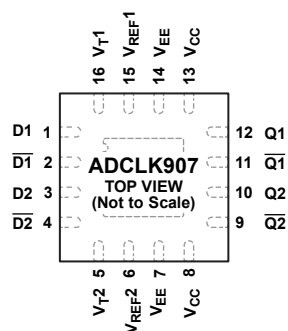
- NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
  2. EXPOSED PAD. THE EXPOSED PAD IS NOT ELECTRICALLY CONNECTED TO ANY PART OF THE CIRCUIT. IT CAN BE LEFT FLOATING FOR OPTIMAL ELECTRICAL ISOLATION BETWEEN THE PACKAGE HANDLE AND THE SUBSTRATE OF THE DIE. IT CAN ALSO BE SOLDERED TO THE APPLICATION BOARD IF IMPROVED THERMAL AND/OR MECHANICAL STABILITY IS DESIRED. EXPOSED METAL AT THE CORNERS OF THE PACKAGE IS CONNECTED TO THIS EXPOSED PAD. ALLOW SUFFICIENT CLEARANCE TO VIAS AND OTHER COMPONENTS.

06318-004

Figure 4. ADCLK905 Pin Configuration

Table 4. Pin Function Descriptions for 1:1 ADCLK905 Buffer

| Pin No.           | Mnemonic       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------------------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                 | D              | Noninverting Input.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 2                 | $\overline{D}$ | Inverting Input.                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 3, 4, 5, 6, 9, 10 | NC             | No Connect. No physical connection to the die.                                                                                                                                                                                                                                                                                                                                                                                                               |
| 7, 14             | $V_{EE}$       | Negative Supply Voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8, 13             | $V_{CC}$       | Positive Supply Voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 11                | $\overline{Q}$ | Inverting Output.                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 12                | Q              | Noninverting Output.                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15                | $V_{REF}$      | Reference Voltage. Reference voltage for biasing ac-coupled inputs.                                                                                                                                                                                                                                                                                                                                                                                          |
| 16                | $V_T$          | Center Tap. Center tap of 100 $\Omega$ input resistor.                                                                                                                                                                                                                                                                                                                                                                                                       |
|                   | EPAD           | Exposed Pad. The exposed pad is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired. Exposed metal at the corners of the package is connected to this exposed pad. Allow sufficient clearance to vias and other components. |



## NOTES

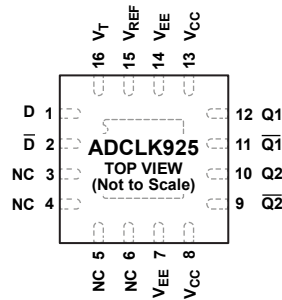
1. EXPOSED PAD. THE EXPOSED PAD IS NOT ELECTRICALLY CONNECTED TO ANY PART OF THE CIRCUIT. IT CAN BE LEFT FLOATING FOR OPTIMAL ELECTRICAL ISOLATION BETWEEN THE PACKAGE HANDLE AND THE SUBSTRATE OF THE DIE. IT CAN ALSO BE SOLDERED TO THE APPLICATION BOARD IF IMPROVED THERMAL AND/OR MECHANICAL STABILITY IS DESIRED. EXPOSED METAL AT THE CORNERS OF THE PACKAGE IS CONNECTED TO THIS EXPOSED PAD. ALLOW SUFFICIENT CLEARANCE TO VIAS AND OTHER COMPONENTS.

06319-005

Figure 5. ADCLK907 Pin Configuration

Table 5. Pin Function Descriptions for Dual 1:1 ADCLK907 Buffer

| Pin No. | Mnemonic        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | D1              | Noninverting Input 1.                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 2       | $\overline{D1}$ | Inverting Input 1.                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 3       | D2              | Noninverting Input 2.                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 4       | $\overline{D2}$ | Inverting Input 2.                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 5       | VT2             | Center Tap 2. Center tap of 100 $\Omega$ input resistor, Channel 2.                                                                                                                                                                                                                                                                                                                                                                                          |
| 6       | VREF2           | Reference Voltage 2. Reference voltage for biasing ac-coupled inputs, Channel 2.                                                                                                                                                                                                                                                                                                                                                                             |
| 7, 14   | VEE             | Negative Supply Voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8, 13   | VCC             | Positive Supply Voltage. Pin 8 and Pin 13 are not strapped internally.                                                                                                                                                                                                                                                                                                                                                                                       |
| 9       | $\overline{Q2}$ | Inverting Output 2.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 10      | Q2              | Noninverting Output 2.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 11      | $\overline{Q1}$ | Inverting Output 1.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 12      | Q1              | Noninverting Output 1.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15      | VREF1           | Reference Voltage 1. Reference voltage for biasing ac-coupled inputs, Channel 1.                                                                                                                                                                                                                                                                                                                                                                             |
| 16      | VT1             | Center Tap 1. Center tap of 100 $\Omega$ input resistor, Channel 1.                                                                                                                                                                                                                                                                                                                                                                                          |
|         | EPAD            | Exposed Pad. The exposed pad is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired. Exposed metal at the corners of the package is connected to this exposed pad. Allow sufficient clearance to vias and other components. |



## NOTES

1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. EXPOSED PAD. THE EXPOSED PAD IS NOT ELECTRICALLY CONNECTED TO ANY PART OF THE CIRCUIT. IT CAN BE LEFT FLOATING FOR OPTIMAL ELECTRICAL ISOLATION BETWEEN THE PACKAGE HANDLE AND THE SUBSTRATE OF THE DIE. IT CAN ALSO BE SOLDERED TO THE APPLICATION BOARD IF IMPROVED THERMAL AND/OR MECHANICAL STABILITY IS DESIRED. EXPOSED METAL AT THE CORNERS OF THE PACKAGE IS CONNECTED TO THIS EXPOSED PAD. ALLOW SUFFICIENT CLEARANCE TO VIAS AND OTHER COMPONENTS.

06318-006

Figure 6. ADCLK925 Pin Configuration

Table 6. Pin Function Descriptions for 1:2 ADCLK925 Buffer

| Pin No.    | Mnemonic        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | D               | Noninverting Input.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 2          | $\overline{D}$  | Inverting Input.                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 3, 4, 5, 6 | NC              | No Connect. No physical connection to the die.                                                                                                                                                                                                                                                                                                                                                                                                               |
| 7, 14      | $V_{EE}$        | Negative Supply Voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8, 13      | $V_{CC}$        | Positive Supply Voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 9          | $\overline{Q2}$ | Inverting Output 2.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 10         | $Q2$            | Noninverting Output 2.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 11         | $\overline{Q1}$ | Inverting Output 1.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 12         | $Q1$            | Noninverting Output 1.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15         | $V_{REF}$       | Reference Voltage. Reference voltage for biasing ac-coupled inputs.                                                                                                                                                                                                                                                                                                                                                                                          |
| 16         | $V_T$           | Center Tap. Center tap of 100 $\Omega$ input resistor.                                                                                                                                                                                                                                                                                                                                                                                                       |
|            | EPAD            | Exposed Pad. The exposed pad is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired. Exposed metal at the corners of the package is connected to this exposed pad. Allow sufficient clearance to vias and other components. |

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , outputs terminated  $50\ \Omega$  to  $V_{CC} - 2\text{ V}$ , unless otherwise noted.

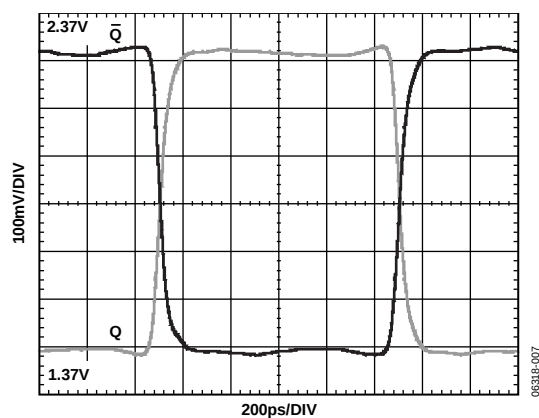


Figure 7. Output Waveform,  $V_{CC} = 3.3\text{ V}$

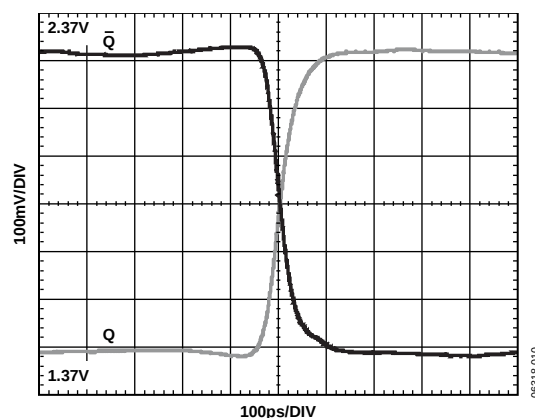


Figure 10. Output Waveform,  $V_{CC} = 3.3\text{ V}$

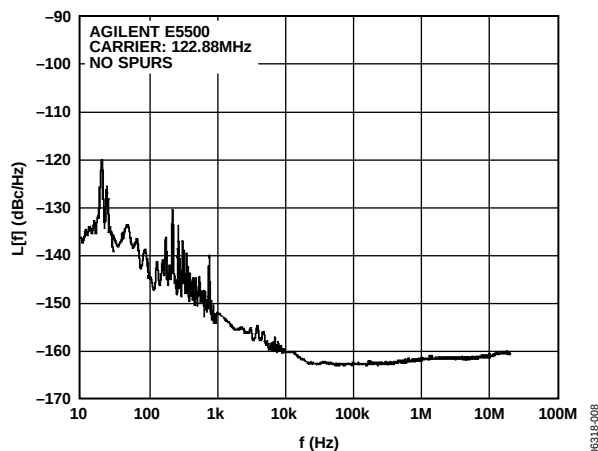


Figure 8. Phase Noise at 122.88 MHz

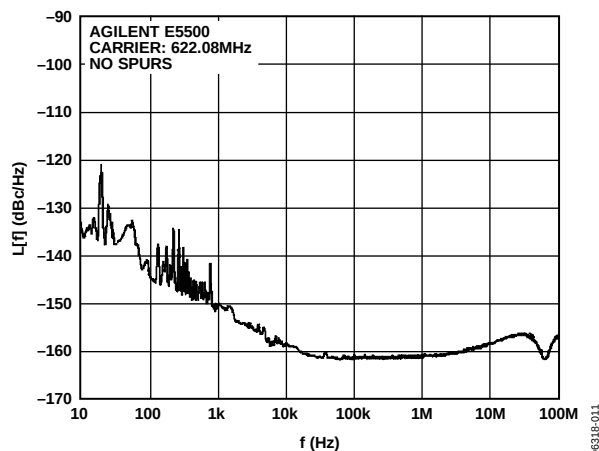


Figure 11. Phase Noise at 622.08 MHz

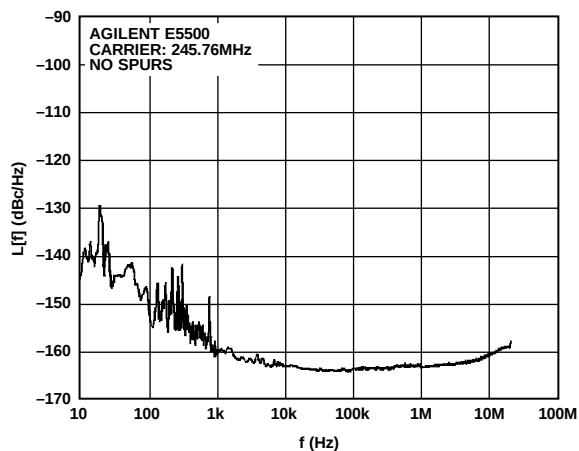


Figure 9. Phase Noise at 245.76 MHz

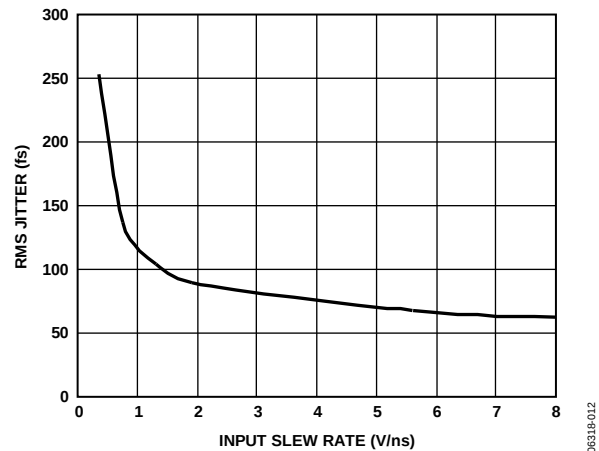


Figure 12. RMS Jitter vs. Input Slew Rate

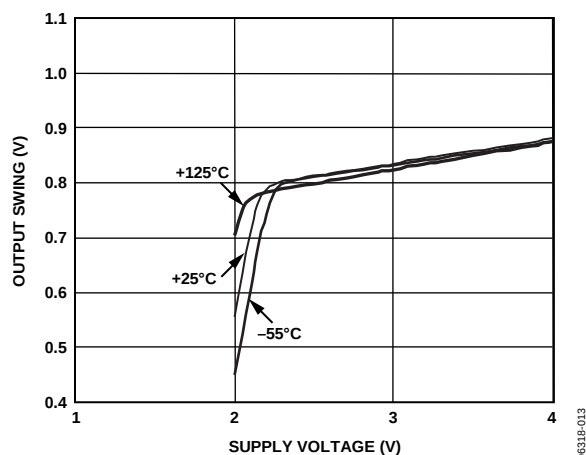
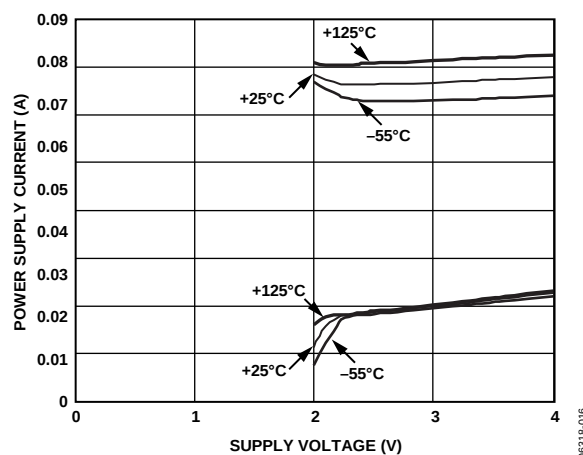
Figure 13.  $V_{OD}$  vs. Power Supply Voltage

Figure 16. Power Supply Current vs. Supply Voltage, ADCLK925

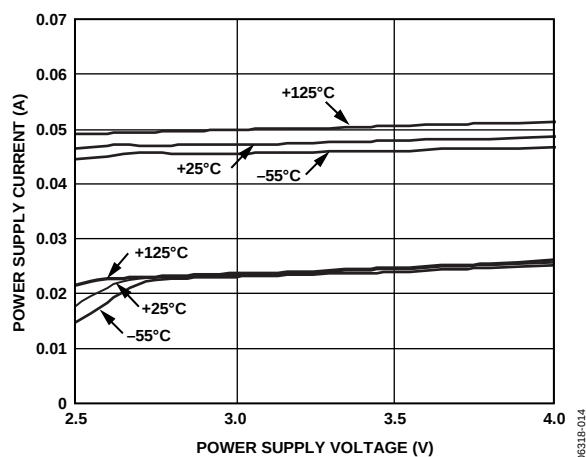


Figure 14. Power Supply Current vs. Power Supply Voltage, ADCLK905

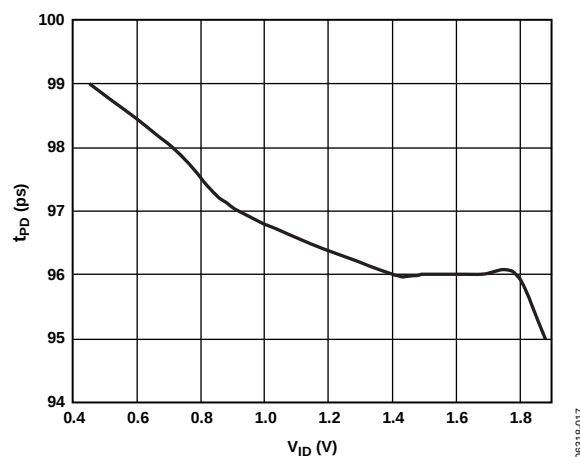
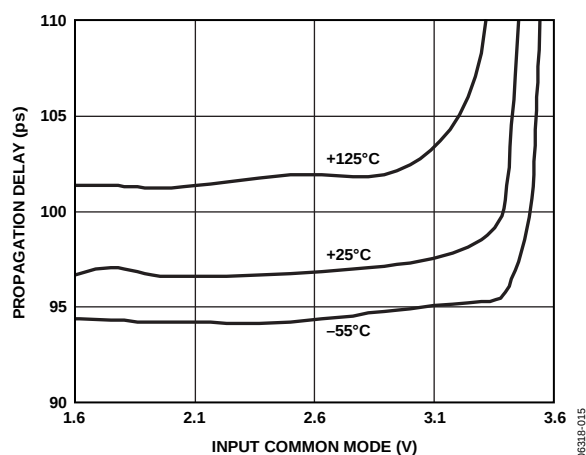
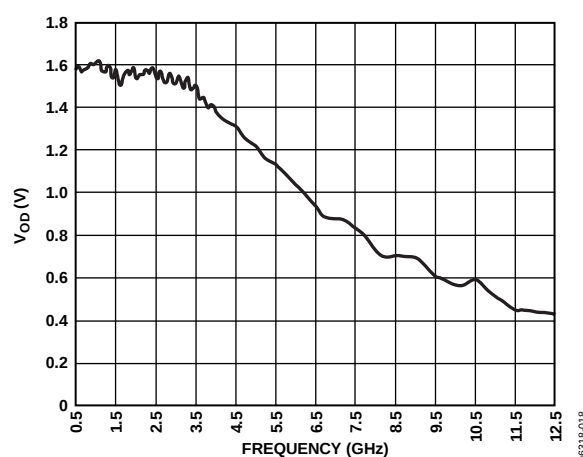
Figure 17. Propagation Delay vs.  $V_{ID}$ Figure 15. Propagation Delay vs.  $V_{ICM}$ ; Input Swing = 200 mV

Figure 18. Toggle Rate, Differential Output Swing vs. Frequency

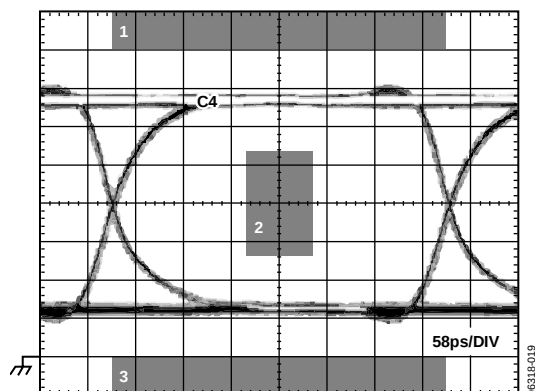


Figure 19. 2.488 Gbps PRBS  $2^{23} - 1$  with OC-48/STM-16 Mask,  
Measured p-p Jitter 8.1 ps, Source p-p Jitter 3.5 ps

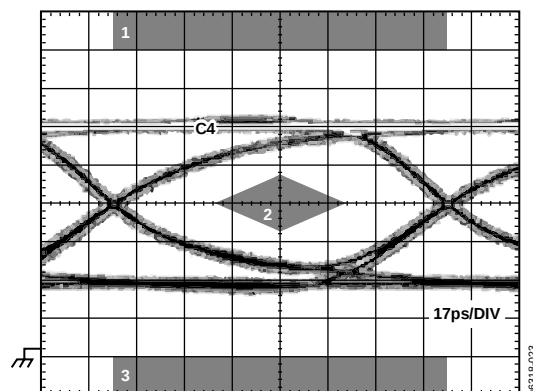


Figure 22. 8.50 Gbps PRBS  $2^{23} - 1$  with FC8500E ABS Beta Rx Mask,  
Measured p-p Jitter 10.9 ps, Source p-p Jitter 4.4 ps

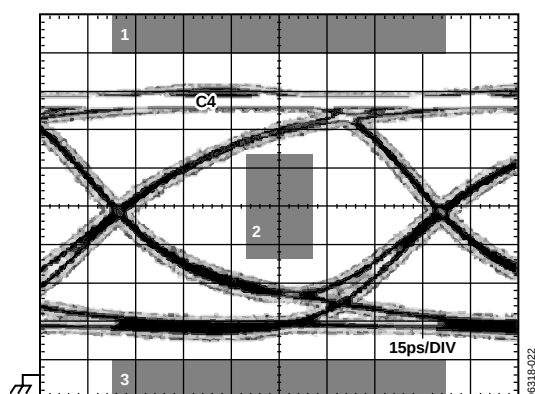


Figure 20. 9.95 Gbps PRBS  $2^{23} - 1$  with OC-193/STM-64 Mask,  
Measured p-p Jitter 10.5 ps, Source p-p Jitter 6.0 ps

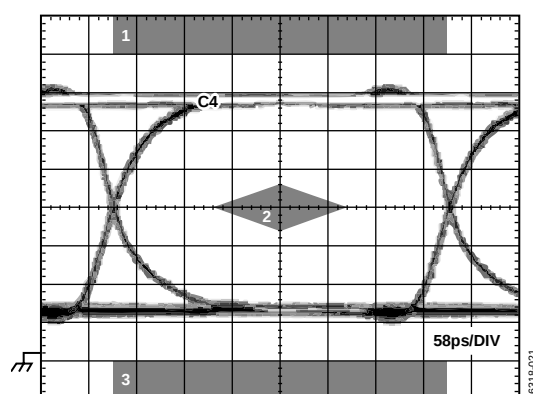


Figure 23. 2.5 Gbps PRBS  $2^{23} - 1$  with PCI Express 2.5 Rx Mask,  
Measured p-p Jitter 8.1 ps, Source p-p Jitter 3.5 ps

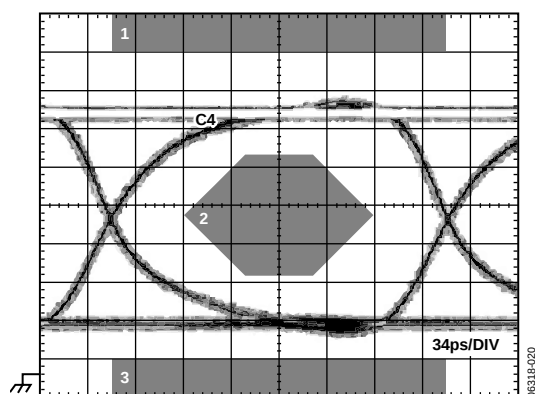


Figure 21. 4.25 Gbps PRBS  $2^{23} - 1$  with FC4250 (Optical) Mask,  
Measured p-p Jitter 8.2 ps, Source p-p Jitter 3.4 ps

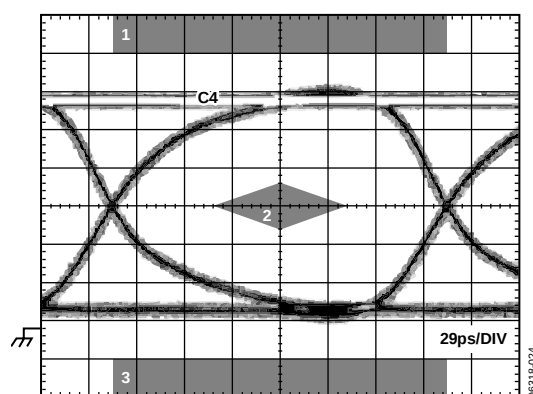


Figure 24. 5.0 Gbps PRBS  $2^{23} - 1$  with PCI Express 5.0 Rx Mask,  
Measured p-p Jitter 8.7 ps, Source p-p Jitter 3.5 ps

## APPLICATIONS INFORMATION

### POWER/GROUND LAYOUT AND BYPASSING

The ADCLK905/ADCLK907/ADCLK925 buffers are designed for very high speed applications. Consequently, high speed design techniques must be used to achieve the specified performance. It is critically important to use low impedance supply planes for both the negative supply ( $V_{EE}$ ) and the positive supply ( $V_{CC}$ ) planes as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. A 1  $\mu\text{F}$  electrolytic bypass capacitor should be placed within several inches of each power supply pin to ground. In addition, multiple high quality 0.001  $\mu\text{F}$  bypass capacitors should be placed as close as possible to each of the  $V_{EE}$  and  $V_{CC}$  supply pins and should be connected to the GND plane with redundant vias. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should be strictly avoided to maximize the effectiveness of the bypass at high frequencies.

### OUTPUT STAGES

The specified performance can be achieved only by using proper transmission line terminations. The outputs of the ADCLK905/ADCLK907/ADCLK925 buffers are designed to directly drive 800 mV into 50  $\Omega$  cable or microstrip/stripline transmission lines terminated with 50  $\Omega$  referenced to  $V_{CC} - 2\text{ V}$ . The PECL output stage is shown in Figure 25. The outputs are designed for best transmission line matching. If high speed signals must be routed more than a centimeter, either the microstrip or the stripline technique is required to ensure proper transition times and to prevent excessive output ringing and pulse width-dependent propagation delay dispersion.

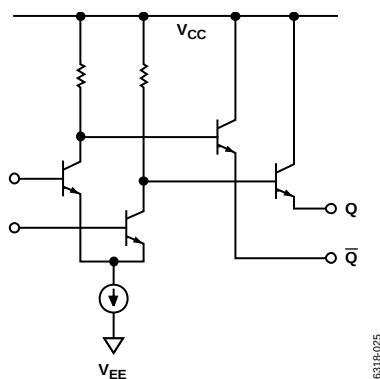


Figure 25. Simplified Schematic Diagram of the ADCLK905/ADCLK907/ADCLK925 PECL Output Stage

### OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed circuit, proper design and layout techniques are essential to obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and cause oscillation. Discontinuities along input and output transmission lines can also severely limit the specified jitter performance by reducing the effective input slew rate.

In a 50  $\Omega$  environment, input and output matching have a significant impact on performance. The buffer provides internal 50  $\Omega$  termination resistors for both D and  $\bar{D}$  inputs. The return side should normally be connected to the reference pin provided. The termination potential should be carefully bypassed, using ceramic capacitors to prevent undesired aberrations on the input signal due to parasitic inductance in the termination return path. If the inputs are directly coupled to a source, care must be taken to ensure the pins are within the rated input differential and common-mode ranges.

If the return is floated, the device exhibits 100  $\Omega$  cross termination, but the source must then control the common-mode voltage and supply the input bias currents.

There are ESD/clamp diodes between the input pins to prevent the application of excessive offsets to the input transistors. ESD diodes are not optimized for best ac performance. When a clamp is desired, it is recommended that appropriate external diodes be used.

### BUFFER RANDOM JITTER

The ADCLK905/ADCLK907/ADCLK925 are specifically designed to minimize added random jitter over a wide input slew rate range. Provided sufficient voltage swing is present, random jitter is affected most by the slew rate of the input signal. Whenever possible, excessively large input signals should be clamped with fast Schottky diodes because attenuators reduce the slew rate. Input signal runs of more than a few centimeters should be over low loss dielectrics or cables with good high frequency characteristics.

## TYPICAL APPLICATION CIRCUITS

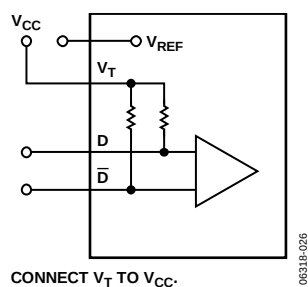


Figure 26. Interfacing to CML Inputs

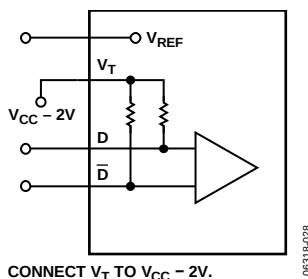
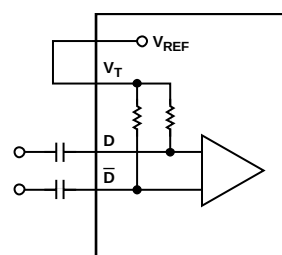


Figure 27. Interfacing to PECL



NOTES  
1. PLACING A BYPASS CAPACITOR FROM  $V_T$  TO GROUND CAN IMPROVE THE NOISE PERFORMANCE.

Figure 28. AC Coupling Differential Signals

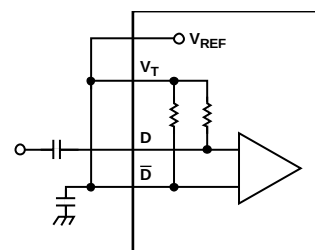
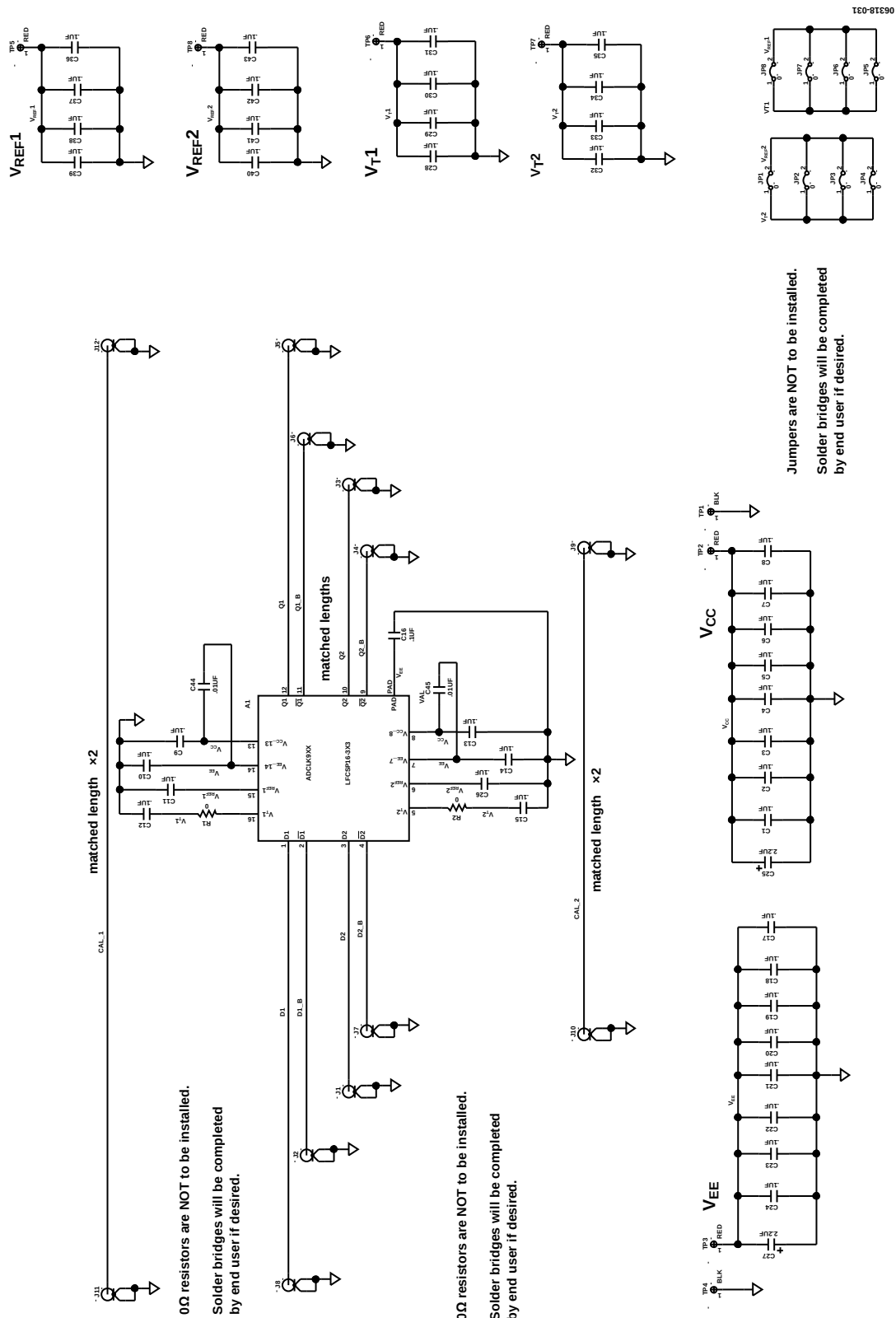
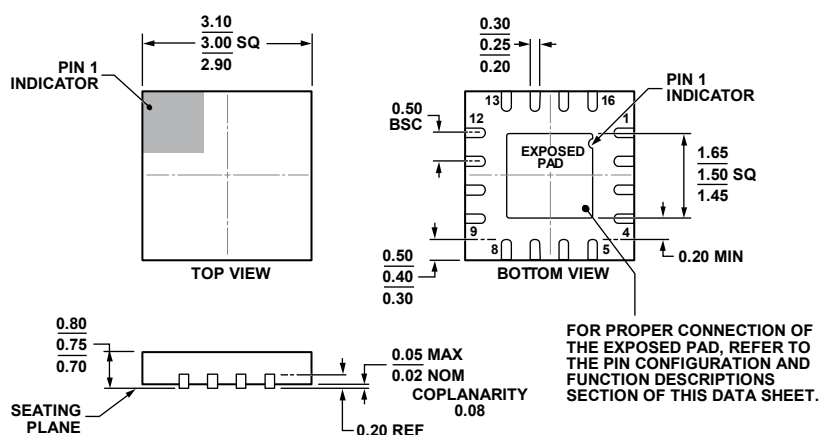


Figure 29. Interfacing to AC-Coupled Single-Ended Inputs

## EVALUATION BOARD SCHEMATIC



## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 31. 16-Lead Lead Frame Chip Scale Package [LFCSP]  
3 mm × 3 mm Body and 0.75 mm Package Height  
(CP-16-27)

Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                           | Package Option | Branding |
|--------------------|-------------------|-----------------------------------------------|----------------|----------|
| ADCLK905BCPZ-WP    | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-27       | Y03      |
| ADCLK905BCPZ-R7    | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-27       | Y03      |
| ADCLK905BCPZ-R2    | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-27       | Y03      |
| ADCLK907BCPZ-WP    | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-27       | Y06      |
| ADCLK907BCPZ-R7    | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-27       | Y06      |
| ADCLK907BCPZ-R2    | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-27       | Y06      |
| ADCLK925BCPZ-WP    | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-27       | Y08      |
| ADCLK925BCPZ-R7    | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-27       | Y08      |
| ADCLK925BCPZ-R2    | −40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-27       | Y08      |
| ADCLK905/PCBZ      |                   | Evaluation Board                              |                |          |
| ADCLK907/PCBZ      |                   | Evaluation Board                              |                |          |
| ADCLK925/PCBZ      |                   | Evaluation Board                              |                |          |

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**