ABSOLUTE MAXIMUM RATINGS	ADC-815	ADC-825
Positive Supply	+18V	
Negative Supply	−18V	
Logic Supply	+7V	
Digital Inputs	+5.5V	
Analog Inputs	±25V	

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

INPUTS	
Analog Input Ranges,[1] Unipolar	0 to +5V, 0 to +10V, 0 to +20V
Bipolar	±2.5V, ±5V, ±10V
Input Impedance, 5V Range	1.34K
10V Range	2.3K
20V Range	4.27K
Start Conversion	+2V min. to +5.5V max. Positive Pulse 50 nsec. min. duration, 10 nsec. typ. rise and fall times. Positive Going Edge resets outputs to 011...1 and sets $\overline{EOC}$ high. Negative going edge initiates conversion. Loading: 2 TTL loads.
Bipolar Offset	Hold high (+5V) for bipolar operation, hold low (ground) for unipolar operation.
OUTPUTS	
Parallel Output Data	9 parallel lines (8 binary bits plus $\overline{MSB}$) V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V Loading: 4 TTL loads
Serial Output Data	NRZ format successive Decision pulse output at internal clock rate generated during conversion. MSB first. Loading: 4 TTL loads
Coding, Unipolar	Straight Binary
Bipolar	Offset Binary, Two's Complement
$\overline{EOC}$	Conversion Status Signal. High ≥ +2.4V during conversion and reset periods. Low ≤ +0.4V when conversion complete. Loading: 4 TTL loads
Clock Output	Internal clock pulse train of negative going pulses[2] from +5V to 0V. Loading: 6 TTL loads

PERFORMANCE		
Conversion Time[3], max.	700 nsec.	1 μsec.
Resolution	8 bits	
Nonlinearity	±½ LSB max.	
Differential Nonlinearity	±½ LSB max.	
Gain Error	±½ LSB max.	
Zero Error	±½ LSB max.	
Gain Tempco, 0°C to +70°C[4]	±20 ppm of FSR/°C max.[5]	
Zero Drift	±150 μV/°C max.	
Offset Tempco	±15 ppm of FSR/°C Max.[5]	
Long Term Stability	±0.02% year	
No Missing Codes	Over Operating Temp. Range	
Power Supply Rejection, max.	±0.06%/% Supply	

POWER REQUIREMENTS	
Analog Supply	±15V ±0.5V at 35 mA max. −15V ±0.5V at 15 mA max.
Logic Supply	+5V ±0.25V at 100 mA max.
Power Dissipation	1.25W max.

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range, MC	0°C to +70°C
MR	−25°C to +85°C
MM	−55°C to +125°C
Storage Temp. Range	−65°C to +150°C
Package Type	24 pin Ceramic DIP
Pins	0.010 x 0.018 inch Kovar
Weight	0.2 ounces (6 grams)

FOOTNOTES:

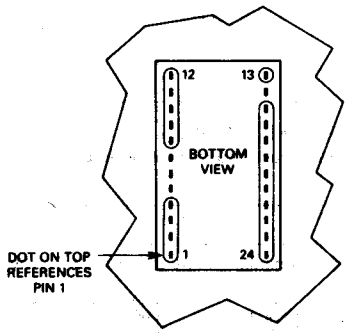
1. Unused analog inputs must be grounded.
2. At 15.9 MHz for the ADC-815, 9.52 MHz for the ADC-825.
3. The conversion time temperature coefficient for these converters is 0.15%/°C. This tempco is positive.
4. Doubles outside this temperature range.
5. FSR is Full Scale Range.

TECHNICAL NOTES

1. The high operating speed of these converters requires that good high frequency board layout techniques be used. Leads from data outputs should be kept as short as possible, output leads longer than 1 inch (2.5 cm) require the use of an output register. Use of a ground plane is particularly important with high-speed data converters as it reduces high frequency noise and aids in decoupling analog signals from digital signals. Ground loop problems are avoided by connecting all grounds on the board to the ground plane. The basic configuration of the ground plane directly below the ADC-815 or ADC-825 is shown in the ground plane layout diagram. This layout should be modified after selection of analog input range to include unused analog inputs.
2. Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference. Unused analog inputs should be grounded.
3. Applications of the ADC-815 and ADC-825 that require an input buffer amplifier may be satisfied by the use of DATEL's AM-1435, an ultra fast hybrid device featuring a maximum settling time of 85 nanoseconds.
4. Analog and digital supplies are internally bypassed to ground with 0.01 μF capacitors; however, it is recommended that the +15V, −15V and +5V supplies be additionally bypassed externally with 1 μF electrolytic capacitors as shown in the connection diagrams.
5. In the bipolar mode, two's complement output coding is available by using the $\overline{MSB}$ output (pin 16); offset binary coding is obtained by using the MSB output (pin 17). Unipolar operation requires use of the MSB output (pin 17) to achieve straight binary output coding.

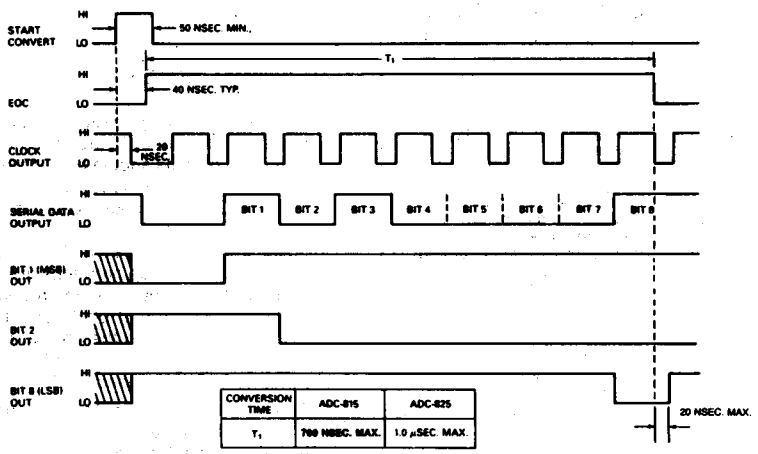
6. Serial output data is available at pin 1 in standard NRZ format with the MSB appearing first. Coding is straight binary for unipolar operation or offset binary for bipolar operation. Synchronization of serial output data is achieved by use of the clock output (pin 13). Each data bit is valid when the clock output is high and appears in succession from the MSB at the second clock low to high transition to the LSB at the ninth clock low to high transition.
7. Applications of these converters that require the use of a sample-hold may be satisfied by DATEL's model SHM-40, an ultra-fast hybrid unit featuring 40 nanosecond acquisition time and a ±2.5V input range.
8. These converters have a maximum power dissipation of 1.25W. The case-to-ambient thermal resistance for this package is approximately 33°C per watt. For operation in ambient temperatures exceeding +83°C, airflow of at least 400 linear feet per minute is recommended.

BASIC GROUND PLANE LAYOUT



THIS BASIC GROUND PLANE LAYOUT SHOULD BE MODIFIED BEFORE IMPLEMENTATION TO INCLUDE UNUSED ANALOG INPUTS.

TIMING DIAGRAM FOR ADC-815, ADC-825
OUTPUT: 10100001



CONVERSION TIME	ADC-815	ADC-825
T_1	700 NSEC. MAX.	1.0 µSEC. MAX.

CODING TABLES

UNIPOLAR OPERATION

UNIPOLAR SCALE	OUTPUT CODING* STRAIGHT BINARY	ANALOG INPUT 0 to +5V	0 to +10V	0 to +20V
F.S. - 1 LSB	1111 1111	+4.980V	+9.961V	+19.922V
¾ F.S.	1100 0000	+3.750V	+7.500V	+15.000V
½ F.S.	1000 0000	+2.500V	+5.000V	+10.000V
¼ F.S.	0100 0000	+1.250V	+2.500V	+5.000V
1 LSB	0000 0001	+0.020V	+0.039V	+0.078V
0	0000 0000	0.000V	0.000V	0.000V

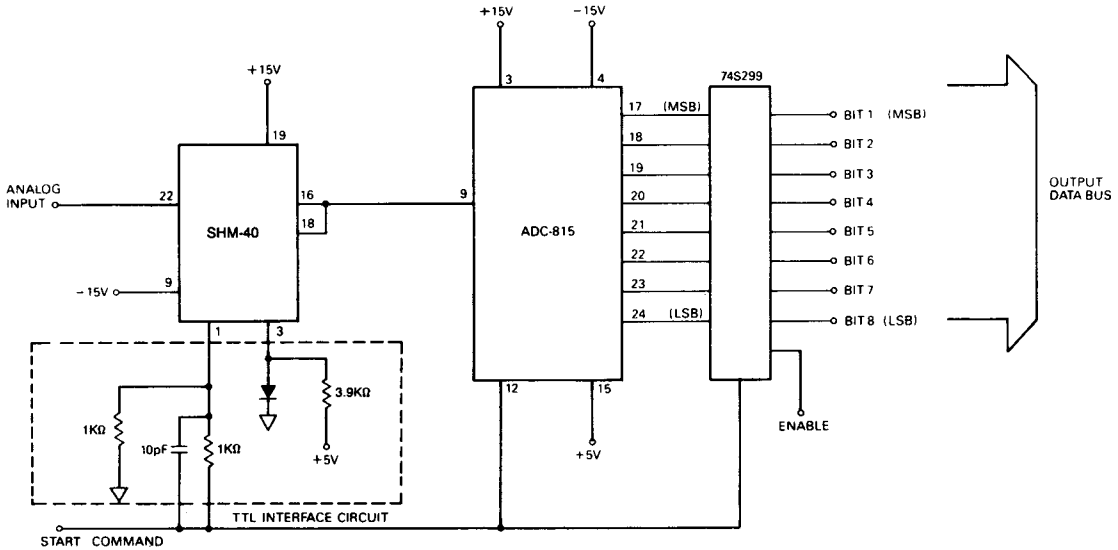
*FOR PARALLEL OR SERIAL OUTPUT DATA

BIPOLAR OPERATION

BIPOLAR SCALE	OUTPUT CODING OFFSET BINARY[1]	OUTPUT CODING TWO'S COMPLEMENT[2]	INPUT VOLTAGE RANGE ±2.5V	±5V	±10V
+F.S.−1 LSB	1111 1111	0111 1111	+2.480V	+4.961V	+9.922V
+½ F.S.	1100 0000	0100 0000	+1.250V	+2.500V	+5.000V
+1 LSB	1000 0001	0000 0001	+0.020V	+0.039V	+0.078V
0	1000 0000	0000 0000	0.000V	0.000V	0.000V
−½ F.S.	0100 0000	1100 0000	−1.250V	−2.500V	−5.000V
−F.S.+1 LSB	0000 0001	1000 0001	−2.480V	−4.961V	+9.922V
−F.S.	0000 0000	1000 0000	−2.500V	−5.000V	+10.000V

NOTES: 1. FOR PARALLEL OR SERIAL OUTPUT DATA
2. FOR PARALLEL OUTPUT DATA ONLY

HIGH SPEED DATA SYSTEM



This diagram represents a high speed data system using DATEL's SHM-40 and ADC-815, with an output register, to drive a data bus. The Start Command is a 60 nsec wide, TTL-compatible pulse with a maximum frequency of 1.5 MHz. Upon receipt of a start command, the SHM-40 will track the input voltage and the ADC-815 will reset. On the trailing edge of the start command, the SHM-40 will hold the input and the ADC-815 will begin its conversion. On the leading edge of the next start command, the output data will be clocked out of the output three-state register. The ADC-815 is an 8-bit, 700 nsec, analog-to-digital converter. With this system, a ±2.5V input step can be acquired to 0.1% accuracy in 40 nsec and held to within 80 μV while the A/D conversion takes place. The SHM-40 can also be used with the DATEL's ADC-816, which will yield 10 bits of resolution.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
ADC-815MC	0°C to +70°C
ADC-815MM	-55°C to +125°C
ADC-825MC	0°C to +70°C
ADC-825MM	-55°C to +125°C

ACCESSORIES

Part Number	Description
DILS-3	Mating Socket, 24-pin socket

For military devices compliant with MIL-STD-883, contact DATEL.