AD532—SPECIFICATIONS (@ 25°C, V_S = ±15 V, R ≥ 2 kΩ V_{OS} grounded, unless otherwise noted.)

Model	AD532J Min	AD532J Typ	AD532J Max	AD532K Min	AD532K Typ	AD532K Max	AD532S Min	AD532S Typ	AD532S Max	Unit
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}$		
Total Error (–10 V ≤ X, Y ≤ +10 V)		±1.5	**±2.0**		±0.7	**±1.0**		±0.5	**±1.0**	%
T_A = Min to Max		±2.5			±1.5				**±4.0**	%
Total Error vs. Temperature		±0.04			±0.03			±0.01	**±0.04**	%/°C
Supply Rejection (±15 V ± 10%)		±0.05			±0.05			±0.05		%/%
Nonlinearity, X (X = 20 V p-p, Y = 10 V)		±0.8			±0.5			±0.5		%
Nonlinearity, Y (Y = 20 V p-p, X = 10 V)		±0.3			±0.2			±0.2		%
Feedthrough, X (Y Nulled, X = 20 V p-p 50 Hz)		50	**200**		30	**100**		30	**100**	mV
Feedthrough, Y (X Nulled, Y = 20 V p-p 50 Hz)		30	**150**		25	**80**		25	**80**	mV
Feedthrough vs. Temperature		2.0			1.0			1.0		mV p-p/°C
Feedthrough vs. Power Supply		±0.25			±0.25			±0.25		mV/%
DYNAMICS										
Small Signal BW (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error		75			75			75		kHz
Slew Rate (V_{OUT} 20 p-p)		45			45			45		V/µs
Settling Time (to 2%, ΔV_{OUT} = 20 V)		1			1			1		µs
NOISE										
Wideband Noise f = 5 Hz to 10 kHz		0.6			0.6			0.6		mV (rms)
f = 5 Hz to 5 MHz		3.0			3.0			3.0		mV (rms)
OUTPUT										
Output Voltage Swing	±10	±13		±10	±13		±10	±13		V
Output Impedance (f ≤ 1 kHz)		1			1			1		Ω
Output Offset Voltage		±40				**±30**			**±30**	mV
Output Offset Voltage vs. Temperature		0.7			0.7				**2.0**	mV/°C
Output Offset Voltage vs. Supply		±2.5			±2.5			±2.5		mV/%
INPUT AMPLIFIERS (X, Y, and Z)										
Signal Voltage Range (Diff. or CM Operating Diff)		±10			±10			±10		V
CMRR	**40**			**50**			**50**			dB
Input Bias Current										
X, Y Inputs		3			1.5	**4**		1.5	**4**	µA
X, Y Inputs T_{MIN} to T_{MAX}		10			8			8		µA
Z Input		±10			±5	**±15**		±5	**±15**	µA
Z Input T_{MIN} to T_{MAX}		±30			±25			±25		µA
Offset Current		±0.3			±0.1			±0.1		µA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		10 V Z/($X_1 - X_2$)			10 V Z/($X_1 - X_2$)			10 V Z/($X_1 - X_2$)		
Total Error										
(V_X = –10 V, –10 V ≤ V_Z ≤ +10 V)		±2			±1			±1		%
(V_X = –1 V, –10 V ≤ V_Z ≤ +10 V)		±4			±3			±3		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10\,V}$			$\frac{(X_1-X_2)^2}{10\,V}$			$\frac{(X_1-X_2)^2}{10\,V}$		
Total Error		±0.8			±0.4			±0.4		%
SQUARE ROOTER PERFORMANCE										
Transfer Function		$-\sqrt{10\,V\,Z}$			$-\sqrt{10\,V\,Z}$			$-\sqrt{10\,V\,Z}$		
Total Error (0 V ≤ V_Z ≤ 10 V)		±1.5			±1.0			±1.0		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±10		**±18**	±10		**±18**	±10		±22	V
Supply Current										
Quiescent		**4**	**6**		**4**	**6**		**4**	**6**	mA
PACKAGE OPTIONS										
TO-116 (D-14)	AD532JD			AD532KD			AD532SD			
TO-100 (H-10A)	AD532JH			AD532KH			AD532SH			
LCC (E-20A)							AD532SE/883B			

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

THERMAL CHARACTERISTICS

H-10A: θ_{JC} = 25°C/W; θ_{JA} = 150°C/W

E-20A: θ_{JC} = 22°C/W; θ_{JA} = 85°C/W

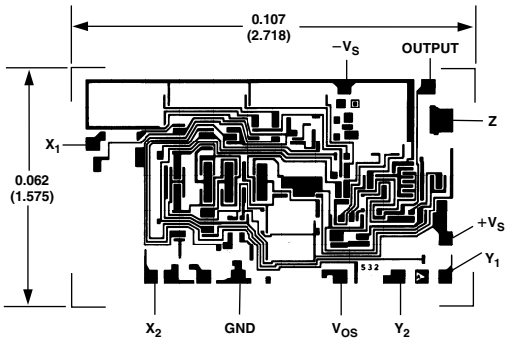
D-14: θ_{JC} = 22°C/W; θ_{JA} = 85°C/W

ORDERING GUIDE

Model	Temperature Ranges	Package Descriptions	Package Options
AD532JD	0°C to 70°C	Side Brazed DIP	D-14
AD532JD/+	0°C to 70°C	Side Brazed DIP	D-14
AD532KD	0°C to 70°C	Side Brazed DIP	D-14
AD532KD/+	0°C to 70°C	Side Brazed DIP	D-14
AD532JH	0°C to 70°C	Header	H-10A
AD532KH	0°C to 70°C	Header	H-10A
AD532JCHIPS	0°C to 70°C	Chip	
AD532SD	–55°C to +125°C	Side Brazed DIP	D-14
AD532SD/883B	–55°C to +125°C	Side Brazed DIP	D-14
JM38510/13903BCA	–55°C to +125°C	Side Brazed DIP	D-14
AD532SE/883B	–55°C to +125°C	LCC	E-20A
AD532SH	–55°C to +125°C	Header	H-10A
AD532SH/883B	–55°C to +125°C	Header	H-10A
JM38510/13903BIA	–55°C to +125°C	Header	H-10A
AD532SCHIPS	–55°C to +125°C	Chip	

CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown in Figure 1, and the complete schematic in Figure 2. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common-mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{OUT} = (X_1 - X_2)(Y_1 - Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{OS} in critical applications . . . otherwise the V_{OS} pin should be grounded.

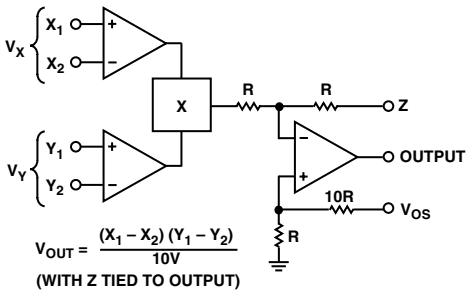


Figure 1. Functional Block Diagram

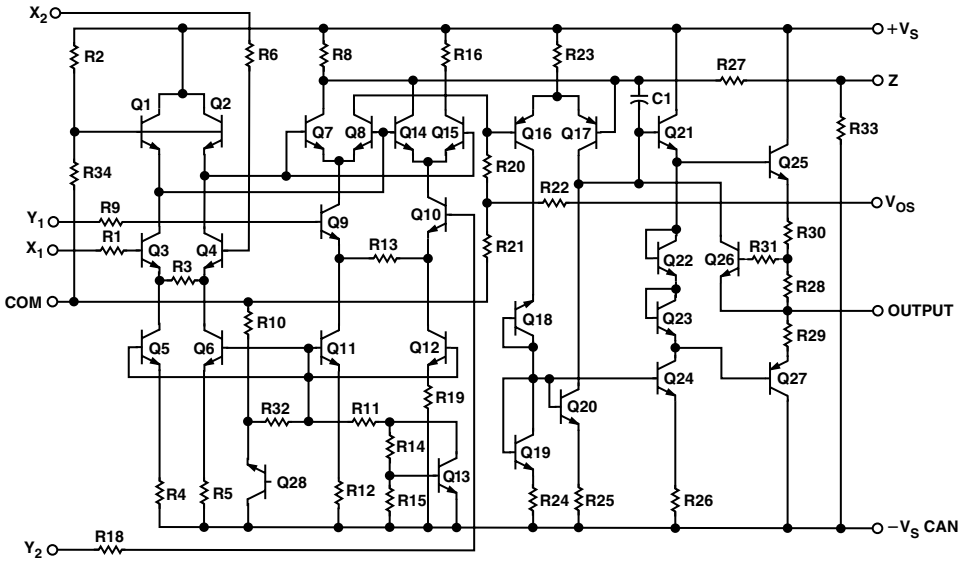


Figure 2. Schematic Diagram

AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at 25°C with the rated power supply. The value specified is in percent of full scale and includes X_{IN} and Y_{IN} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common-mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output op amp as shown in Figure 13. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwidth and other multiplier cell errors are adversely affected. The divide error and drift are then $\epsilon_m \times 10\ V/X_1 - X_2)$ where ϵ_m represents multiplier full-scale error and drift, and $(X_1–X_2)$ is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 3 and 4 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10 V dc. In Figure 4 the sine wave amplitude is 20 V (p-p).

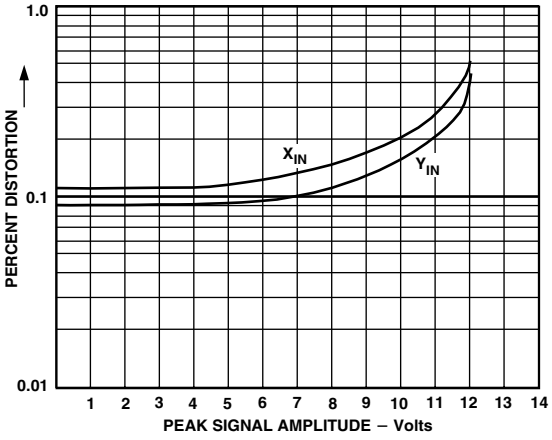


Figure 3. Percent Distortion vs. Input Signal

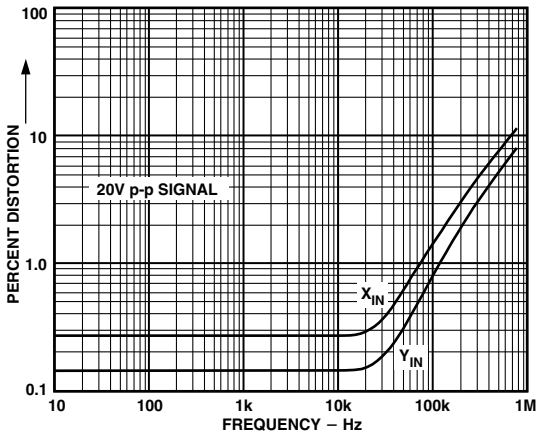


Figure 4. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 5. It is measured for the condition $V_X = 0$, $V_Y = 20$ V (p-p) and $V_Y = 0$, $V_X = 20$ V (p-p) over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

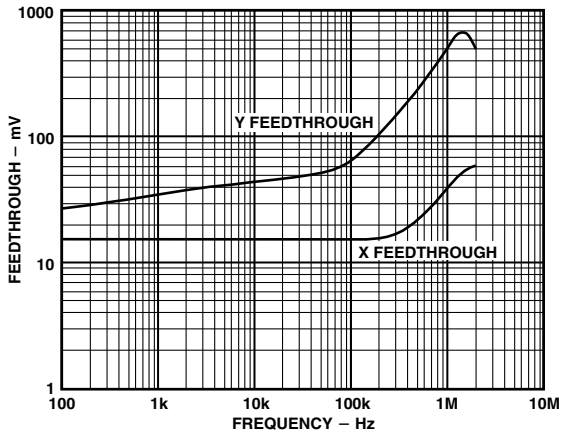


Figure 5. Feedthrough vs. Frequency

COMMON-MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common-mode rejection for both inputs as a function of frequency is shown in Figure 6. It is measured with $X_1 = X_2 = 20$ V (p-p), $(Y_1 – Y_2) = 10$ V dc and $Y_1 = Y_2 = 20$ V (p-p), $(X_1 – X_2) = 10$ V dc.

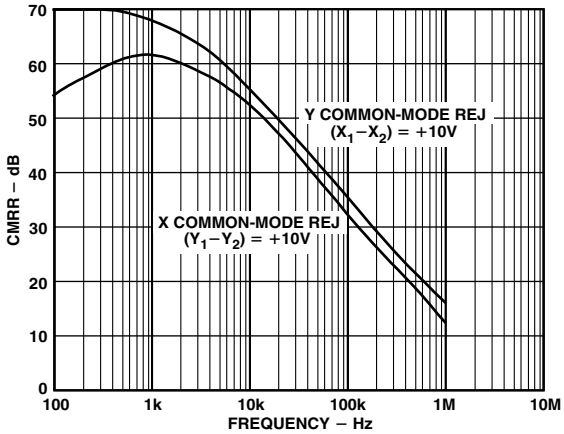


Figure 6. CMRR vs. Frequency

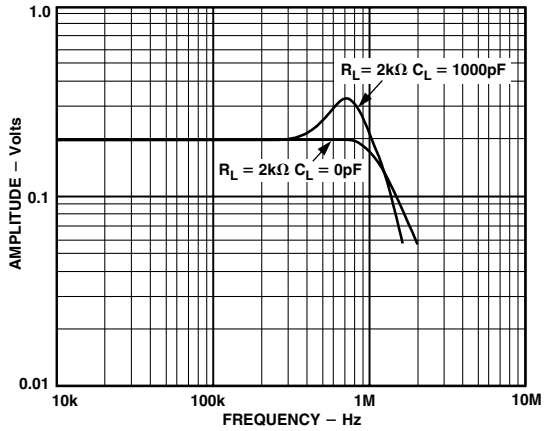


Figure 7. Frequency Response, Multiplying

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3 dB bandwidth of 1 MHz and rolls off at 6 dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 7. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 8.

Stable operation is maintained with capacitive loads to 1000 pF in all modes, except the square root for which 50 pF is a safe upper limit. Higher capacitive loads can be driven if a 100 Ω resistor is connected in series with the output for isolation.

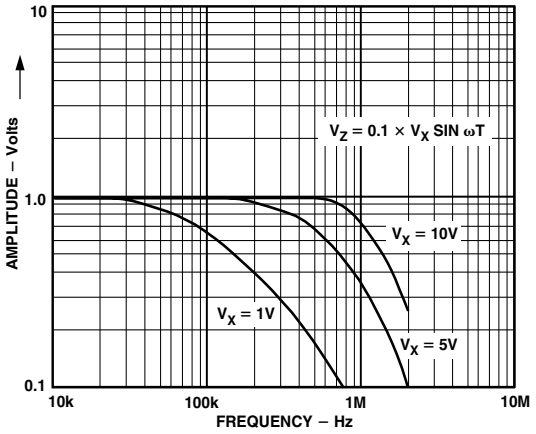


Figure 8. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15 V dc supplies, it may be operated at any supply voltage from ±10 V to ±18 V for the J and K versions, and ±10 V to ±22 V for the S version. The input and output signals must be reduced proportionately to prevent saturation; however, with supply voltages below ±15 V, as shown in Figure 9. Since power supply sensitivity is not dependent on external null networks as in other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

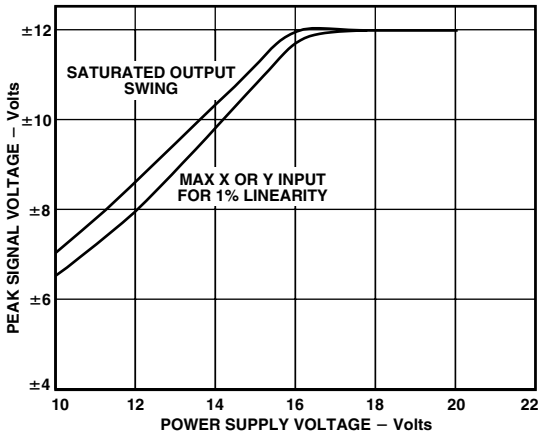


Figure 9. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532s are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 10.

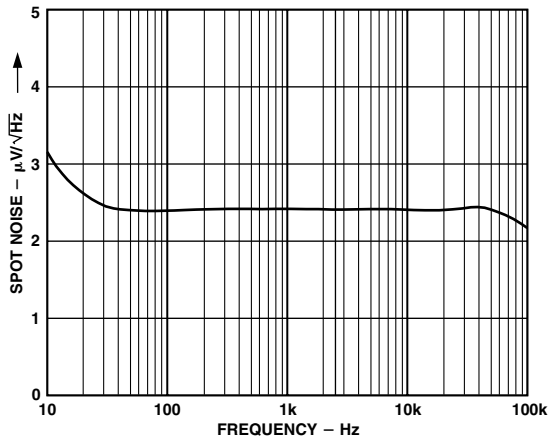


Figure 10. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin-film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

APPLICATIONS

MULTIPLICATION

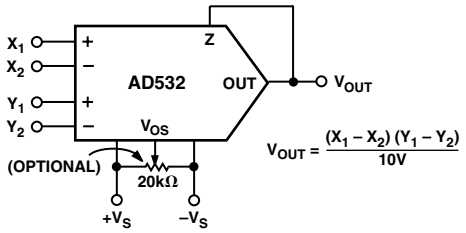


Figure 11. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 11. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see Figure 1). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

SQUARE

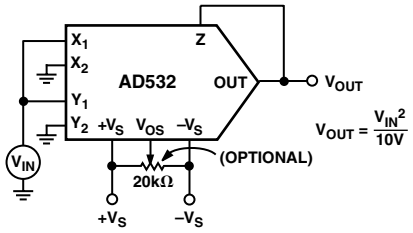


Figure 12. Squarer Connection

The squaring circuit in Figure 12 is a simple variation of the multiplier. The differential input capability of the AD532, however, can be used to obtain a positive or negative output response to the input . . . a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

DIVISION

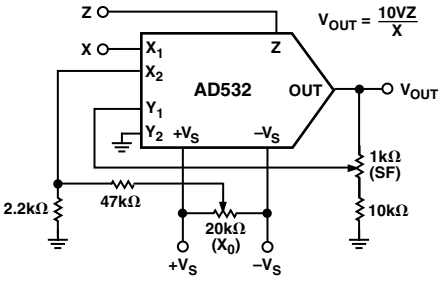


Figure 13. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 13. It should be noted, however, that the output error is given approximately by 10 V $\epsilon_m/(X_1 - X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \times (X_1 - X_2)/10$ V, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0 V to –10 V), connect the input to X and the offset null to X_2; for single-ended positive inputs (0 V to +10 V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

For practical reasons, the useful range in denominator input is approximately 500 mV ≤ $|(X_1 - X_2)|$ ≤ 10 V. The voltage offset adjust (V_{OS}), if used, is trimmed with Z at zero and $(X_1 - X_2)$ at full scale.

Table I. Adjust Procedure (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:		Adjust for:	With:	Adjust for:
Adjust	X	Z	V_{OUT}	Z	V_{OUT}
Scale Factor	–10 V	+10 V	–10 V	+10 V	–10 V
X_0 (Offset)	–1 V	+0.1 V	–1 V	+0.1 V	–1 V

Repeat if required.

SQUARE ROOT

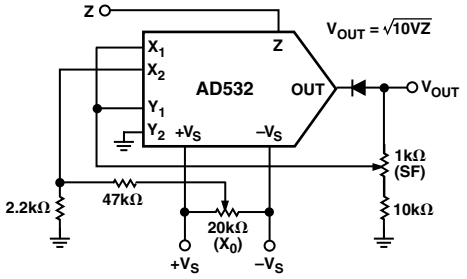


Figure 14. Square Rooter Connection

The connections for square root mode are shown in Figure 14. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{IN} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{IN} = +0.1 V dc, adjusting V_{OS} to obtain –1.0 V dc in the output, $V_{OUT} = -\sqrt{10\text{ V}\ Z}$. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

DIFFERENCE OF SQUARES

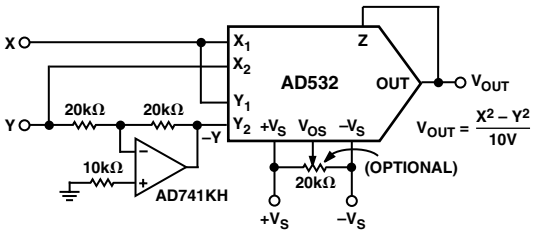


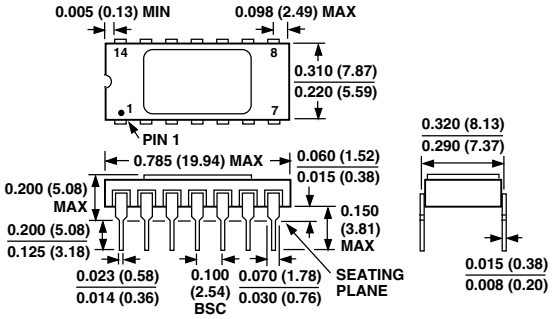
Figure 15. Differential of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X_2 - Y_2/10$ V. As shown in Figure 15, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{IN}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

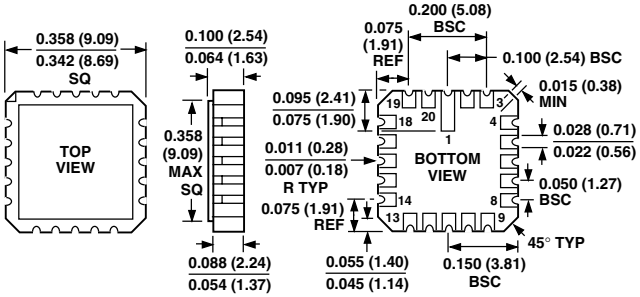
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

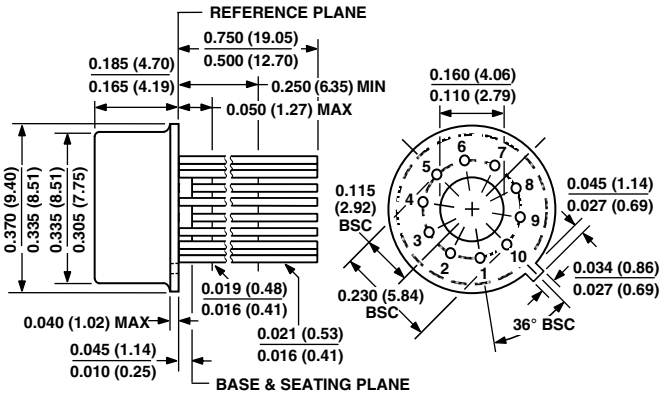
Side-Brazed DIP
(D-14)



Leadless Chip Carrier
(E-20A)



Metal Can
(H-10A)



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