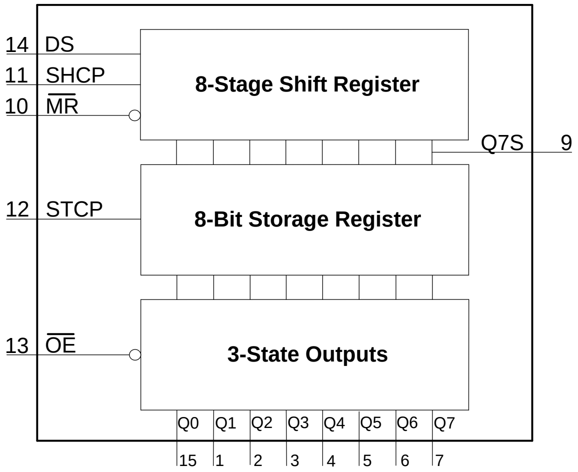
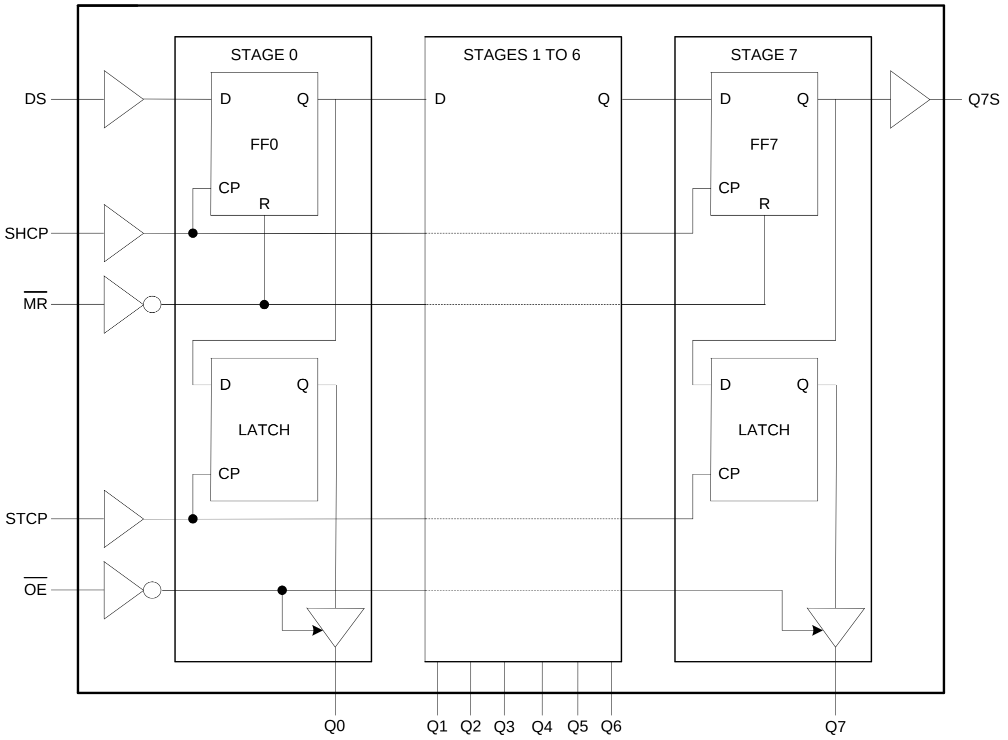
Pin Descriptions

Pin Number	Pin Name	Function
1	Q1	Parallel Data Output 1
2	Q2	Parallel Data Output 2
3	Q3	Parallel Data Output 3
4	Q4	Parallel Data Output 4
5	Q5	Parallel Data Output 5
6	Q6	Parallel Data Output 6
7	Q7	Parallel Data Output 7
8	GND	Ground
9	Q7S	Serial Data Output
10	$\overline{MR}$	Master Reset Input
11	SHCP	Shift Register Clock Input
12	STCP	Storage Register Clock Input
13	$\overline{OE}$	Output Enable Input
14	DS	Serial Data Input
15	Q0	Parallel Data Output 0
16	V_{CC}	Supply Voltage

Functional Diagram



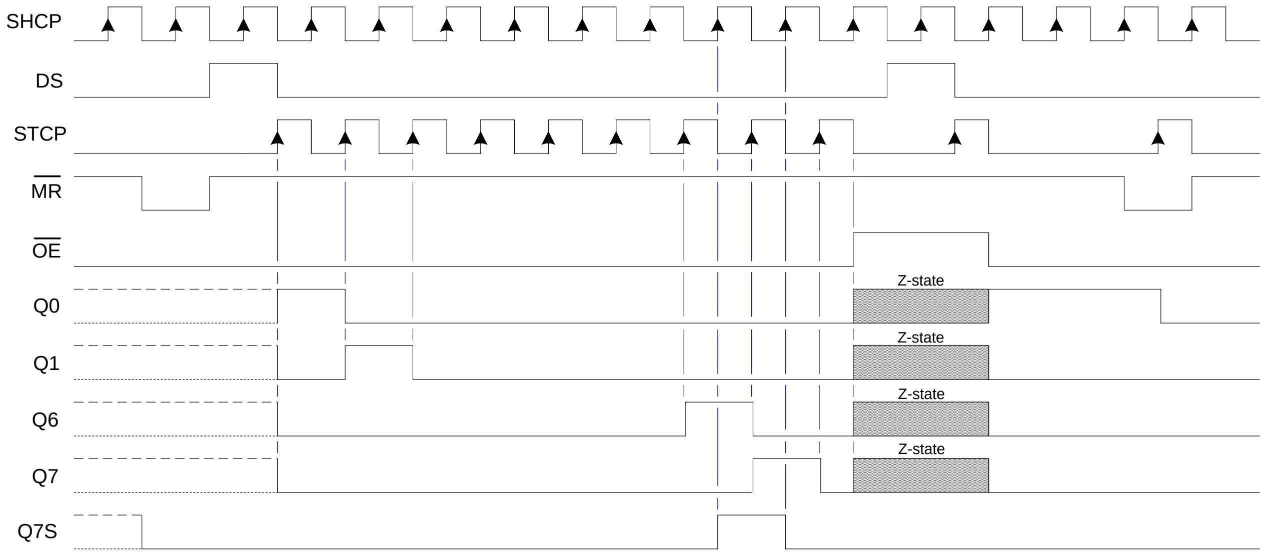
Logic Diagram



Functional Description and Timing Diagram

Control				Input	Output		Function
SHCP	STCP	$\overline{\text{OE}}$	$\overline{\text{MR}}$	DS	Q7S	Qn	
X	X	L	L	–	L	NC	Low-level asserted on MR clears shift register. Storage register is unchanged.
X	↑	L	L	–	L	L	Empty shift register transferred to storage register.
X	X	H	L	–	L	Z	Shift register remains clear; All Q ouputs in Z state.
↑	X	L	H	–	Q6S	NC	HIGH is shifted into first stage of Shift Register Contents of each register shifted to next register. The content of Q6S has been shifted to Q7S and now appears on device pin Q7S.
X	↑	L	H	–	NC	QnS	Contents of shift register copied to storage register. With output now in active state the storage resister contents appear on Q outputs.
↑	↑	L	H	–	Q6S	QnS	Contents of shift register copied to output register then shift register shifted.

H=HIGH Voltage State
L=LOW Voltage State
↑=LOW to HIGH Transition
X= Don'T Care – High or Low (Not Floating)
NC= No Change
Z= High-Impedance State



Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Description		Rating	Unit
ESD HBM	Human Body Model ESD Protection		2	kV
ESD CDM	Charged Device Model ESD Protection		1	kV
ESD MM	Machine Model ESD Protection		200	V
V_{CC}	Supply Voltage Range		-0.5 to +7.0	V
V_I	Input Voltage Range		-0.5 to +7.0	V
V_o	Voltage Applied to Output in High or Low State		-0.3 to V_{CC} +0.5	V
I_{IK}	Input Clamp Current $V_I < -0.5V$		-20	mA
I_{IK}	Input Clamp Current $V_I > V_{CC}$ +0.5V		20	mA
I_{OK}	Output Clamp Current $V_O < -0.5V$		-20	mA
I_{OK}	Output Clamp Current $V_O > V_{CC}$ +0.5V		20	mA
I_O	Continuous Output Current	Q7 Standard Output	±25	mA
		Qn Bus Driver Outputs	±35	mA
I_{CC}	Continuous Current through Vdd or GND		70	mA
I_{GND}	Continuous Current through Vdd or GND		-70	mA
T_J	Operating Junction Temperature		-40 to +150	°C
T_{STG}	Storage Temperature		-65 to +150	°C
P_{TOT}	Total Power Dissipation		500	mW

Note: 4. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 5) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	–	2.0	6.0	V
V_I	Input Voltage	–	0	V_{CC}	V
V_O	Output Voltage	Active Mode	0	V_{CC}	V
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 2.0V	–	1000	ns/V
		V_{CC} = 4.5V	–	500	
		V_{CC} = 6.0V	–	400	–
T_A	Operating Free-Air Temperature	–	-40	+125	°C

Note: 5. Unused inputs should be held at V_{CC} or Ground.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	V_{CC}	T_A = +25°C			T_A = -40°C to +85°C		T_A = -40°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage	–	2.0V	1.5	1.2	–	1.5	–	1.5	–	V
		–	4.5V	3.15	2.4	–	3.15	–	3.15	–	
		–	6.0V	4.2	3.2	–	4.2	–	4.2	–	
V_{IL}	Low-Level Input Voltage	–	2.0V	–	0.8	0.5	–	0.5	–	0.5	V
		–	4.5V	–	2.1	1.35	–	1.35	–	1.35	
		–	6.0V	–	2.8	1.8	–	1.8	–	1.8	
V_{OH}	High-Level Output Voltage	I_{OH} = -20µA All Outputs	2.0V	1.9	2.0	–	1.9	–	1.9	–	V
			4.5V	4.4	4.5	–	4.4	–	4.4	–	
			6.0V	5.9	6.0	–	5.9	–	5.9	–	
	Q7S Output	I_{OH} = -4.0mA	4.5V	3.84	4.32	–	4.32	–	3.7	–	
		I_{OH} = -5.2mA	6.0V	5.34	5.81	–	5.81	–	5.2	–	
	Qn Bus Outputs	I_{OH} = -6.0mA	4.5V	3.84	4.32	–	4.32	–	3.7	–	
		I_{OH} = -7.8mA	6.0V	5.34	5.81	–	5.81	–	5.2	–	
V_{OL}	Low-Level Output Voltage	I_{OL} = 20µA All Outputs	2.0V	–	0	0.1	–	0.1	–	0.1	V
			4.5V	–	0	0.1	–	0.1	–	0.1	
			6.0V	–	0	0.1	–	0.1	–	0.1	
	Q7S Output	I_{OL} = 4.0mA	4.5V	–	.15	0.33	–	0.33	–	0.4	
		I_{OL} = 5.2mA	6.0V	–	.16	0.33	–	0.33	–	0.4	
	Qn Bus Outputs	I_{OL} = 6.0mA	4.5V	–	.15	0.33	–	0.33	–	0.4	
		I_{OL} = 7.8mA	6.0V	–	.16	0.33	–	0.33	–	0.4	
I_I	Input Current	V_I =GND to 5.5V	6.0V	–	–	±0.1	–	± 1	–	± 1	µA
I_{OZ}	OFF-State Output Current	Qn Internal High or Low Vo = V_{CC} or GND	6.0V	–	–	± 5	–	± 5	–	± 10	µA
I_{CC}	Supply Current	V_I = GND or V_{CC} I_O = 0	6.0V	–	–	8.0	–	80	–	160	µA
C_i	Input Capacitance	V_I = V_{CC} or GND	6.0V	–	4	10	–	10	–	10	pF

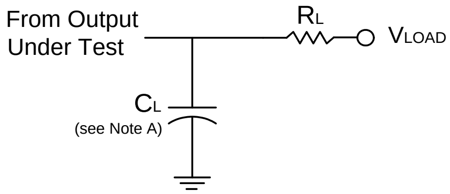
Operating Characteristics (@T_A = +25°C, unless otherwise specified.)

Parameter		Test Conditions	V_{CC} = 5V	Unit
			Typ	
C_{pd}	Power Dissipation Capacitance	f = 1 MHz All Outputs Switching-No Load	43	pF

Switching Characteristics

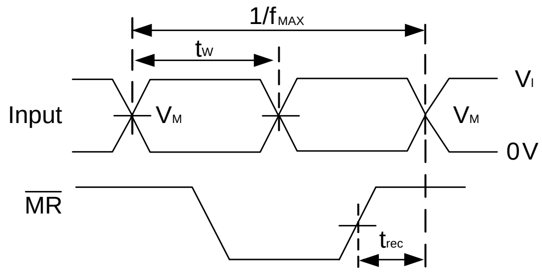
Symbol / Parameter	Pins	Test Conditions	V_{CC}	T_A = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
f_{MAX} Maximum Frequency	SHCP or STCP	Figure 1	2.0V	9	30	–	4.8	–	4	–	MHz
			4.5V	30	91	–	24	–	20	–	
			6.0V	35	108	–	28	–	24	–	
t_W Pulse Width	SHCP HIGH or LOW	Figure 1	2.0V	75	17	–	95	–	110	–	ns
			4.5V	15	6	–	19	–	22	–	
			6.0V	13	5	–	16	–	19	–	
	STCP HIGH or LOW	Figure 1	2.0V	75	11	–	95	–	110	–	
			4.5V	15	4	–	19	–	22	–	
			6.0V	13	3	–	16	–	19	–	
	$\overline{\text{MR}}$ LOW	Figure 1	2.0V	75	17	–	95	–	110	–	
			4.5V	15	6	–	19	–	22	–	
			6.0V	13	5	–	16	–	19	–	
t_{SU} Set-up Time	DS to SHCP	Figure 1	2.0V	50	11	–	65	–	75	–	ns
			4.5V	10	4	–	13	–	15	–	
			6.0V	9	3	–	11	–	13	–	
	SHCP tp STCP	Figure 1	2.0V	75	22	–	95	–	110	–	ns
			4.5V	15	8	–	19	–	22	–	
			6.0V	13	7	–	16	–	19	–	
t_H Hold Time	DS to SHCP	Figure 1	2.0V	3	-6	–	3	–	3	–	ns
			4.5V	3	-2	–	3	–	3	–	
			6.0V	3	-2	–	3	–	3	–	
t_{REC} Recovery Time	$\overline{\text{MR}}$ to SHCP	Figure 1	2.0V	50	-19	–	65	–	75	–	ns
			4.5V	10	-7	–	13	–	15	–	
			6.0V	9	-6	–	11	–	13	–	
t_{PD} Propagation Delay	SHCP to Q7S	Figure 1 C_L=50pF	2.0V	–	52	160	–	200	–	240	ns
			4.5V	–	19	32	–	40	–	48	
			6.0V	–	15	27	–	34	–	41	
	STCP to Qn	Figure 1 C_L=50pF	2.0V	–	55	175	–	220	–	265	ns
			4.5V	–	20	35	–	44	–	53	
			6.0V	–	16	30	–	37	–	45	
t_{PHL} Propagation Delay	$\overline{\text{MR}}$ to Q7S	Figure 1 C_L=50pF	2.0V	–	47	175	–	220	–	265	ns
			4.5V	–	17	35	–	44	–	53	
			6.0V	–	14	30	–	37	–	45	
t_{EN} Enable Time	$\overline{\text{OE}}$ to Qn	Figure 1 C_L=50pF	2.0V	–	47	150	–	190	–	225	ns
			4.5V	–	17	30	–	38	–	45	
			6.0V	–	14	26	–	33	–	38	
t_{DIS} Disable Time	$\overline{\text{OE}}$ to Qn	Figure 1 C_L=50pF	2.0V	–	41	150	–	190	–	225	ns
			4.5V	–	15	30	–	38	–	45	
			6.0V	–	12	26	–	33	–	38	

Parameter Measurement Information

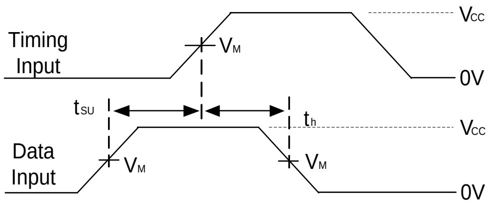


TEST	V_{LOAD}
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

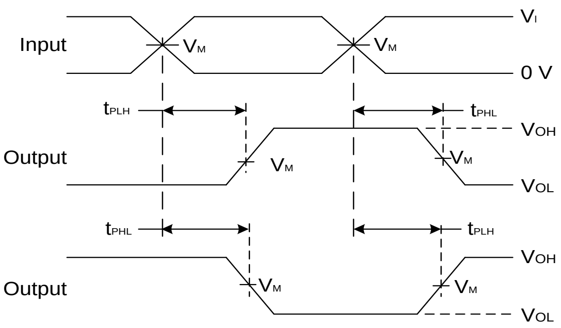
V_{CC}	Inputs		V_M	C_L
	V_I	t_r/t_f		
2.0V	V_{CC}	6ns	$V_{CC}/2$	50pF
4.5V	V_{CC}	6ns	$V_{CC}/2$	50pF
6.0V	V_{CC}	6ns	$V_{CC}/2$	50pF



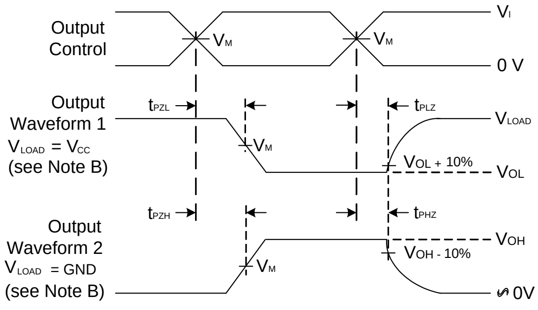
Voltage Waveform
Pulse Duration and Recovery Time



Voltage Waveform
Set-up and Hold Times



Voltage Waveform
Propagation Delay Times
Inverting and Non Inverting Outputs

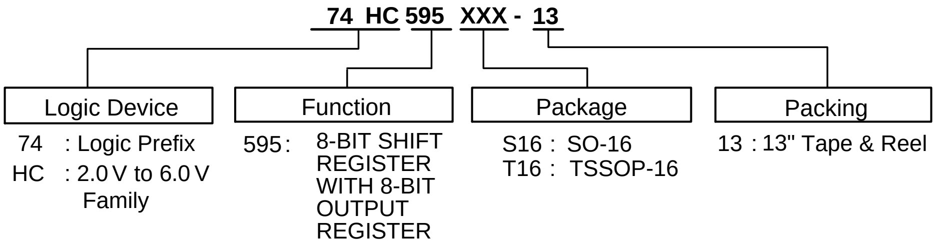


Voltage Waveform
Enable and Disable Times

Notes:
- A. Includes test lead and test apparatus capacitance.
- B. Output Waveform 1 depends on the internal Q_N node being low and behaves in this manner based on OE pin.
  Output Waveform 2 depends on the internal Q_N node being high and behaves in this manner based on OE pin.
- C. All pulses are supplied at pulse repetition rate ≤ 10MHz.
- D. Inputs are measured separately one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{PD}.

Figure 1. Load Circuit and Voltage Waveforms

Ordering Information

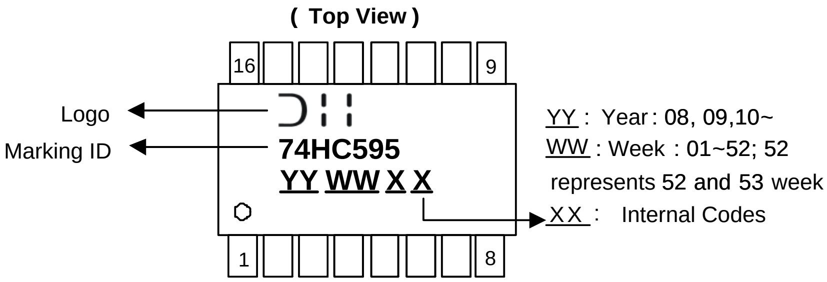


Part Number	Package Code	Packaging	7" Tape and Reel (Note 6)	
			Quantity	Part Number Suffix
74HC595S16-13	S16	SO-16	2500/Tape & Reel	-13
74HC595T16-13	T16	TSSOP-16	2500/Tape & Reel	-13

Note: 6. The taping orientation is located on our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information

(1) SO-16, TSSOP16

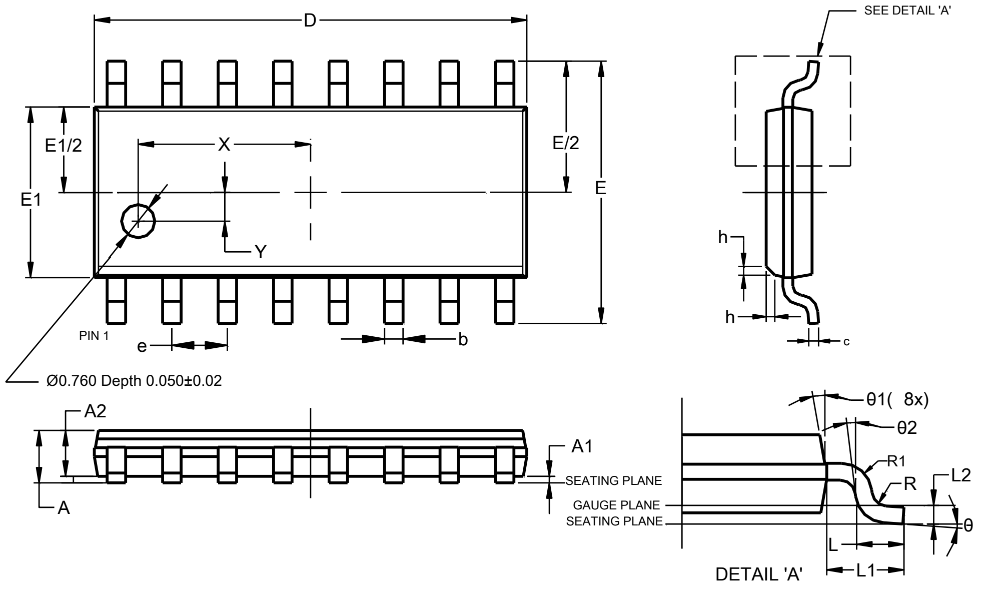


Part Number	Package
74HC595S16	SO-16
74HC595T16	TSSOP-16

Package Outline Dimensions (All dimensions in mm.)

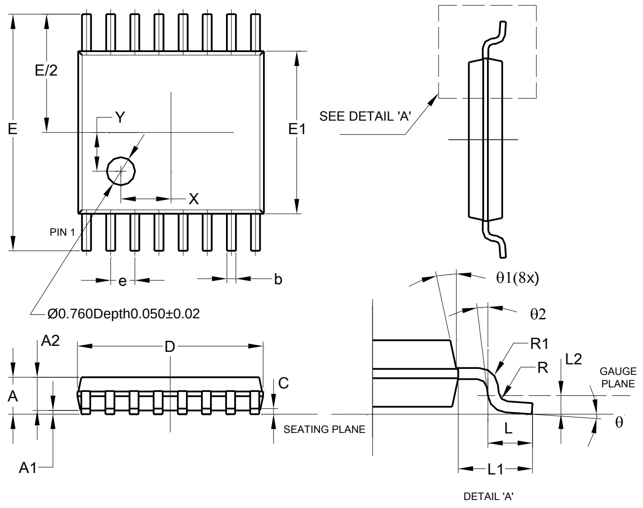
Please see http://www.diodes.com/package-outlines.html for the latest version.

Package Type: SO-16



SO-16			
Dim	**Min**	**Max**	**Typ**
A	--	1.260	--
A1	0.10	0.23	--
A2	1.02	--	--
b	0.31	0.51	--
c	0.10	0.25	--
D	9.80	10.00	--
E	5.90	6.10	--
E1	3.80	4.00	--
e	1.27 BSC		
h	0.15	0.25	0.20
L	0.40	1.27	--
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	--	--
R1	0.07	--	--
X	3.945 REF		
Y	0.661 REF		
θ	0°	8°	--
θ1	5°	15°	--
θ2	0°	--	--
All Dimensions in mm			

Package Type: TSSOP-16

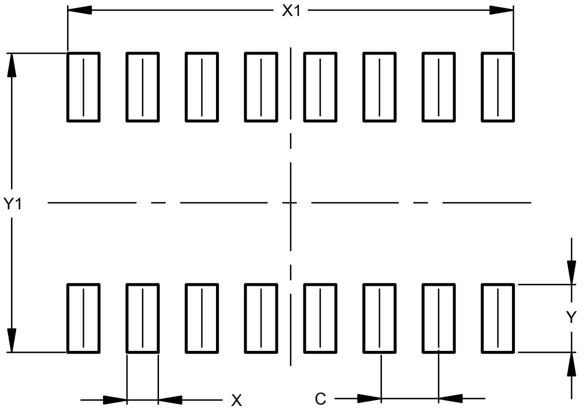


TSSOP-16			
Dim	**Min**	**Max**	**Typ**
A	-	1.08	-
A1	0.05	0.15	-
A2	0.80	0.93	-
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	-
E	6.40 BSC		
E1	4.30	4.50	-
e	0.65 BSC		
L	0.45	0.75	-
L1	1.00 REF		
L2	0.25 BSC		
R / R1	0.09	-	-
X	-	-	1.350
Y	-	-	1.050
θ	0°	8°	-
θ1	5°	15°	-
θ2	0°	-	-
All Dimensions in mm			

Suggested Pad Layout

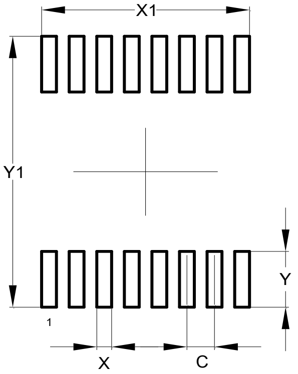
Please see http://www.diodes.com/package-outlines.html for the latest version.

Package Type: SO-16



Dimensions	Value (in mm)
C	1.270
X	0.670
X1	9.560
Y	1.450
Y1	6.400

Package Type: TSSOP-16



Dimensions	Value (in mm)
C	0.650
X	0.350
X1	4.900
Y	1.400
Y1	6.800

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