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1.0 GENERAL DESCRIPTION

The USB2227/USB2228 is a USB 2.0 Bulk Only Mass Storage Class Peripheral Controller intended for supporting CompactFlash (CF and CF Ultra I/II) in True IDE Mode only, SmartMedia (SM) and XD cards, Memory Stick (MS), Memory Stick DUO (MSDUO) and Memory Stick Pro (MSPRO), Secure Digital (SD), and MultiMediaCard (MMC) flash memory devices. It provides a single chip solution for the most popular flash memory cards in the market.

The device consists of a USB 2.0 PHY and SIE, buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, and CF, MS, SM and SD controllers. The SD controller supports both SD and MMC devices. SM controller supports both SM and xD cards.

Provisions for external Flash Memory up to 64K bytes for program storage is provided.

12K bytes of scratchpad SRAM and 768 Bytes of program SRAM are also provided.

Fifteen GPIO pins are provided for indicators, external serial EEPROM for OEM id and system configuration information, and other special functions.

Internal power FETs are provided to directly supply power to the xD/SM, MMC/SD and MS/MSPro cards.

The internal ROM program is capable of implementing any combination of single or multi-LUN CF/SD/MMC/SM/MS reader functions with individual card power control and activity indication. Microchip also provides licenses** for Win98 and Win2K drivers and setup utilities. Note: Please check with Microchip for precise features and capabilities for the current ROM code release.

1.1 Acronyms

SM: SmartMedia

SMC: SmartMedia Controller

FM: Flash Media

FMC: Flash Media Controller

CF: Compact Flash

CFC: CompactFlash Controller

SD: Secure Digital

SDC: Secure Digital Controller

MMC: MultiMediaCard

MS: Memory Stick

MSC: Memory Stick Controller

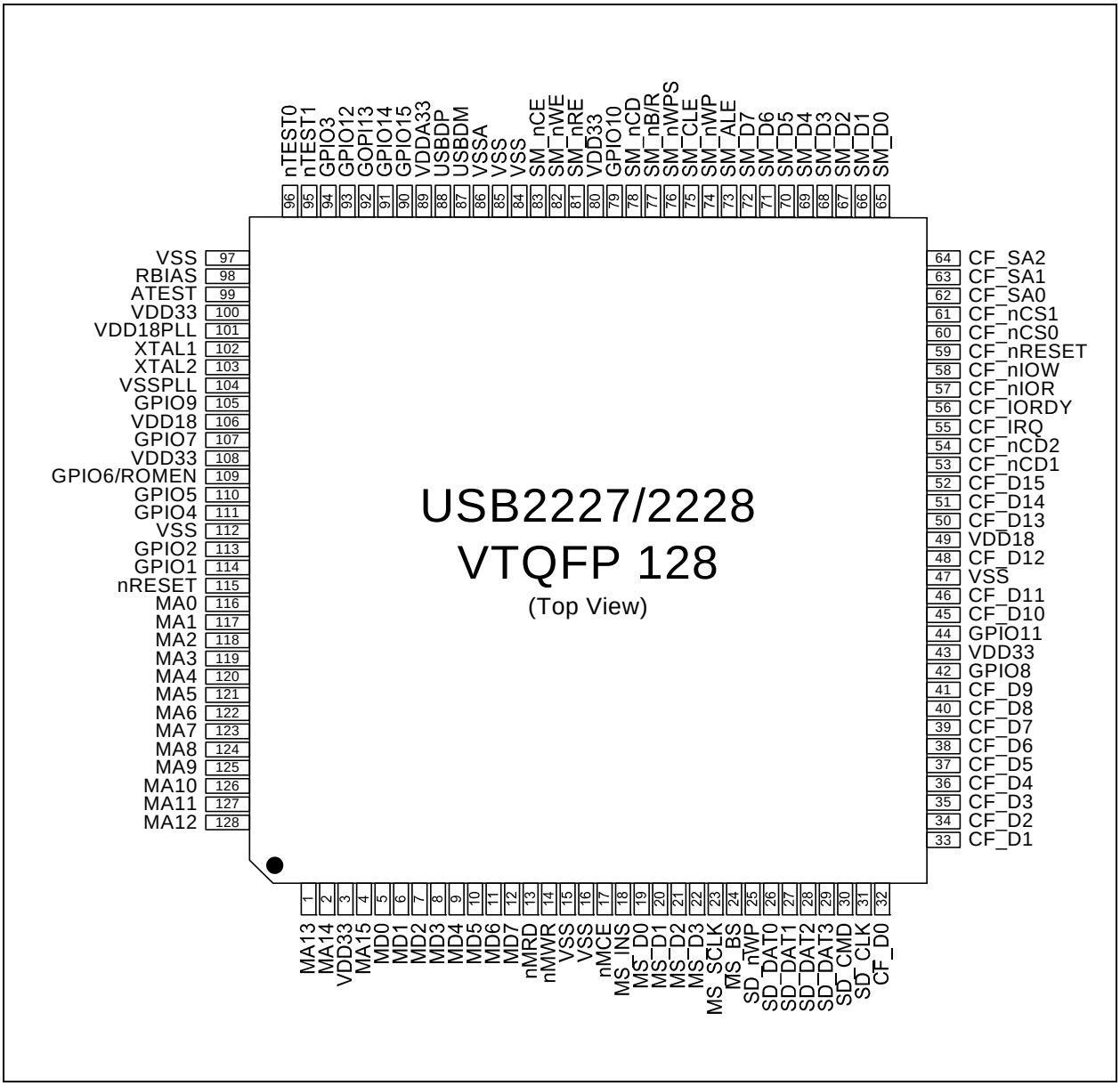
TPC: Transport Protocol Code.

ECC: Error Checking and Correcting

CRC: Cyclic Redundancy Checking

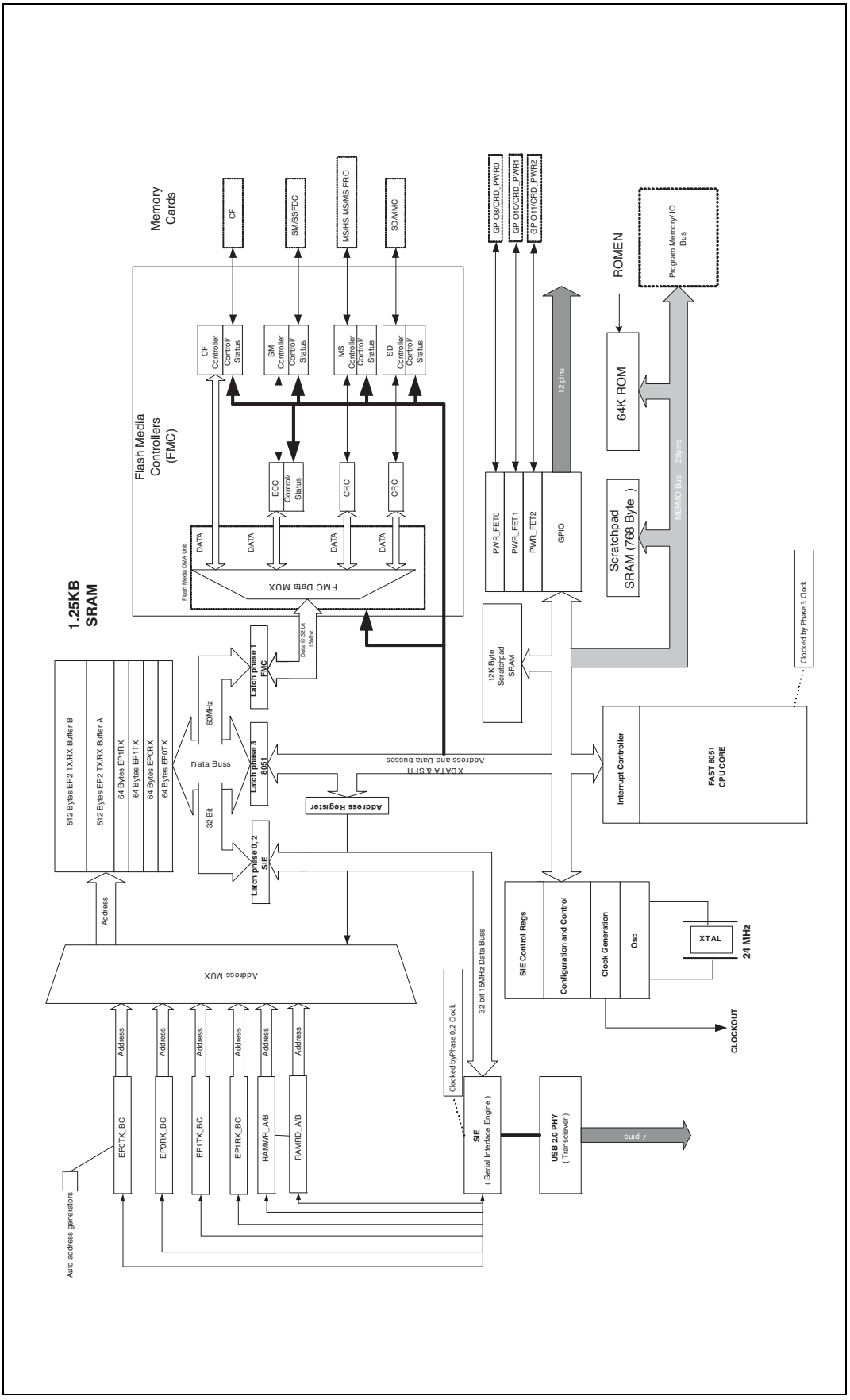
2.0 PIN CONFIGURATION

FIGURE 2-1: USB2227/USB2228 128-PIN VTQFP



3.0 BLOCK DIAGRAM

FIGURE 3-1: USB2227/USB2228 BLOCK DIAGRAM



4.0 PIN DESCRIPTIONS

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

4.1 PIN Descriptions

Symbol	128-Pin VTQFP	Buffer Type	Description
CompactFlash (In True IDE Mode) Interface			
CF_nCS1	61	O8PU	CF Chip Select 1: This pin is the active low chip select 1 signal for the CF ATA device.
CF_nCS0	60	O8PU	CF Chip Select 0: This pin is the active low chip select 0 signal for the task file registers of CF ATA device in the True IDE mode.
CF_SA2	64	O8	CF Register Address 2: This pin is the register select address bit 2 for the CF ATA device.
CF_SA1	63	O8	CF Register Address 1: This pin is the register select address bit 1 for the CF ATA device.
CF_SA0	62	O8	CF Register Address 0: This pin is the register select address bit 0 for the CF ATA device.
CF_IRQ	55	IPD	CF Interrupt: This is the active high interrupt request signal from the CF device.
CF_D[15:8]	52 51 50 48 46 45 41 40	I/O8PD	CF Data 15-8: The bi-directional data signals CF_D15-CF_D8 in True IDE mode data transfer. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. The bi-directional data signal has an internal weak pull-down resistor.
CF_D[7:0]	39 38 37 36 35 34 33 32	I/O8PD	CF Data 7-0: The bi-directional data signals CF_D7-CF_D0 in the True IDE mode data transfer. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. The bi-directional data signal has an internal weak pull-down resistor.
CF_IORDY	56	IPU	IO Ready: This pin is active high input signal. This pin has an internally controlled weak pull-up resistor.

Symbol	128-Pin VTQFP	Buffer Type	Description
CF_nCD2	54	IPU	CF Card Detection2: This card detection pin is connected to the ground on the CF device, when the CF device is inserted. This pin has an internally controlled weak pull-up resistor.
CF_nCD1	53	IPU	CF Card Detection1: This card detection pin is connected to ground on the CF device, when the CF device is inserted. This pin has an internally controlled weak pull-up resistor.
CF_nRESET	59	O8	CF Hardware Reset: This pin is an active low hardware reset signal to CF device.
CF_nIOR	57	O8	CF IO Read: This pin is an active low read strobe signal for CF device.
CF_nIOW	58	O8	CF IO Write Strobe: This pin is an active low write strobe signal for CF device.
SmartMedia Interface			
SM_nWP	74	O8PD	SM Write Protect: This pin is an active low write protect signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.
SM_ALE	73	O8PD	SM Address Strobe: This pin is an active high Address Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.
SM_CLE	75	O8PD	SM Command Strobe: This pin is an active high Command Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.
SM_D[7:0]	72 71 70 69 68 67 66 65	I/O8PD	SM Data 7-0: These pins are the bi-directional data signal SM_D7-SM_D0. The bi-directional data signal has an internal weak pull-down resistor.
SM_nRE	81	08PU	SM Read Enable: This pin is an active low read strobe signal for SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).

Symbol	128-Pin VTQFP	Buffer Type	Description
SM_nWE	82	O8PU	SM Write Enable: This pin is an active low write strobe signal for SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM_nWPS	76	IPU	SM Write Protect Switch: A write-protect seal is detected, when this pin is low. This pin has an internally controlled weak pull-up resistor.
SM_nB/R	77	I	SM Busy or Data Ready: This pin is connected to the BSY/RDY pin of the SM device. An external pull-up resistor is required on this signal. The pull-up resistor must be pulled up to the same power source that powers the SM/NAND flash device.
SM_nCE	83	O8PU	SM Chip Enable: This pin is the active low chip enable signal to the SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM_nCD	78	IPU	SM Card Detection: This is the card detection signal from SM device to indicate if the device is inserted. This pin has an internally controlled weak pull-up resistor.
Memory Stick Interface			
MS_BS	24	O8	MS Bus State: This pin is connected to the BS pin of the MS device. It is used to control the Bus States 0, 1, 2 and 3 (BS0, BS1, BS2 and BS3) of the MS device.
MS_SDIO/MS_D0	19	I/O8PD	MS System Data In/Out: This pin is a bi-directional data signal for the MS device. Most significant bit (MSB) of each byte is transmitted first by either MSC or MS device. The bi-directional data signal has an internal weak pull-down resistor.
MS_D1	20	I/O8PD	MS System Data In/Out: This pin is a bi-directional data signal for the MS device. This pin has internally controlled weak pull-up and pull-down resistors for various operational modes.

Symbol	128-Pin VTQFP	Buffer Type	Description
MS_D[3:2]	22 21	I/O8PD	MS System Data In/Out: This pin is a bi-directional data signal for the MS device. The bi-directional data signal has an internal weak pull-down resistor.
MS_INS	18	IPU	MS Card Insertion: This pin is the card detection signal from the MS device to indicate, if the device is inserted. This pin has an internally controlled weak pull-up resistor.
MS_SCLK	23	O8	MS System CLK: This pin is an output clock signal to the MS device. The clock frequency is software configurable.
SD Interface			
SD_DAT[3:0]	29 28 27 26	I/O8PU	SD Data 3-0: These are bi-directional data signals. These pins have internally controlled weak pull-up resistors.
SD_CLK	31	O8	SD Clock: This is an output clock signal to SD/MMC device. The clock frequency is software configurable.
SD_CMD	30	I/O8PU	SD Command: This is a bi-directional signal that connects to the CMD signal of SD/MMC device. This pin has an internally controlled weak pull-up resistor.
SD_nWP	25	IPD	SD Write Protected: This pin is an input signal with an internal weak pull-down. This pin has an internally controlled weak pull-down resistor.
USB Interface			
USBDM USBDP	87 88	IO-U	USB Bus Data: These pins connect to the USB bus data signals.
RBIAS	98	I	USB Transceiver Bias: A 12.0kΩ, ± 1.0% resistor is attached from VSSA to this pin, in order to set the transceiver's internal bias currents.
ATEST	99	AIO	Analog Test: This signal is used for testing the analog section of the chip and should be connected to VDDA33 for normal operation.
VDD18PLL	101		1.8v Power for the PLL
VSSPLL	104		PLL Ground Reference: Ground Reference for 1.8v PLL power
VDDA33	89		3.3v Analog Power
VSSA	86		Analog Ground Reference: Analog Ground Reference for 3.3v Analog Power.

Symbol	128-Pin VTQFP	Buffer Type	Description
XTAL1/ CLKIN	102	ICLKx	Crystal Input/External Clock Input: 24Mhz Crystal or external clock input. This pin can be connected to one terminal of the crystal or can be connected to an external 24Mhz clock when a crystal is not used. **Note:** The MA[2:0] pins will be sampled while nRESET is asserted, and the value will be latched upon nRESET negation. This will determine the clock source and value.
XTAL2	103	OCLKx	Crystal Output: 24Mhz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.
Memory I/O Interface			
MD[7:0]	12 11 10 9 8 7 6 5	I/O8PU	Memory Data Bus: When ROMEN bit of GPIO_IN1 register = 0, these signals are used to transfer data between the internal CPU and the external program memory. These pins have internally controlled weak pull-up resistors.
MA[15:3]	4 2 1 128 127 126 125 124 123 122 121 120 119	O8	Memory Address Bus: These signals address memory locations within the external memory.
MA2/ SEL_CLKDRV	118	I/O8PD	Memory Address Bus: MA2 Addresses memory locations within the external memory. SEL_CLKDRV. During nRESET assertion, this pins will select the operating clock mode (crystal or externally driven clock source), and a weak pull-down resistor is enabled. When nRESET is negated, the value will be internally latched and this pin will revert to MA2 functionality, the internal pull-down will be disabled. ‘0’ = Crystal operation (24MHz only) ‘1’ = Externally driven clock source (24MHz or 48MHz) **Note:** If the latched value is ‘1’, then the MA2 pin is tri-stated when the following conditions are true: 1. IDLE bit (PCON.0) is 1. 2. INT2 is negated 3. SLEEP bit of CLOCK_SEL is 1. If the latched value is ‘0’, then the MA2 pin will function identically to the MA[15:3] pins at all times (other than during nRESET assertion).

Symbol	128-Pin VTQFP	Buffer Type	Description
MA[1:0]/CLK_SEL[1:0]	117 116	I/O8PD	Memory Address Bus: MA[1:0], These signals address memory locations within the external memory.
			SEL[1:0]. During nRESET assertion, these pins will select the operating frequency of the external clock, and the corresponding weak pull-down resistors are enabled. When nRESET is negated, the value on these pins will be internal latched and these pins will revert to MA[1:0] functionality, the internal pull-downs will be disabled. SEL[1:0] = '00'. 24MHz SEL[1:0] = '01'. RESERVED SEL[1:0] = '10'. RESERVED SEL[1:0] = '11'. 48MHz **Note:** If the latched value is '1', then the corresponding MA pin is tri-stated when the following conditions are true: 1. IDLE bit (PCON.0) is 1. 2. INT2 is negated 3. SLEEP bit of CLOCK_SEL is 1. If the latched value is '0', then the corresponding MA pin will function identically to the MA[15:3] pins at all times (other than during nRESET assertion).
nMWR	14	O8	Memory Write Strobe: Program Memory Write; active low
nMRD	13	O8	Memory Read Strobe: Program Memory Read; active low
nMCE	17	O8	Memory Chip Enable: Program Memory Chip Enable; active low. This signal is asserted, when any of the following conditions are no longer met: 1. IDLE bit (PCON.0) is 1. 2. INT2 is negated 3. SLEEP bit of CLOCK_SEL is 1. **Note:** This signal is held to a logic 'high' while nRESET is asserted.
MISC			
GPIO1	114	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO2	113	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO3	94	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO4	111	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.

Symbol	128-Pin VTQFP	Buffer Type	Description
GPIO5	110	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO6/ ROMEN	109	IPU	GPIO6, ROMEN: This pin has an internal weak pull-up resistor that is enabled or disabled by the state of nRESET. The pull-up is enabled when nRESET is active. The pull-up is disabled, when the nRESET is inactive (some clock cycles later, after the rising edge of nRESET). The state of this pin is latched internally on the rising edge of nRESET to determine if internal or external program memory is used. The state latched is stored in ROMEN bit of GPIO_IN1 register.
		I/O8	After the rising edge of nRESET, this pin may be used as GPIO6 or RXD. When pulled low via an external weak pull-down resistor, an external program memory should be connected to the memory data bus. The USB2227/USB2228 uses this external bus for program execution. When this pin is left unconnected or pulled high by a weak pull-up resistor, the USB2227/USB2228 uses the internal ROM for program execution.
GPIO7	107	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO8/ CRD_PWR0	42	I/O8	General Purpose I/O or Card Power: GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 100mA.
GPIO9	105	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO10/ CRD_PWR1	79	I/O8	General Purpose I/O or Card Power: GPIO: These pins may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 100mA.
GPIO11/ CRD_PWR2	44	I/O8	General Purpose I/O or Card Power: GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 200mA.
GPIO[15:12]	90 91 92 93	I/O8	General Purpose I/O: These pins may be used either as input, or output.
nRESET	115	IS	RESET input: This active low signal is used by the system to reset the chip. The active low pulse should be at least 1µs wide.

Symbol	128-Pin VTQFP	Buffer Type	Description
nTEST[1:0]	95 96	I	TEST input: These signals are used for testing the chip. User should normally tie them high externally, if the test function is not used.
Digital Power, Grounds and no Connects			
VDD18	49 106		1.8v Digital Core Power: +1.8V Core power All VDD18 pins must be connected together on the circuit board.
VDD33	3 43 80 100 108		3.3v Power & Voltage Regulator Input: 3.3V Power & Regulator Input. Pins 100 & 108 supply 3.3V power to the internal 1.8V regulators.
VSS	15 16 47 84 85 97 112		Ground: Ground Reference

Note 1: Hot-insertion capable card connectors are required for all flash media. It is required for SD connector to have Write Protect switch. This allows the chip to detect MMC card.

2: nMCE is normally asserted except when the 8051 is in standby mode.

3: VDD18 (Pin 106) and VDD18PLL (Pin 101) must have a 10uF +/-20% Low-ESR (equivalent series resistance) <0.1 ohm bypass capacitor to VSSA. These capacitors must be as close to these pins as possible.

4.2 Buffer Type Descriptions

TABLE 4-1: USB2227/USB2228 BUFFER TYPE DESCRIPTIONS

Buffer	Description
I	Input
IPU	Input with internal weak pull-up resistor.
IPD	Input with internal weak pull-down resistor.
IS	Input with Schmitt trigger
I/O8	Input/Output buffer with 8mA sink and 8mA source.
I/O8PU	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.
I/O8PD	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
O8	Output buffer with 8mA sink and 8mA source.
O8PU	Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.
O8PD	Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Analog Input/Output Defined in USB specification
AIO	Analog Input/Output

5.0 DC PARAMETERS

5.1 Maximum Ratings

Parameter	Symbol	MIN	MAX	Units	Comments
Storage Temperature	T_A	-55	150	°C	
Lead Temperature			325	°C	Soldering < 10 seconds
3.3V supply voltage	V_{DD33}, V_{DDA33}	-0.5	4.0	V	
Voltage on GPIO3 & USBDP/DM pins		-0.5	(3.3V supply voltage + 2) ≤ 6	V	
Voltage on GPIO8,10&11		-0.5	V_{DD33} + 0.3	V	When internal power FET operation of these pins is enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63V indefinitely, without damage to the device as long as V_{DD33} and V_{DDA33} are less than 3.63V and T_A is less than 70°C.
Voltage on any signal pin		-0.5	V_{DD33} + 0.3	V	
Voltage on XTAL1		-0.5	4.0	V	
Voltage on XTAL2		-0.5	V_{DD18} + 0.3	V	

Note 1: Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

2: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

5.2 Recommended Operating Conditions

Parameter	Symbol	MIN	MAX	Units	Comments
Operating Temperature	T_A	0	70	°C	
3.3V supply voltage	V_{DD33}, V_{DDA33}	3.0	3.6	V	
Voltage on GPIO3 & USBDP/DM pins		-0.3	5.5	V	If any 3.3V supply voltage drops below 3.0V, then the MAX becomes: (3.3V supply voltage) + 0.5 ≤ 5.5
Voltage on any signal pin		-0.3	V_{DD33}	V	
Voltage on XTAL1		-0.3	V_{DDA33}	V	
Voltage on XTAL2		-0.3	V_{DD18}	V	

5.3 DC Electrical Characteristics

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
I,IPU & IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis	V_{HYSI}		500		mV	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	mA	V_{IN} = V_{DD33}

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
O8. O8PU & 08PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -8mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 5-1)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
I/O8, I/O8PU & I/O8PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} – 0.4			V	I_{OH} = -8 mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 5-1)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U (Note 5-2)						
Integrated Power FET for GPIO8 & GPIO10 (and GPIO11 when used with Firmware version -03 or older)						
Output Current	I_{OUT}	100			mA	GPIO8 or 10; $Vdrop_{FET}$ = 0.23V
Short Circuit Current Limit	I_{SC}			140	mA	GPIO8 or 10; $Vout_{FET}$ = 0V
On Resistance	R_{DSON}			2.1	Ω	GPIO8 or 10; I_{FET} = 70mA
Output Voltage Rise Time	t_{DSON}			800	µs	GPIO8 or 10; C_{LOAD} = 10µF

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Integrated Power FET for GPIO11 (only when used with Firmware version -04 or later)						
Output Current	I_{OUT}	200			mA	GPIO11; $Vdrop_{FET}$ = 0.46V
Short Circuit Current Limit	I_{SC}			181	mA	GPIO11; $Vout_{FET}$ = 0V
On Resistance	R_{DSON}			2.1	Ω	GPIO11; I_{FET} = 70mA
Output Voltage Rise Time	t_{DSON}			800	µs	GPIO11; C_{LOAD} = 10µF
Supply Current Unconfigured	I_{CCINIT}		55	80	mA	
Supply Current Active (Full Speed)	I_{CC}		75	90	mA	
Supply Current Active (High Speed)	I_{CC}		75	100	mA	
Supply Current Standby	I_{CSBY}		305	420	µA	

Note 5-1 Output leakage is measured with the current pins in high impedance.

Note 5-2 See Appendix A for USB DC electrical characteristics.

Note 5-3 The Maximum power dissipation parameters of the package should not be exceeded

Note 5-4 The assignment of each Integrated Card Power FET to a designated Card Connector is controlled by both firmware and the specific board implementation. Firmware will default to the settings listed in Table 7-1, “GPIO Usage (ROM Rev -11),” on page 20.

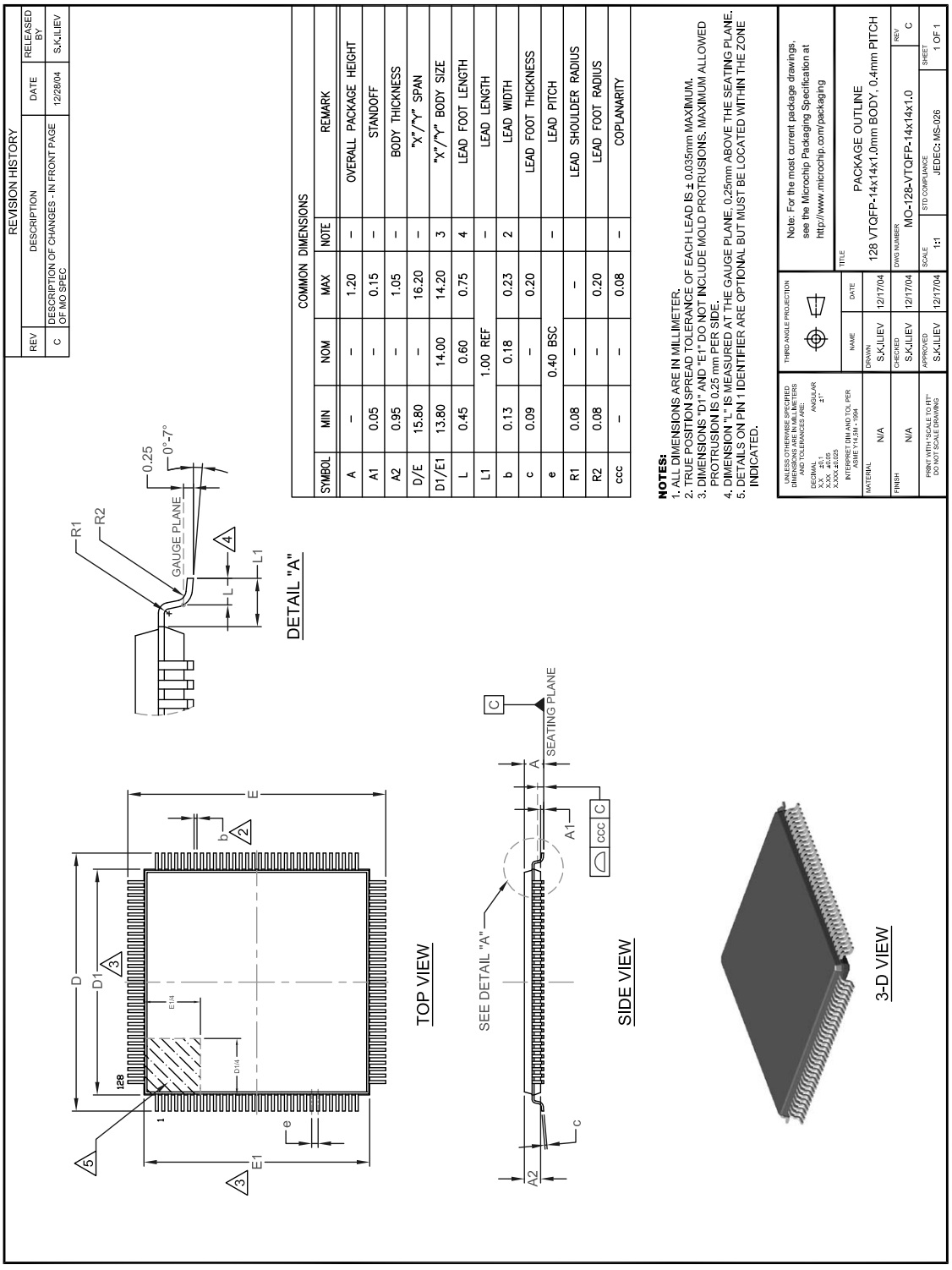
5.4 Capacitance

T_A = 25°C; fc = 1MHz; V_{DD18}, $V_{DD18PLL}$ = *1.8V*

Parameter	Symbol	Limits			Unit	Test Condition
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

6.0 PACKAGE INFORMATION

FIGURE 6-1: USB2227/USB2228 128-PIN VTQFP PKG, 14 X 14 X 1.0MM BODY, 0.4MM PITCH



REVISION HISTORY

REV	DESCRIPTION	DATE	RELEASED BY
C	DESCRIPTION OF CHANGES - IN FRONT PAGE OF MO SPEC	12/28/04	S.K.LILIEV

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	–	–	1.20	–	OVERALL PACKAGE HEIGHT
A1	0.05	–	0.15	–	STANDOFF
A2	0.95	–	1.05	–	BODY THICKNESS
D/E	15.80	–	16.20	–	"X"/"Y" SPAN
D1/E1	13.80	14.00	14.20	3	"X"/"Y" BODY SIZE
L	0.45	0.60	0.75	4	LEAD FOOT LENGTH
L1		1.00 REF		–	LEAD LENGTH
b	0.13	0.18	0.23	2	LEAD WIDTH
c	0.09	–	0.20		LEAD FOOT THICKNESS
e		0.40 BSC		–	LEAD PITCH
R1	0.08	–	–		LEAD SHOULDER RADIUS
R2	0.08	–	0.20		LEAD FOOT RADIUS
ccc	–	–	0.08	–	COPLANARITY

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. TRUE POSITION SPREAD TOLERANCE OF EACH LEAD IS ± 0.035mm MAXIMUM.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. MAXIMUM ALLOWED PROTRUSION IS 0.25 mm PER SIDE.
4. DIMENSION "L" IS MEASURED AT THE GAUGE PLANE, 0.25mm ABOVE THE SEATING PLANE.
5. DETAILS ON PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

UNLESS OTHERWISE SPECIFIED DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994
DECIMAL X.X ±0.1 X.XX ±0.05 X.XXX ±0.025
ANGULAR ±1°
INTERPRET DIM AND TOL PER ASME Y14.5M - 1994
MATERIAL: N/A
FINISH: N/A
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN	S.K.LILIEV	12/17/04
CHECKED	S.K.LILIEV	12/17/04
APPROVED	S.K.LILIEV	12/17/04

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

TITLE: PACKAGE OUTLINE 128 VTQFP-14x14x1.0mm BODY, 0.4mm PITCH
DWG NUMBER: MO-128-VTQFP-14x14x1.0
REV: C
SCALE: 1:1
STD COMPLIANCE: JEDEC± MS-026
SHEET: 1 OF 1

DETAIL "A"
TOP VIEW
SIDE VIEW
3-D VIEW

7.0 GPIO USAGE

TABLE 7-1: GPIO USAGE (ROM REV -11)

Name	Active Level	Symbol	Description and Note
GPIO1	H	Flash Media Activity LED/ xD_Door	Indicates media activity. Media or USB cable must not be removed with LED lit. Also may be used for xD Door functionality
GPIO2	H	EE_CS	Serial EE PROM chip select
GPIO3	H	V_BUS	USB V bus detect
GPIO4	H	EE_DIN/EE_DOUT/xDID	Serial EE PROM input/output and xD Identify
GPIO5	L	HS_IND/SD_CD	HS Indicator LED or SD Card Detect Switch input
GPIO6	H	A16/ROMEN	A16 address line connect for DFU or debug LED indicator optional.
GPIO7	H	EE_CLK/ UNCONF_LED	Serial EE PROM clock output or Unconfigured LED.
GPIO8	L	MS_PWR_CTRL/ CRD_PWR0	Memory Stick Card Power Control, or Internal Power FET0.
GPIO9	L	CF_PWR_CTRL	CompactFlash Card Power Control
GPIO10	L	SM_PWR_CTRL/ CRD_PWR1	SmartMedia Card Power Control, or Internal Power FET1.
GPIO11	L	SD/MMC_PWR_CTRL/ CRD_PWR2	SD/MMC Card Power Control, or Internal Power FET2.
GPIO12	H	MS_ACT_IND/ Media Activity	Memory Stick Activity Indicator, or Media Activity LED.
GPIO13	H	CF_ACT_IND	CompactFlash Activity Indicator
GPIO14	H	SM_ACT_IND	SmartMedia Activity Indicator
GPIO15	H	SD/MMC_ACT_IND	SD/MMC Activity Indicator

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002256A (08-02-16)	Replaces previous SMSC version Rev. 1.93 (11-01-07)	

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PART NO.	[X]	-	XXX	-	[X]
Device	Temperature Range		Package		Internal Microchip Code

Device:	USB2227, USB2228
Temperature Range:	Blank = 0°C to +70°C (Commercial)
Package:	NU = 128-pin VTQFP

Examples:

USB2227-NU-11
128-pin VTQFP RoHS Compliant package, Commercial Temp, Tray

USB2228-NU-11
128-pin VTQFP RoHS Compliant package, Commercial Temp, Tray

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