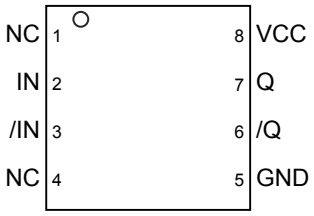
PACKAGE/ORDERING INFORMATION



8-Pin QFN

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89327LMGTR	QFN-8	Industrial	327 with Pb-Free bar-line indicator	Pb-Free NiPdAu

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
2, 3	IN, /IN	Differential inputs: This input is the differential signal input to the device. This input accepts AC- or DC-coupled signals as small as 100mV. External termination is required. Please refer to the "Input Interface Applications" section for more details.
8	VCC	Positive power supply. Bypass with 0.1µF ||0.01µF low ESR capacitors.
7, 6	Q, /Q	Differential LVPECL Output: Terminate with 50Ω to V_{CC}–2V. See "Output Interface Applications" section. Output pair is 100k temperature compensated LVPECL compatible.
5	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
1, 4	NC	No connect.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

Do not leave unused inputs floating. Tie either the true or complement input to ground. A logic zero is achieved by connecting the complement input to ground with the true input floating. For a TTL input, tie a 2.5kΩ resistor between the complement input and ground. See "Input Interface" section.

Input Levels

LVDS, CML, and HSTL differential signals may be connected directly to the D inputs. Depending on the actual worst case voltage seen, the SY8327L's performance varies as per the following table:

Input Voltage Range	Minimum Voltage Swing	Maximum Translation Speed
0 to 2.4V	100mV	2.5Gbps
0 to V_{CC} +0.3V	200mV	1.25Gbps

For LVDS applications, only point-to-point interfaces are supported. Due to the current required by the input structure shown in Figure 1, multi-drop and multi-point architectures are not supported.

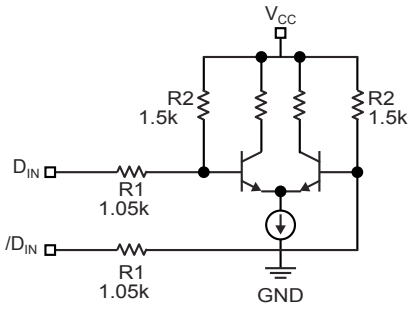


Figure 1. Simplified Input Structure

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC}) ..... –-0.5V to + 4.0V
Input Voltage (VIN) ..... –0.5V to V_{CC}
Input Current
  Source or sink current on IN, /IN ..... ±50mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(2)

Supply Voltage (V_{CC}) ..... 3.0V to 3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance(3)
QFN (Θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
QFN (Ψ_{JB})
  Junction-to-Board ..... 32°C/W

DC ELECTRICAL CHARACTERISTICS(4)

T_A = –40°C to +85°C; unless stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}(5)		28	45	mA

INPUT ELECTRICAL CHARACTERISTICS(4)

V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	V_{IH} min must be ≥ 1.2V			V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		–0.3			V
V_{IN}	Input Voltage Swing	See Figure 2a, V_{IH} < 2.4V	100			mV
		See Figure 2a, V_{IH} < V_{CC} +0.3V	200			mV

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS(4)

V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Output HIGH Voltage Q, /Q		V_{CC}–1.945		V_{CC} –1.695	V
V_{OH}	Output Common Mode Range Q, /Q		V_{CC}–1.145		V_{CC} –0.895	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 2a	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 2b	1100	1600		mV_{PP}

Notes:

1. Permanent device damage may occur if the “Absolute Maximum Ratings” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices' most negative potential on the PCB. Ψ_{JB} uses 4-layer Θ_{JA} in still-air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS [5]

V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	2.5			Gbps
		V_{OUT} ≥ 200mV Clock		2.5		GHz
t_{pd}	Propagation Delay IN-to-Q, /IN-to-/Q	V_{IN} ≥ 100mV			400	ps
t_{JITTER}	RMS Phase Jitter	Output = 622MHz Integration Range: 12kHz - 20MHz		75		fs
t_r, t_f	Rise / Fall Time (20% to 80%) Q, /Q	At full output swing			200	ps

Notes:

5. See “Timing Diagrams” section for definition of parameters. High frequency AC-parameters are guaranteed by design and characterization.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

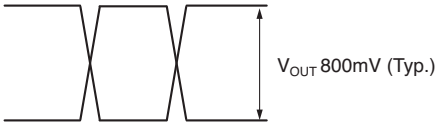


Figure 2a. Single-Ended Voltage Swing

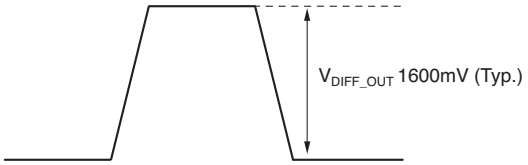


Figure 2b. Differential Voltage Swing

TIMING DIAGRAM

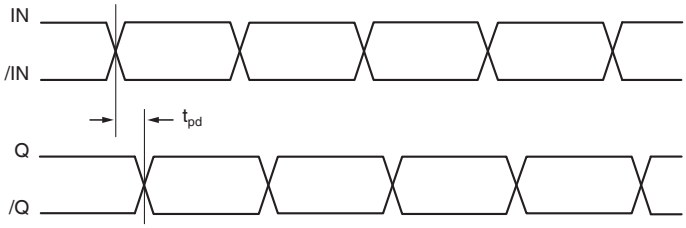


Figure 3. Timing Diagram

INPUT INTERFACE APPLICATIONS

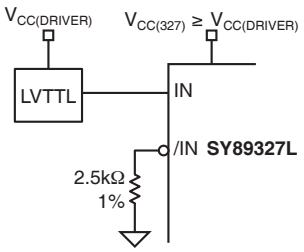


Figure 4. 3.3V "TTL"

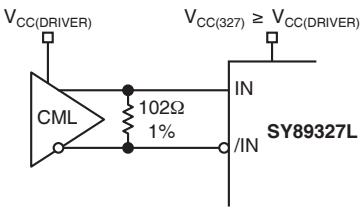


Figure 5. CML-DC Coupled

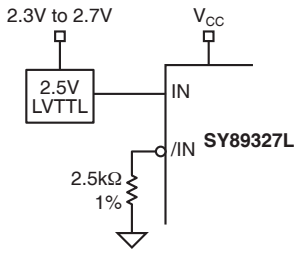


Figure 6. 2.5V "TTL"

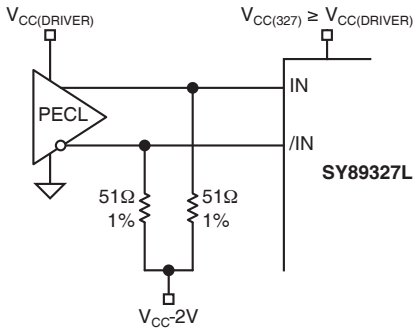


Figure 7. PECL-DC Coupled

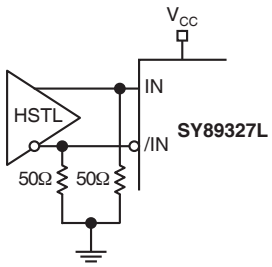


Figure 8. HSTL

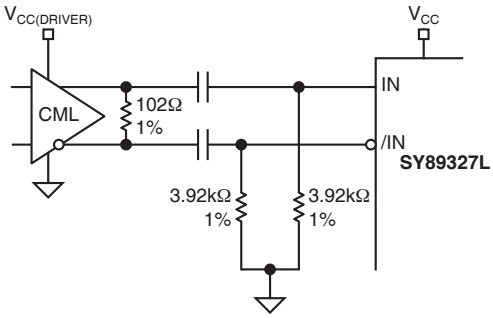


Figure 9. CML-AC Coupled Short Lines

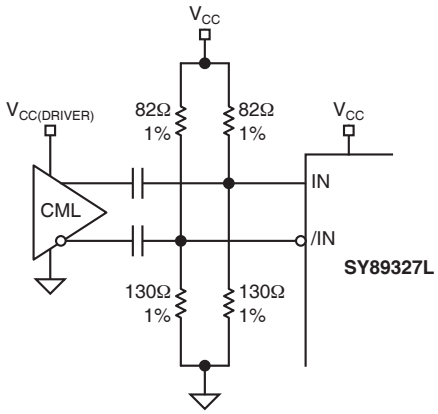


Figure 10. CML-AC Coupled Long Lines

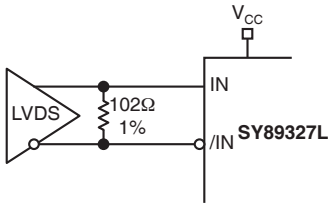


Figure 11. LVDS

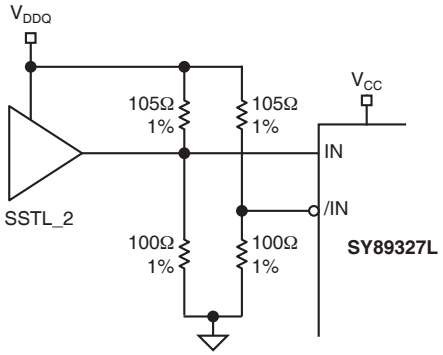


Figure 12. SSTL_2

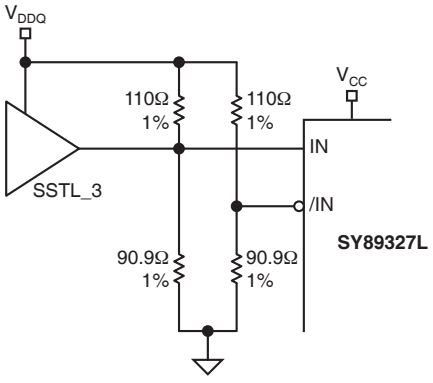
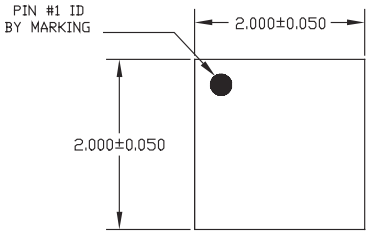


Figure 13. SSTL_3

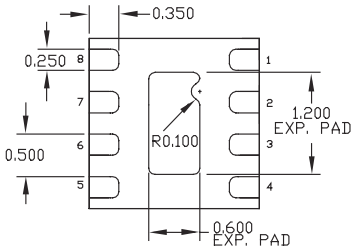
RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Datasheet Link
SY55857L	3.3V, 2.5Gbps Any Input-to-LVPECL Dual Translator	www.micrel.com/product-info/products/sy55857l.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

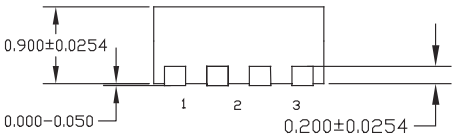
8-PIN QFN (QFN-8)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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