

Contents

1      **Electrical ratings** ..... 3

2      **Electrical characteristics** ..... 4

      2.1    Electrical characteristics (curves) ..... 6

3      **Test circuits** ..... 8

4      **Package mechanical data** ..... 9

5      **Packaging mechanical data** ..... 12

6      **Revision history** ..... 14



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	160	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	115	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	640	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	36	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	26	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	144	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	84	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	4	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	200	mJ
$T_j$	Operating junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature		$^{\circ}\text{C}$

1. This value is rated according to  $R_{thj-c}$
2. Pulse width limited by safe operating area
3. This value is rated according to  $R_{thj-pcb}$
4.  $L=1\text{ mH}$ ,  $I_D=20\text{ A}$ ,  $V_{DD}=25\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31.3	$^{\circ}\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case max	1.5	$^{\circ}\text{C/W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified).

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 24\text{ V}$			500	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	1.2		2.3	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 18\text{ A}$		0.0016	0.0021	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$		0.0025	0.0031	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	3245	-	pF
$C_{oss}$	Output capacitance		-	970	-	pF
$C_{rss}$	Reverse transfer capacitance		-	52	-	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}, I_D = 36\text{ A},$ $V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 13</a> )	-	20	-	nC
$Q_{gs}$	Gate-source charge		-	9.3	-	nC
$Q_{gd}$	Gate-drain charge		-	5.7	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}, I_D = 18\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 4.5\text{ V}$	-	12.4	-	ns
$t_r$	Rise time		-	21.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	50.7	-	ns
$t_f$	Fall time		-	19.5	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		480	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0$ , $I_{SD} = 2$ A	-	0.4	0.7	V
$t_{rr}$	Reverse recovery time	$V_{GS} = 0$ V, $I_D = 36$ A, $di/dt = 100$ A/ $\mu$ s	-	46		ns
$Q_{rr}$	Reverse recovery charge		-	46		nC
$I_{RRM}$	Reverse recovery current		-	2		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

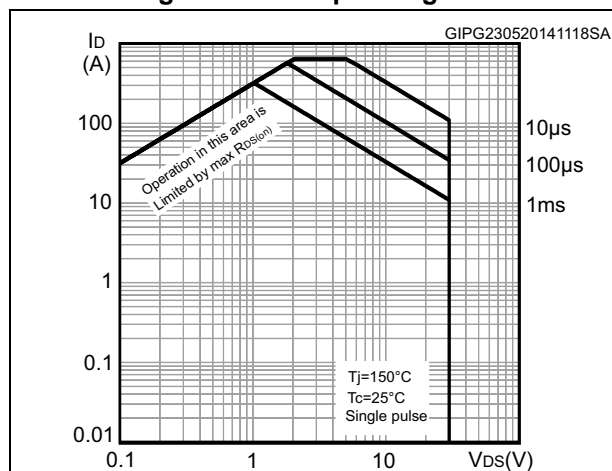


Figure 3. Thermal impedance

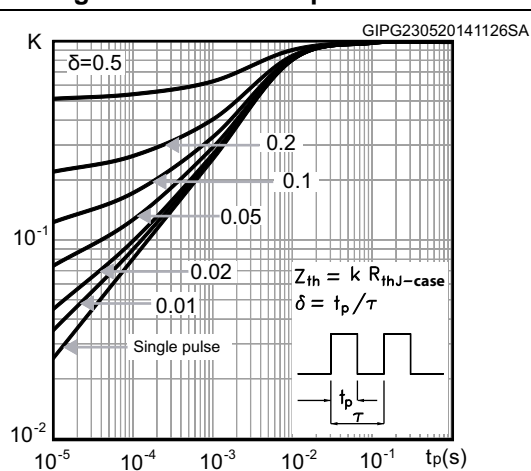


Figure 4. Output characteristics

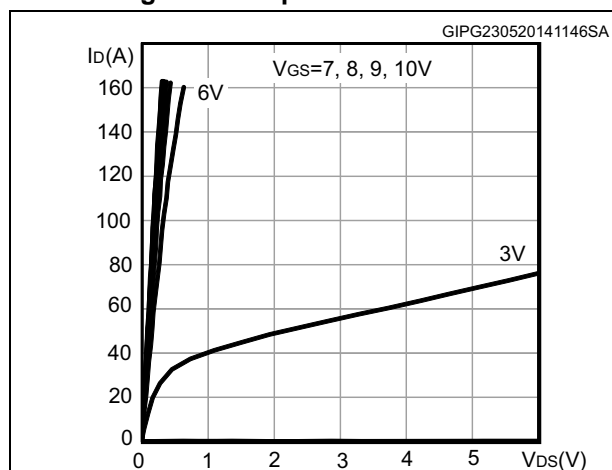


Figure 5. Transfer characteristics

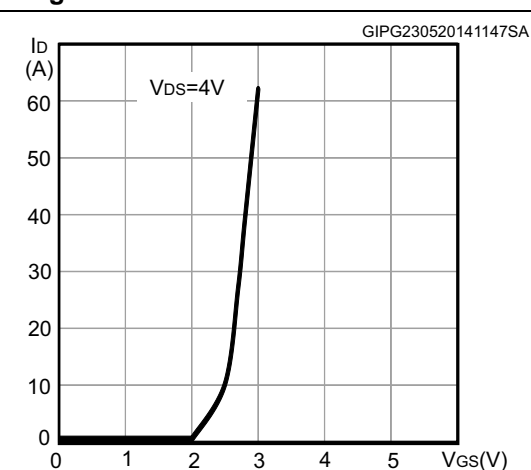


Figure 6. Gate charge vs gate-source voltage

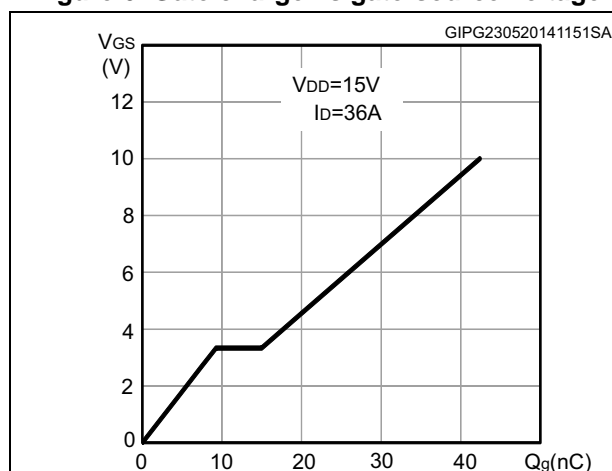


Figure 7. Static drain-source on-resistance

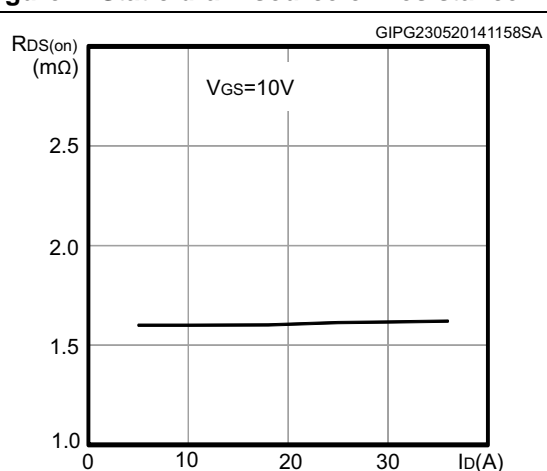


Figure 8. Capacitance variations

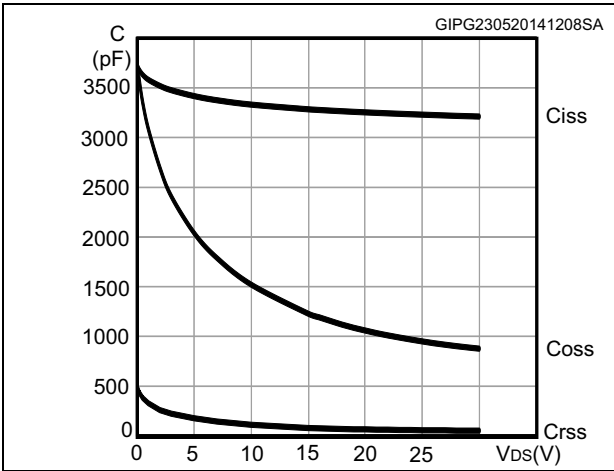


Figure 9. Normalized gate threshold voltage vs temperature

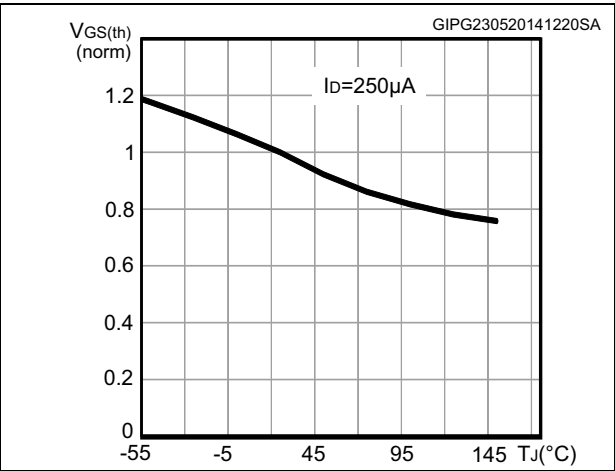


Figure 10. Normalized on-resistance vs temperature

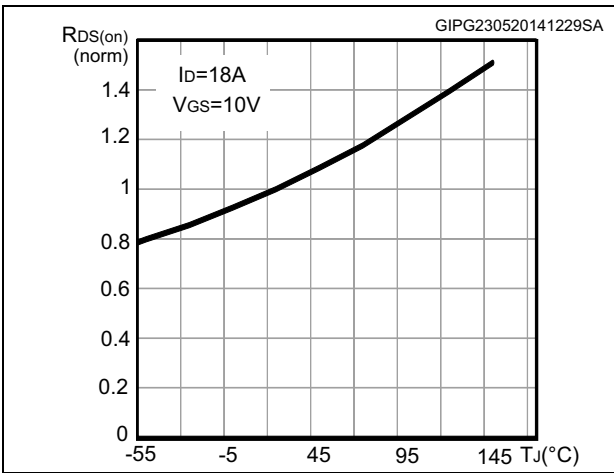
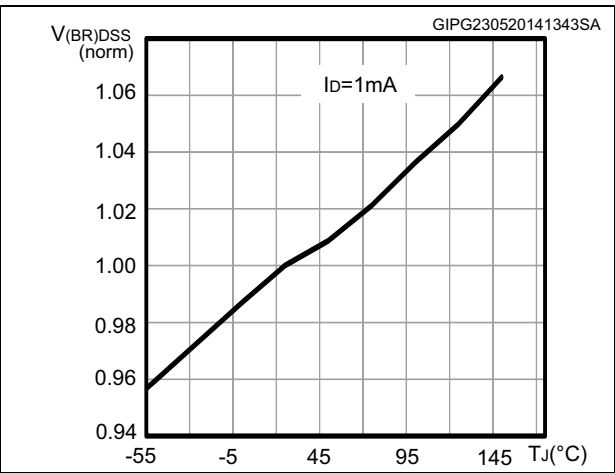


Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature



### 3 Test circuits

Figure 12. Switching times test circuit for resistive load

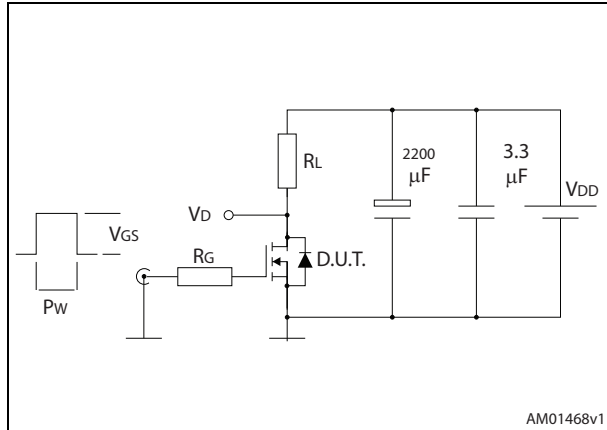


Figure 13. Gate charge test circuit

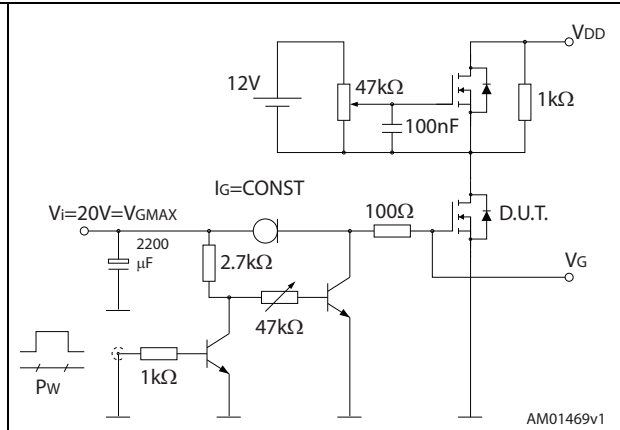


Figure 14. Test circuit for inductive load switching and diode recovery times

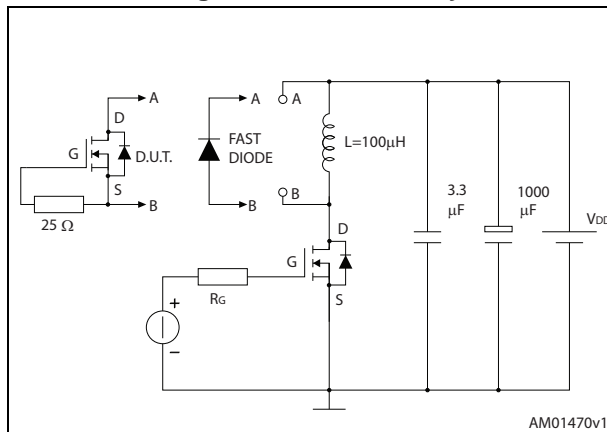


Figure 15. Unclamped inductive load test circuit

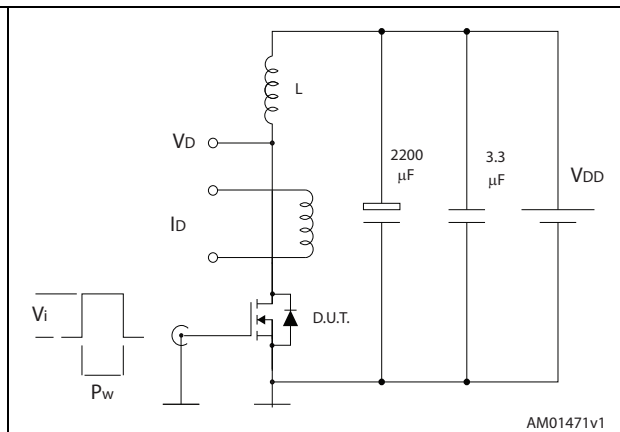


Figure 16. Unclamped inductive waveform

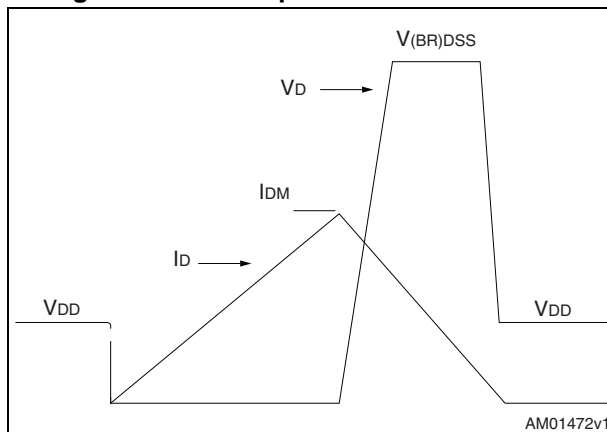
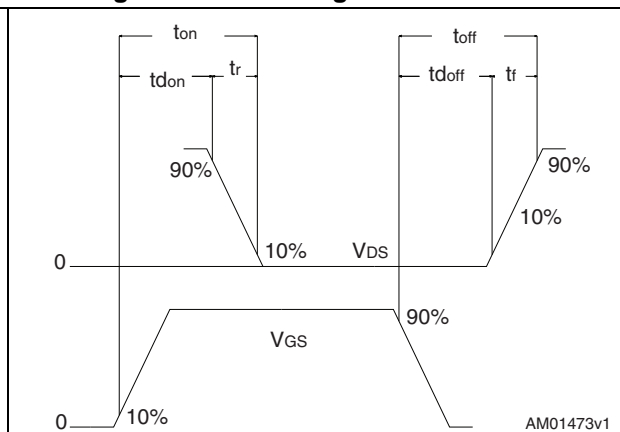


Figure 17. Switching time waveform



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.



Figure 18. PowerFLAT™ 5x6 type S-C mechanical data

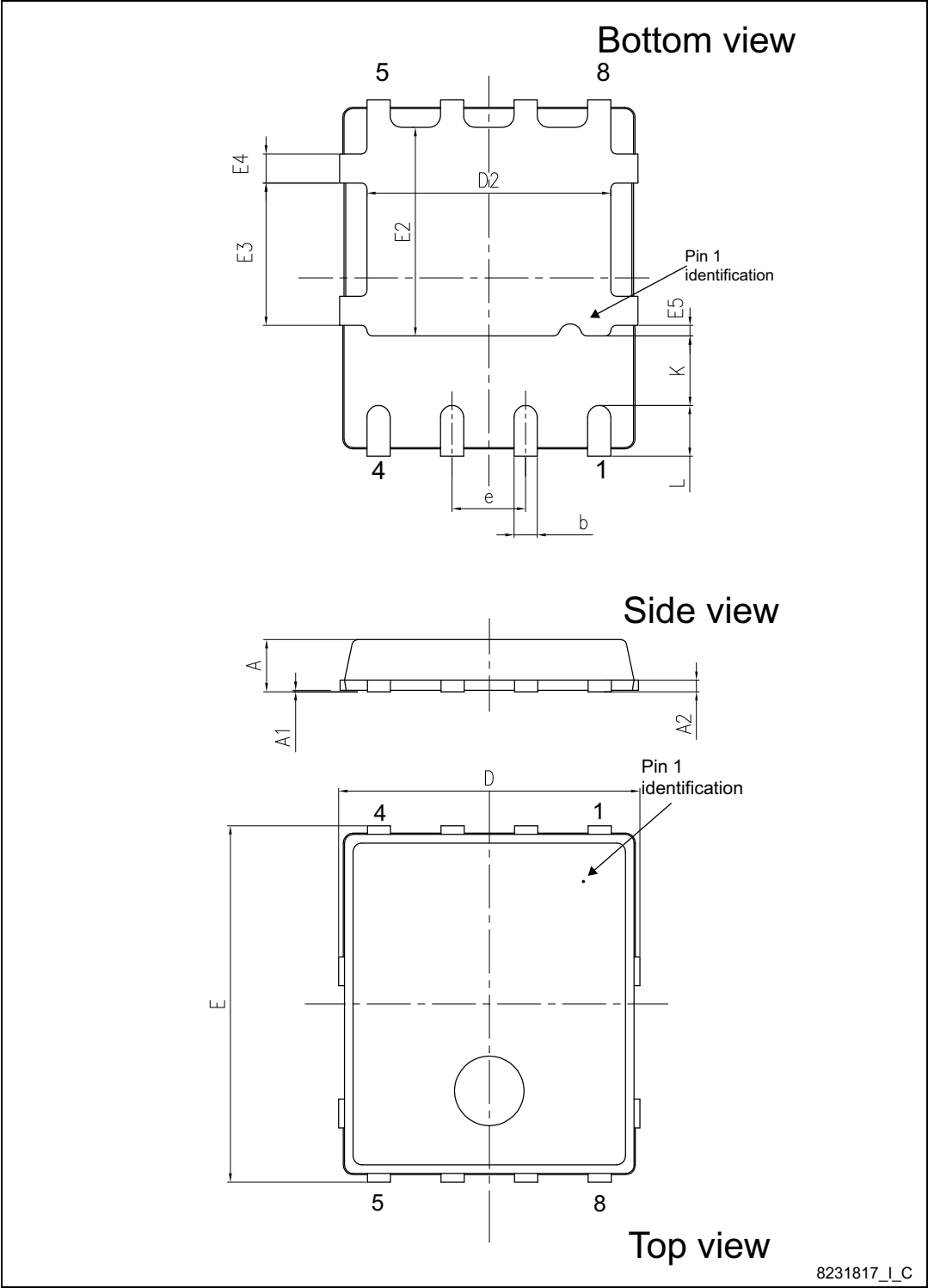
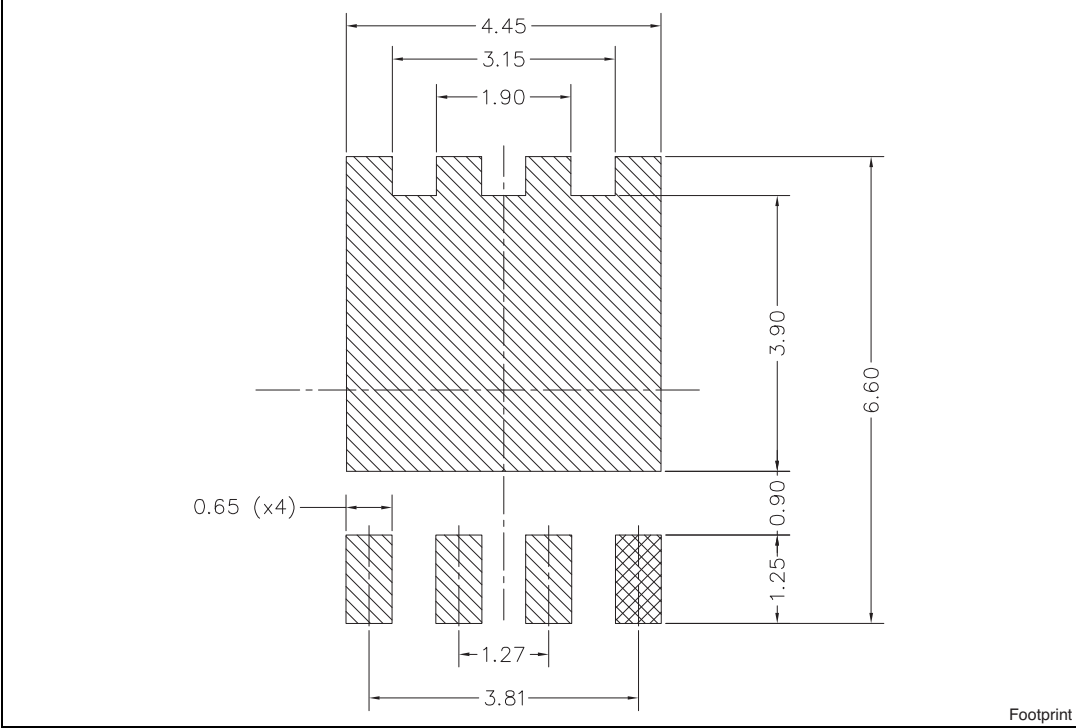


Table 8. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
D2	4.11		4.31
E		6.15	
e		1.27	
e1		0.65	
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
K	1.05		1.35
L	0.715		1.015

Figure 19. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 20. PowerFLAT™ 5x6 tape<sup>(a)</sup>

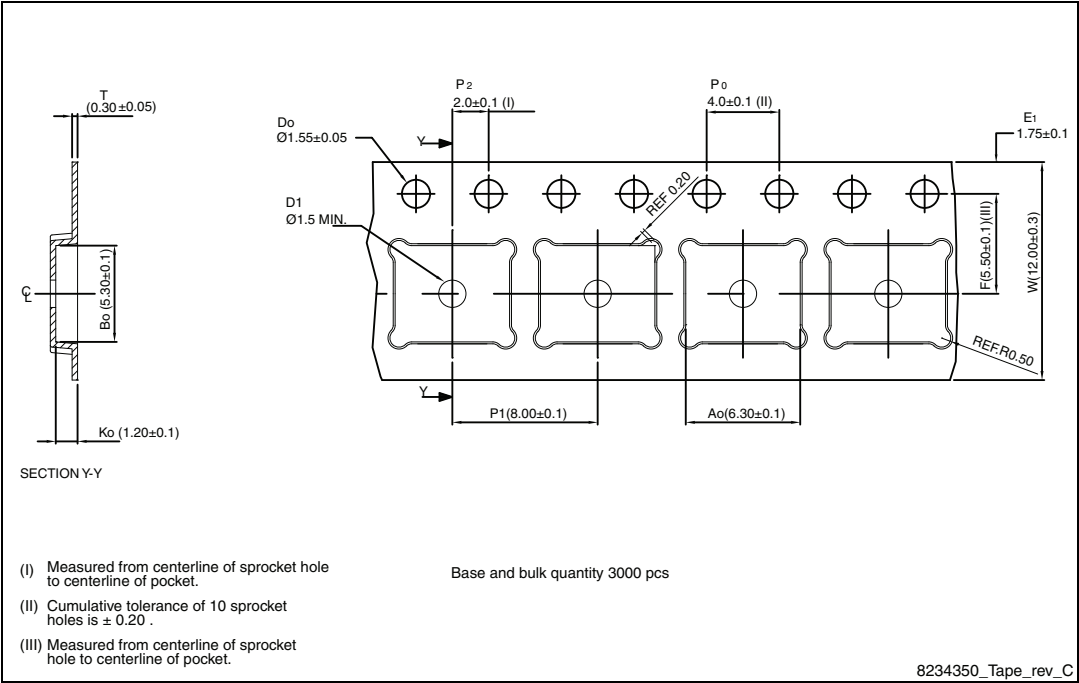
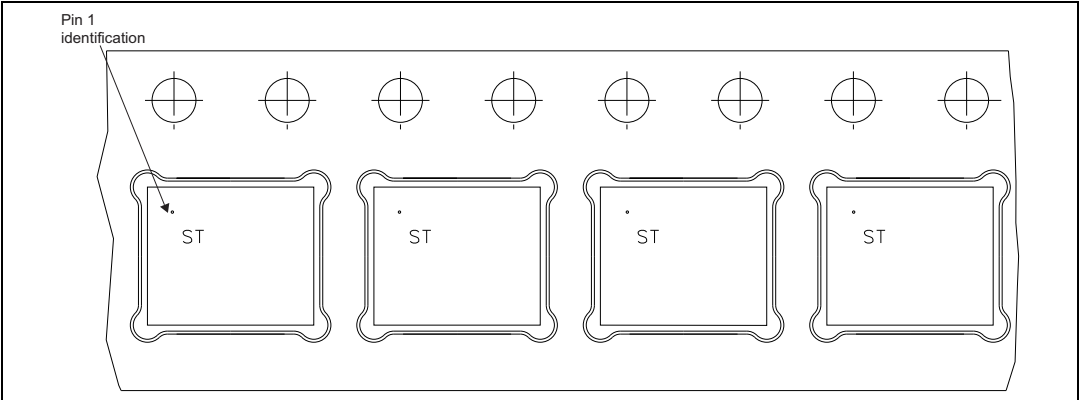
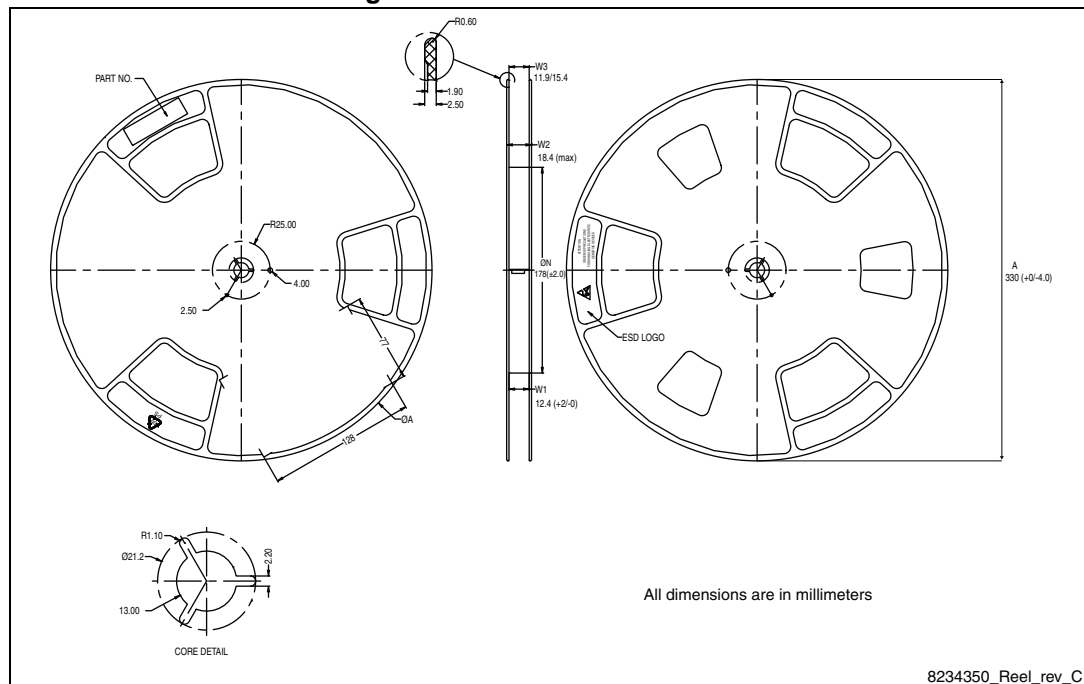


Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

**Figure 22. PowerFLAT™ 5x6 reel**



## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
11-Jun-2013	1	First release.
26-May-2014	2	<ul style="list-style-type: none"><li>– Document status promoted from target to production data</li><li>– Modified: <math>T_J</math> value in <a href="#">Table 2</a></li><li>– Modified: the entire typical values in <a href="#">Table 5</a>, <a href="#">6</a>, <a href="#">7</a></li><li>– Added: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>
18-Jun-2014	3	<ul style="list-style-type: none"><li>– Added: <math>E_{AS}</math> value in <a href="#">Table 2</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>
24-Jul-2014	4	<ul style="list-style-type: none"><li>– Modified: title and features</li><li>– Modified: <math>P_{TOT}</math> values in <a href="#">Table 2</a></li><li>– Modified: <math>I_{SD}</math> and <math>I_{SDM}</math> max values in <a href="#">Table 7</a></li><li>– Minor text changes</li></ul>

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved

