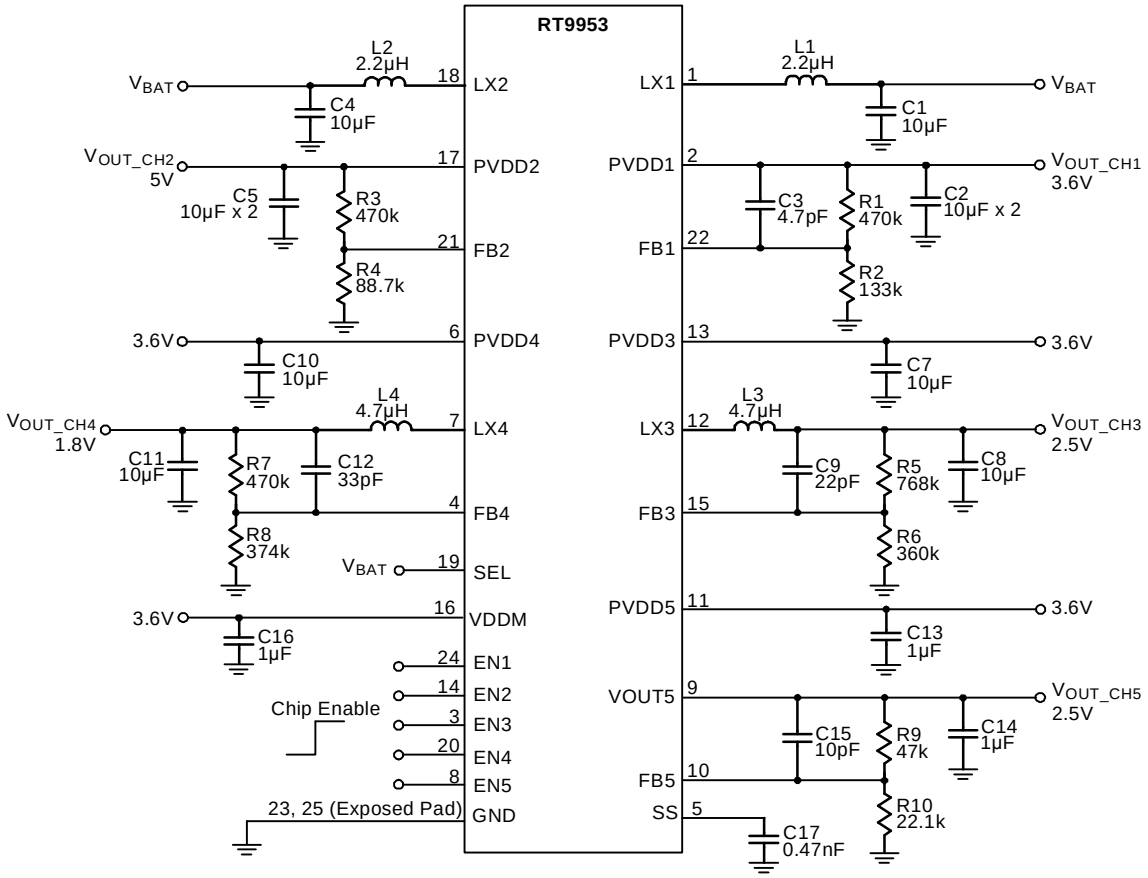
Typical Application Circuit

For 2AA



For Li-ion

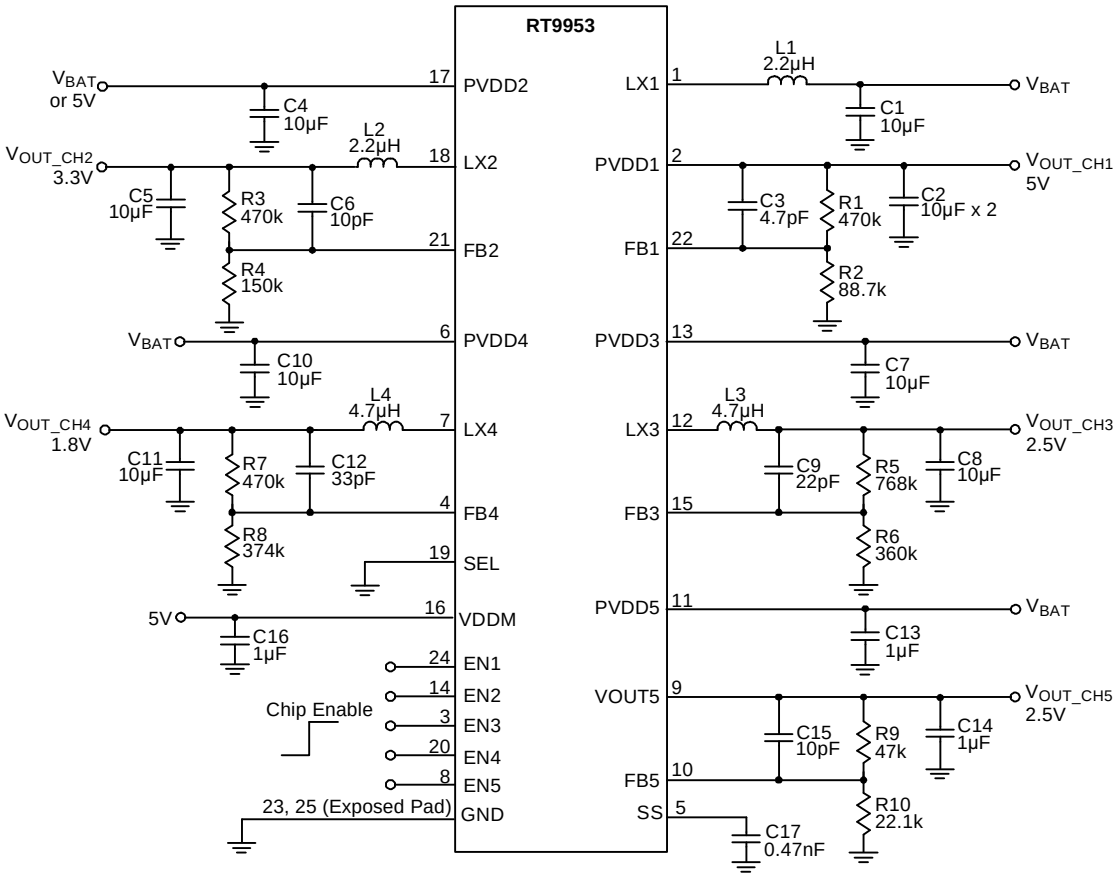


Table 1. Recommended Components for the Typical Application Circuit

Channel	CH3						
Formula	$V_{OUT\_CH3} = (1+R5/R6) \times 0.8$						
V_{OUT_CH3} (V)	3.3	2.5	1.8	1.5	1.3	1.2	1.0
L3 (μH)	4.7	4.7	4.7	4.7	4.7	4.7	4.7
R5 (kΩ)	86.6	768	470	330	237	187	23.2
R6 (kΩ)	27.4	360	374	374	374	374	93.1
C9 (pF)	22	22	33	47	68	82	47
C8 (μF)	10	10	10	10	10	10	10

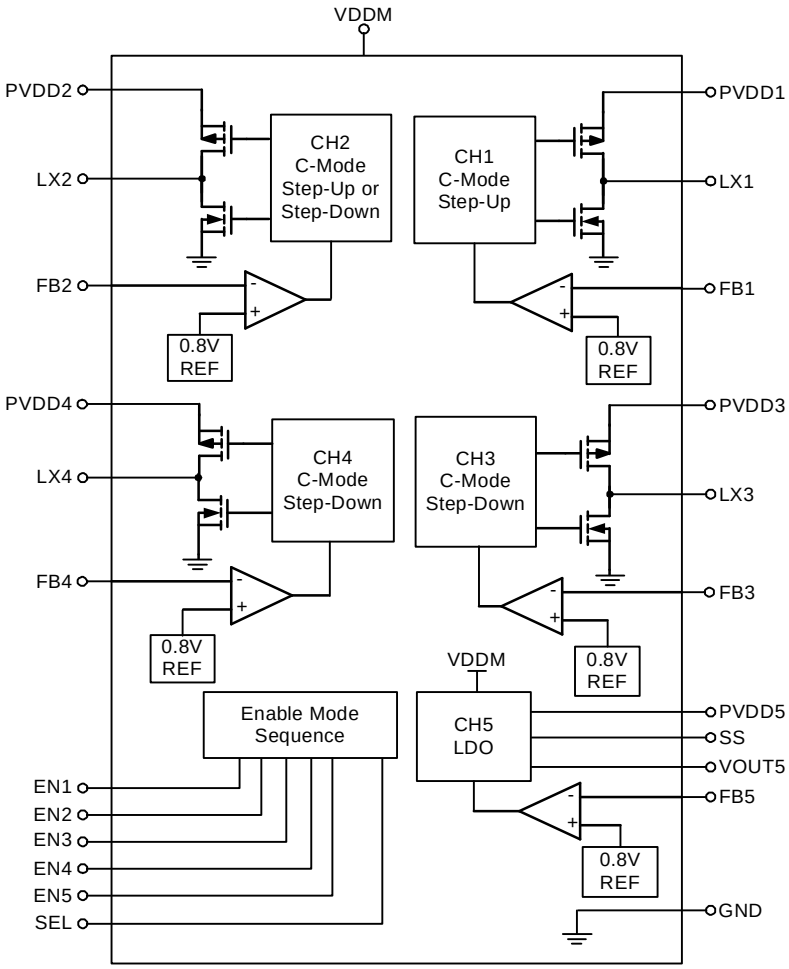
Channel	CH4						
Application	$V_{OUT\_CH4} = (1+R7/R8) \times 0.8$						
V_{OUT_CH4} (V)	3.3	2.5	1.8	1.5	1.3	1.2	1.0
L4 (μH)	4.7	4.7	4.7	4.7	4.7	4.7	4.7
R7 (kΩ)	86.6	768	470	330	237	187	23.2
R8 (kΩ)	27.4	360	374	374	374	374	93.1
C12 (pF)	22	22	33	47	68	82	47
C11 (μF)	10	10	10	10	10	10	10

Channel	CH5
Formula	$V_{OUT\_CH5} = (1+R9/R10) \times 0.8$
V_{OUT_CH5} (V)	2.5
R9 (kΩ)	47
R10 (kΩ)	22.1
C15 (pF)	10
C14 (μF)	1

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LX1	Switch Node of CH1. High impedance in shutdown mode.
2	PVDD1	Power Input of CH1.
3	EN3	Enable Control Input of CH3.
4	FB4	Feedback Input of CH4. High impedance in shutdown mode.
5	SS	Soft-Start Control Input.
6	PVDD4	Power Input of CH4.
7	LX4	Switch Node of CH7. High impedance in shutdown mode.
8	EN5	Enable Control Input of CH5.
9	VOUT5	Output Voltage of CH5.
10	FB5	Feedback Input of CH5. High impedance in shutdown mode.
11	PVDD5	Power Input of CH5.
12	LX3	Switch Node of CH3. High impedance in shutdown mode.
13	PVDD3	Power Input of CH3.
14	EN2	Enable Control Input of CH2.
15	FB3	Feedback Input of CH3. High impedance in shutdown mode.
16	VDDM	Analog Power Input.
17	PVDD2	Power Input of CH2.
18	LX2	Switch Node of CH2. High impedance in shutdown mode.
19	SEL	Selection Input for CH2 step-up or step-down operation mode. Logic state can not be changed during operation.
20	EN4	Enable Control Input of CH4.
21	FB2	Feedback Input of CH2. High impedance in shutdown mode.
22	FB1	Feedback Input of CH1. High impedance in shutdown mode.
23, 25 (Exposed Pad)	GND	Ground Pin. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
24	EN1	Enable Control Input of CH1.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, VDDM, PVDD5 ---------- 0.3V to 7V
- Power Switch :
  LX1, LX2, LX3, LX4 ---------- –0.3V to 6.5V
- The Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN 24L 4x4 ---------- 1.852W
- Package Thermal Resistance (Note 2)
  WQFN 24L 4x4, θ_{JA} ---------- 54°C/W
  WQFN 24L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DDM} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VDDM Operating Voltage	V_{DDM}		2.7	--	5.5	V
VDDM Startup Voltage	V_{ST}		1.5	--	--	V
VDDM Over Voltage Protection			5.7	6	6.25	V
PVDD5 Operating Voltage	V_{PVDD5}		2.5	--	5.5	V
Supply Current						
Shutdown Supply Current into VDDM	I_{OFF}	All EN = 0	--	--	0.1	µA
CH1 (Syn Step-Up) : Supply Current into VDDM	I_{Q1}	Non Switching, EN1 = 3.3V	--	--	800	µA
CH2 (Syn Step-Up or Syn Step-Down) : Supply Current into VDDM	I_{Q2}	Non Switching, EN2 = 3.3V	--	--	800	µA
CH3 (Syn Step-Down) : Supply Current into VDDM	I_{Q3}	Non Switching, EN3 = 3.3V	--	--	800	µA
CH4 (Syn Step-Down) : Supply Current into VDDM	I_{Q4}	Non Switching, EN4 = 3.3V	--	--	800	µA
CH5 (LDO) : Supply Current into PVDD5	I_{Q5}	EN5 = 3.3V, I_{OUT} = 0mA	--	90	130	µA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
CH1,2,3,4 Operating Frequency	f_{OSC}		900	1000	1100	kHz
CH1 Maximum Duty Cycle (Step-Up)		V_{FB1} = 0.7V	80	83	86	%
CH2 Maximum Duty Cycle (Step-Up)		V_{FB2} = 0.7V	80	83	86	%
CH2 Maximum Duty Cycle (Step-Down)		V_{FB2} = 0.7V	--	--	100	%
CH3 Maximum Duty Cycle (Step-Down)		V_{FB3} = 0.7V	--	--	100	%
CH4 Maximum Duty Cycle (Step-Down)		V_{FB4} = 0.7V	--	--	100	%
Feedback Regulation Voltage						
Feedback Regulation Voltage @ FB1, FB2, FB3, FB4, FB5			0.788	0.8	0.812	V
Total Accuracy (Including load regulation and line regulation)			–3	--	3	%
Power Switch						
CH1 On Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, PVDD1 = 3.3V	--	200	250	mΩ
		N-MOSFET, PVDD1 = 3.3V	--	150	200	
CH1 Current Limitation (Step-Up)			--	3	--	A
CH2 On Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, PVDD2 = 3.3V	--	200	250	mΩ
		N-MOSFET, PVDD2 = 3.3V	--	150	200	
CH2 Current Limitation (Step-Down)			--	1.8	--	A
CH2 Current Limitation (Step-Up)			--	3	--	A
CH3 On Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, PVDD3 = 3.3V	--	350	400	mΩ
		N-MOSFET, PVDD3 = 3.3V	--	300	400	
CH3 Current Limitation (Step-Down)			--	1.5	--	A
CH4 On Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, PVDD4 = 3.3V	--	350	400	mΩ
		N-MOSFET, PVDD4 = 3.3V	--	300	400	
CH4 Current Limitation (Step-Down)			--	1.5	--	A
CH5 Dropout Voltage (LDO)	V_{Drop}	2.2V ≦ PVDD5 ≦ 2.7V, I_{OUT} = 400mA	--	160	320	mV
		2.7V ≦ PVDD5 ≦ 5.5V, I_{OUT} = 500mA	--	250	400	
Protection						
Over Voltage Protection of CH1, CH2 Step-Up, PVDD1 and PVDD2			5.7	6	6.25	V
Over Voltage Protection Hysteresis of CH1, CH2 Step-Up, PVDD1 and PVDD2			--	0.5	--	V
Under Voltage Protection (CH1 to CH5)		FB Threshold	0.36	0.4	0.44	V
CH5 Current Limit	I_{LIM}	2.2V ≦ PVDD5 ≦ 2.7V	0.4	0.7	1.05	A
		2.7V ≦ PVDD5 ≦ 5.5V	0.5	0.8	1.05	
Protection Fault Delay			--	100	--	ms

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Control							
EN1 to EN5, SEL Input Threshold	Logic High			1.3	--	5.5	V
	Logic Low			--	--	0.4	V
EN1 to EN5, SEL Sink Current				--	2	6	μA
CH5 LDO Regulation							
Line Regulation		ΔV_{LINE}	V_{PVDD5} = (V_{OUT5} + 1V) to 5.5V I_{OUT} = 1mA	--	--	0.3	%
Load Regulation		ΔV_{LOAD}	1mA < I_{OUT} < 300mA	--	--	0.6	%
Power Supply Rejection Rate	f = 100Hz	PSRR	C_{OUT} = 1uF, I_{OUT} = 100mA	--	–60	--	dB
	f = 10kHz			--	–30	--	
Thermal Protection							
Thermal Shutdown		T_{SD}		125	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

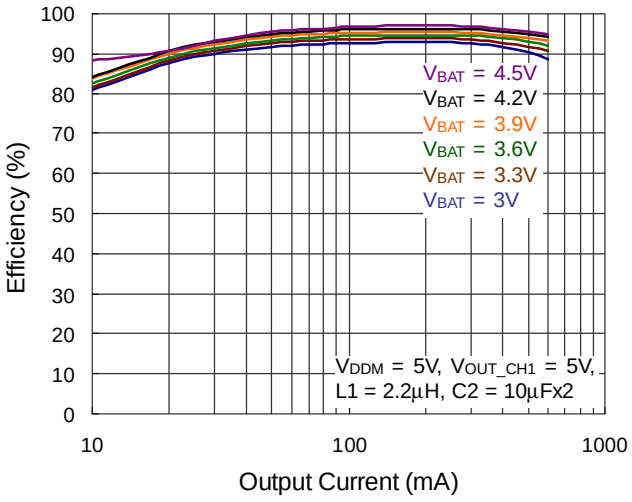
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the WQFN package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

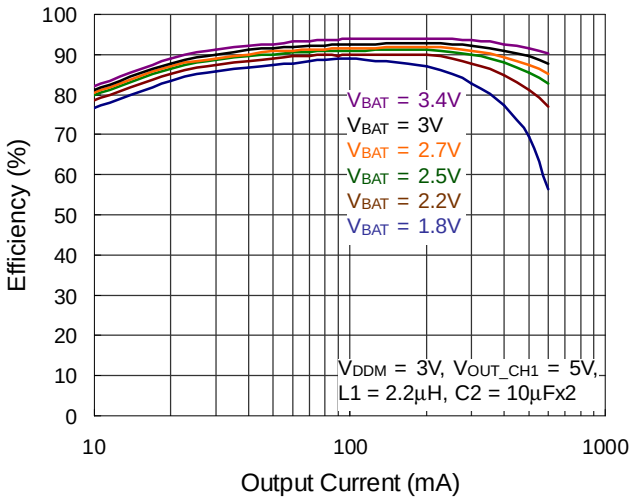
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

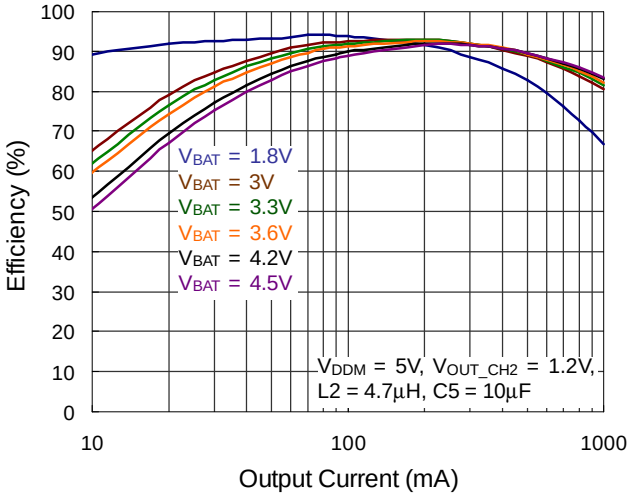
CH1 Step-Up Efficiency vs. Output Current



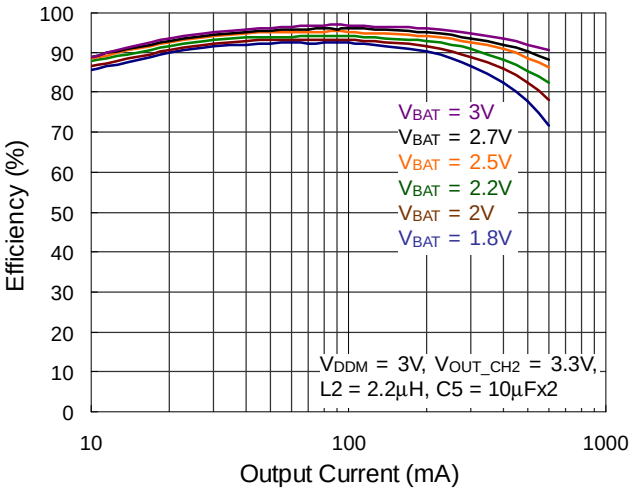
CH1 Step-Up Efficiency vs. Output Current



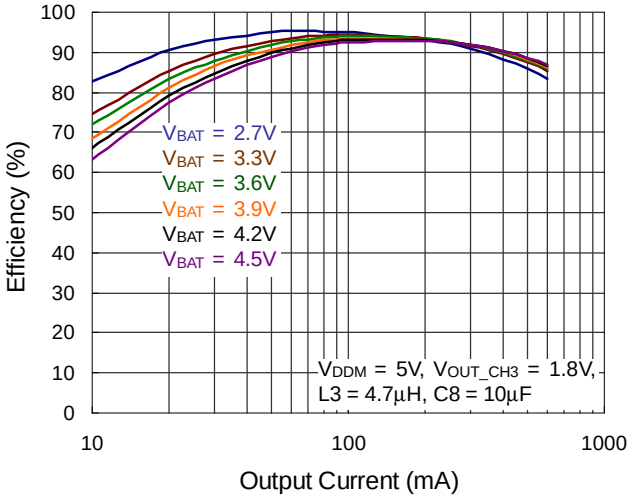
CH2 Step-Down Efficiency vs. Output Current



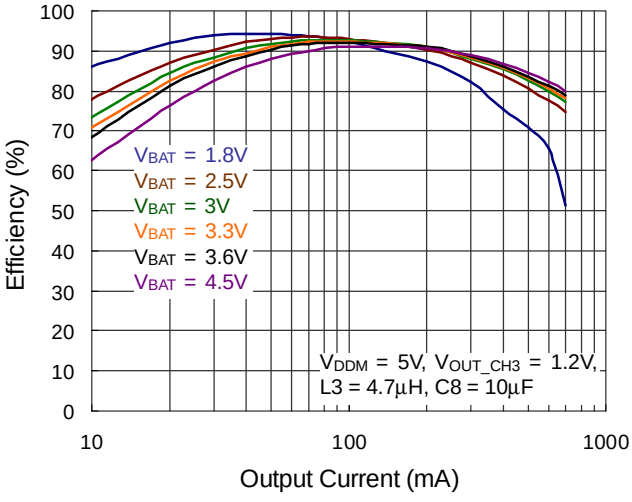
CH2 Step-Up Efficiency vs. Output Current



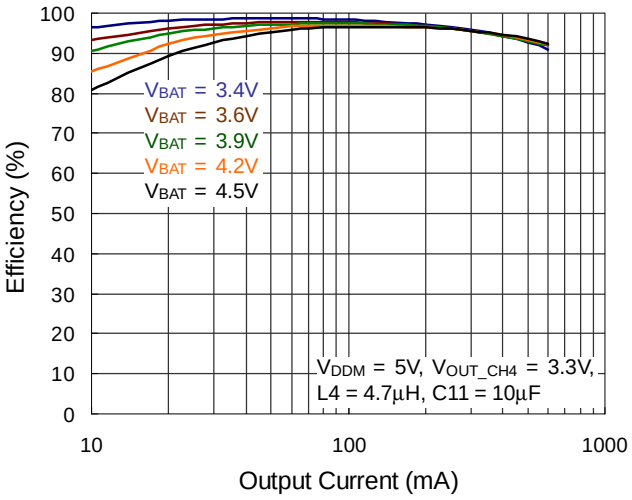
CH3 Step-Down Efficiency vs. Output Current



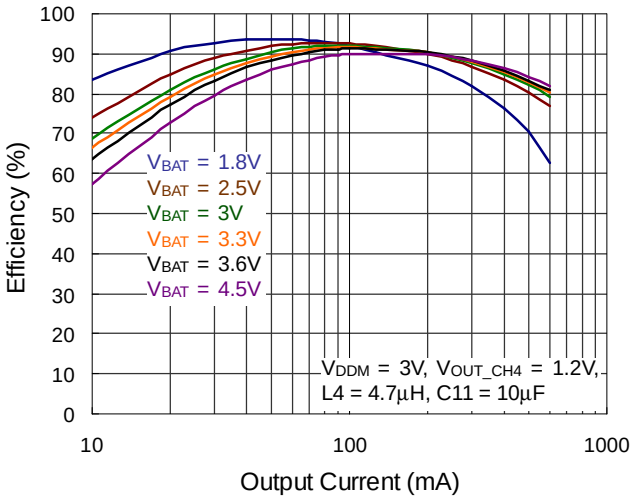
CH3 Step-Down Efficiency vs. Output Current



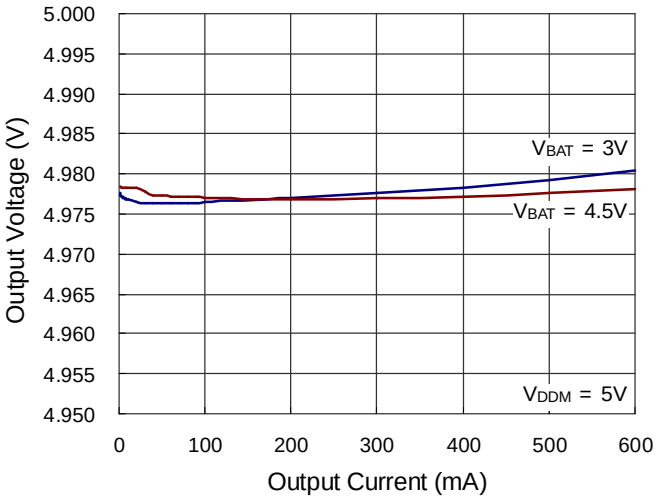
CH4 Step-Down Efficiency vs. Output Current



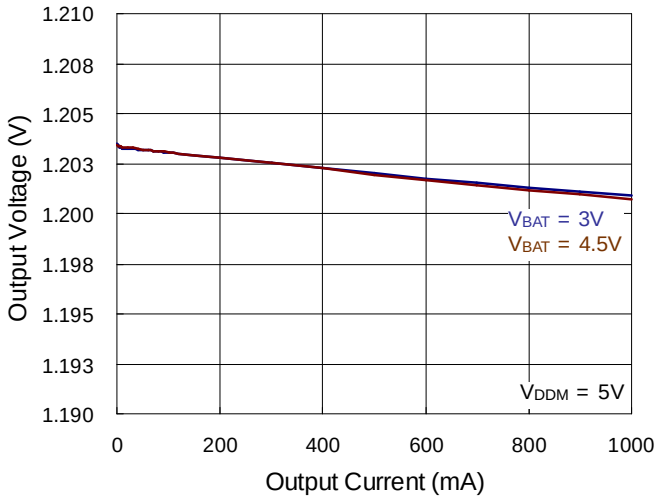
CH4 Step-Down Efficiency vs. Output Current



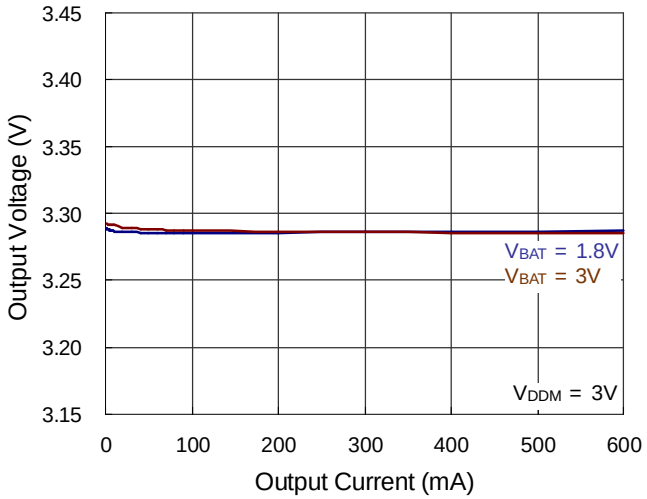
CH1 Step-Up Output Voltage vs. Output Current



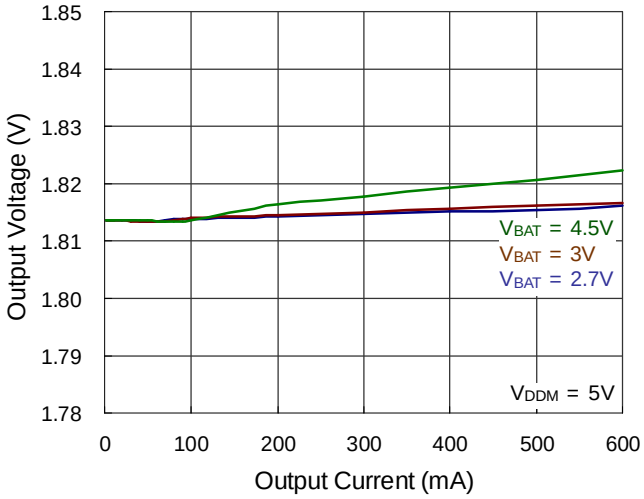
CH2 Step-Down Output Voltage vs. Output Current



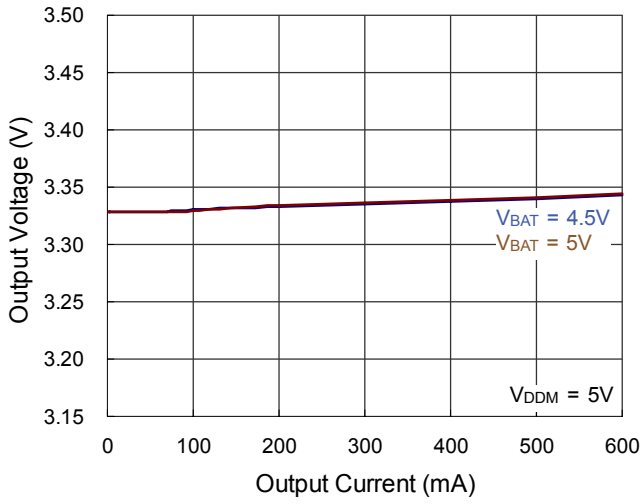
CH2 Step-Up Output Voltage vs. Output Current



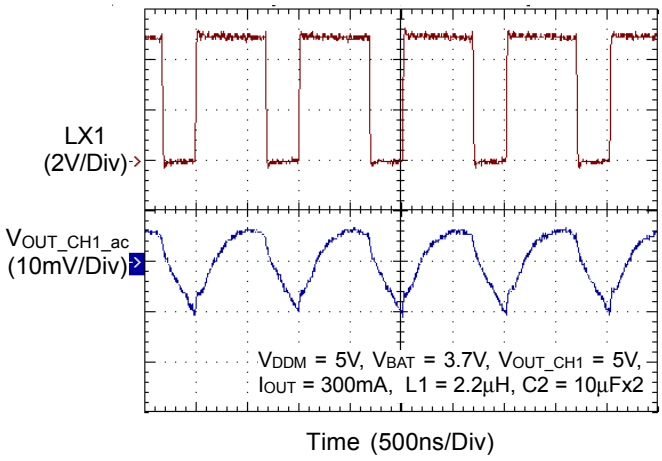
CH3 Step-Down Output Voltage vs. Output Current



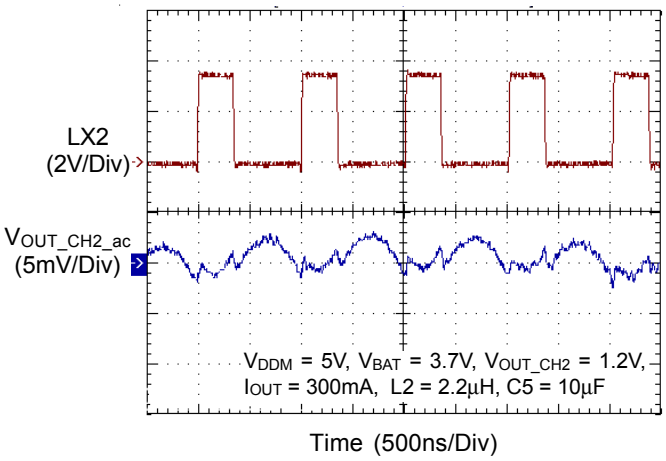
CH4 Step-Down Output Voltage vs. Output Current



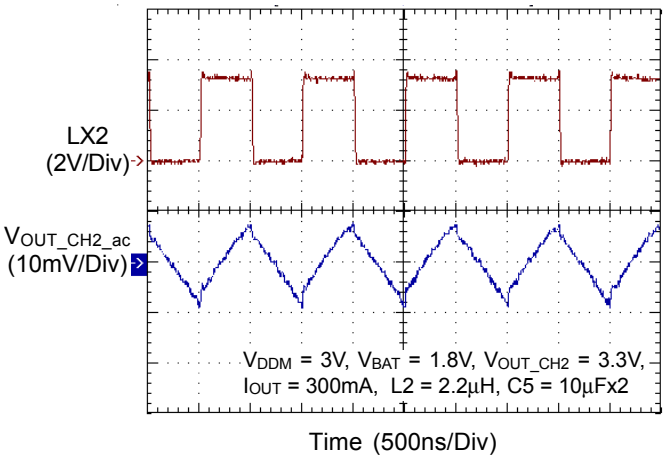
CH1 Output Voltage Ripple



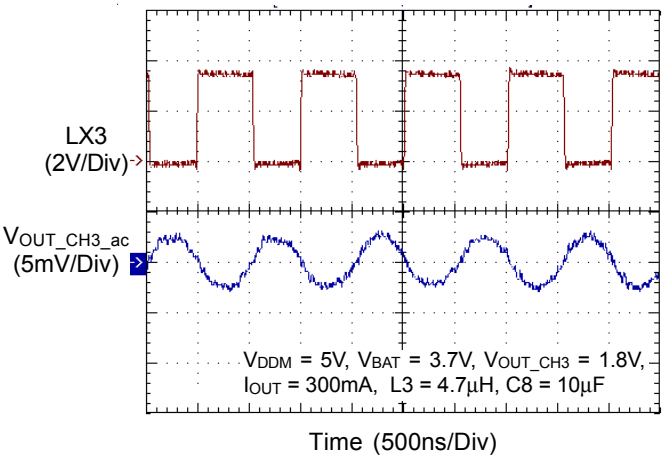
CH2 Step-Down Output Voltage Ripple



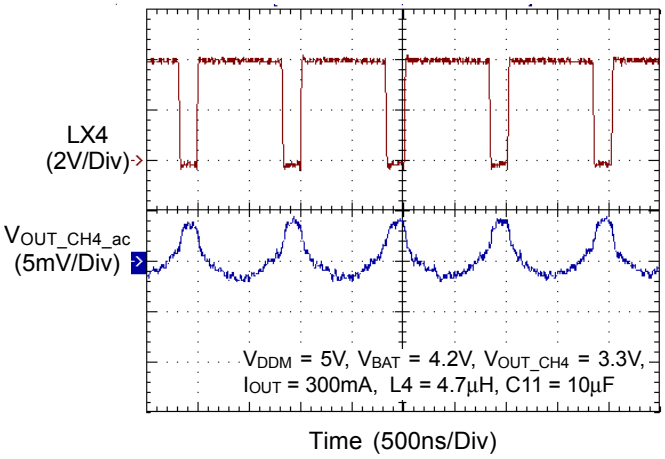
CH2 Step-Up Output Voltage Ripple



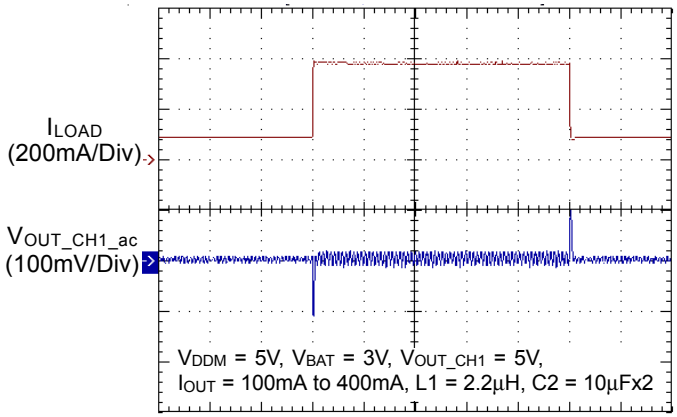
CH3 Output Voltage Ripple



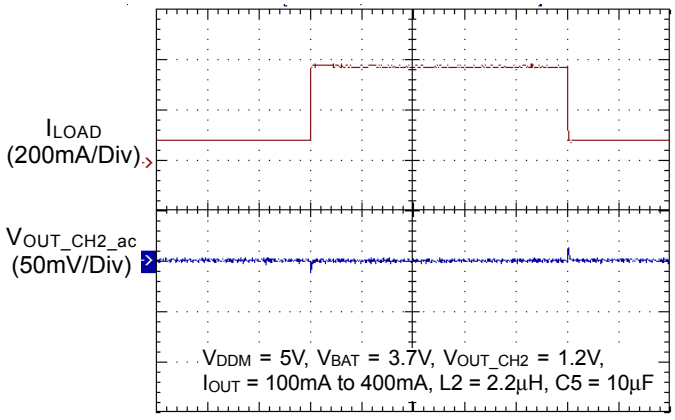
CH4 Output Voltage Ripple



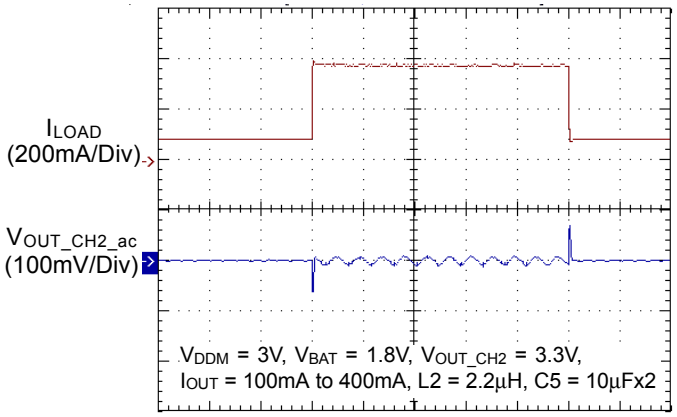
CH1 Load Transient Response



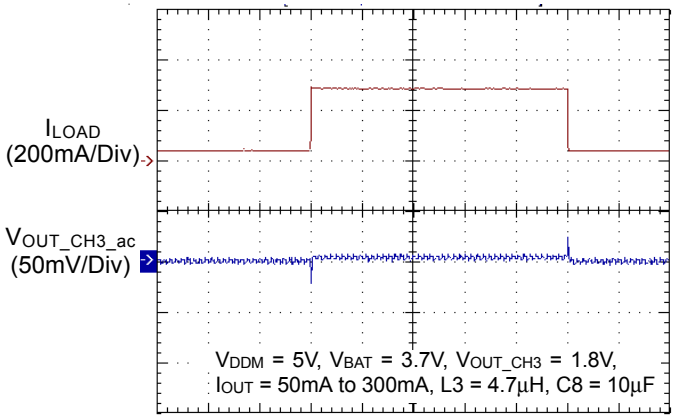
CH2 Step-Down Load Transient Response



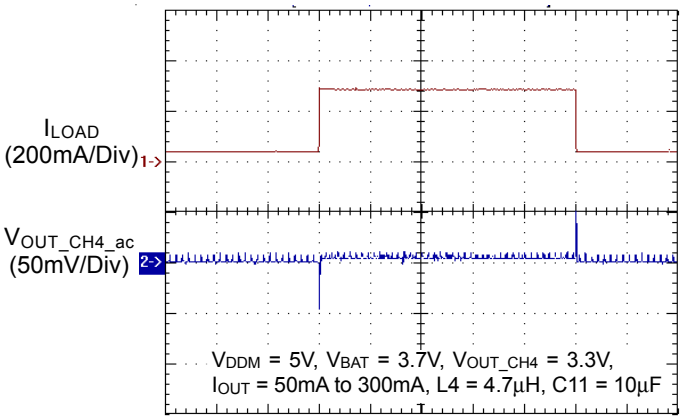
CH2 Step-Up Load Transient Response



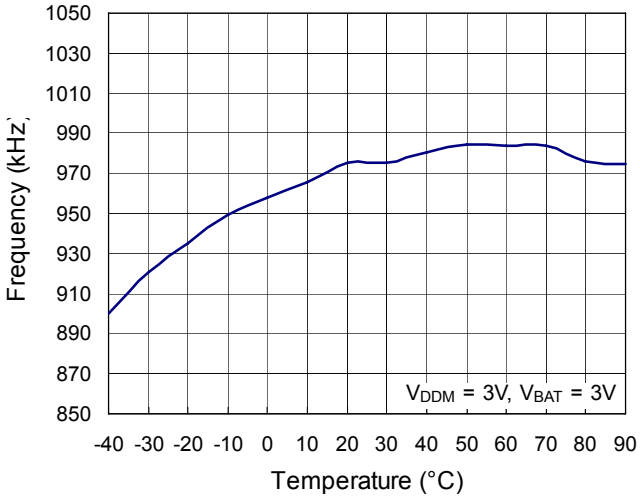
CH3 Load Transient Response



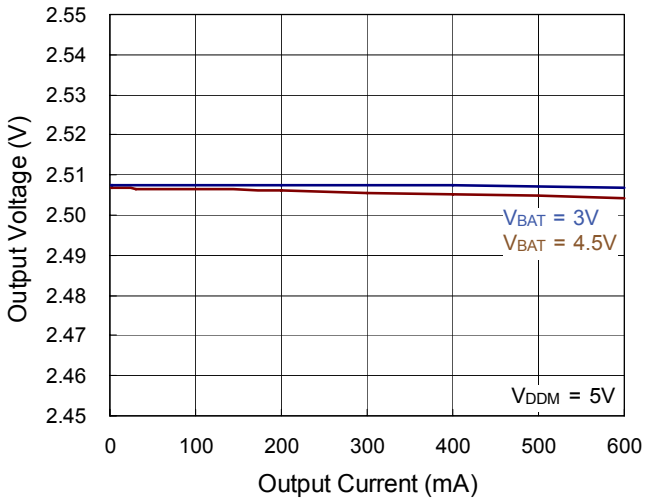
CH4 Load Transient Response



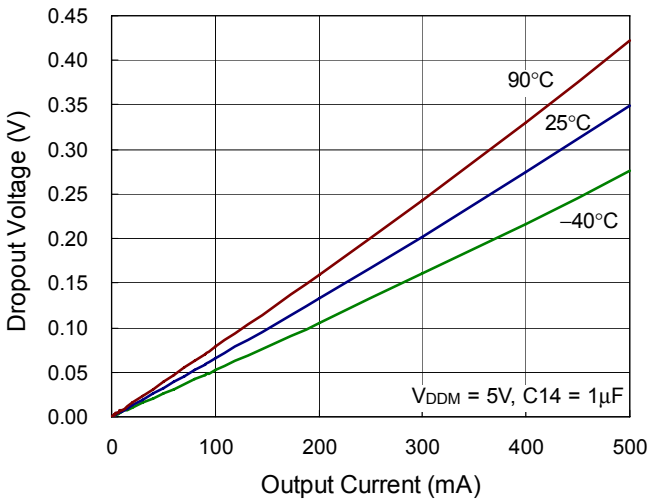
Frequency vs. Temperature



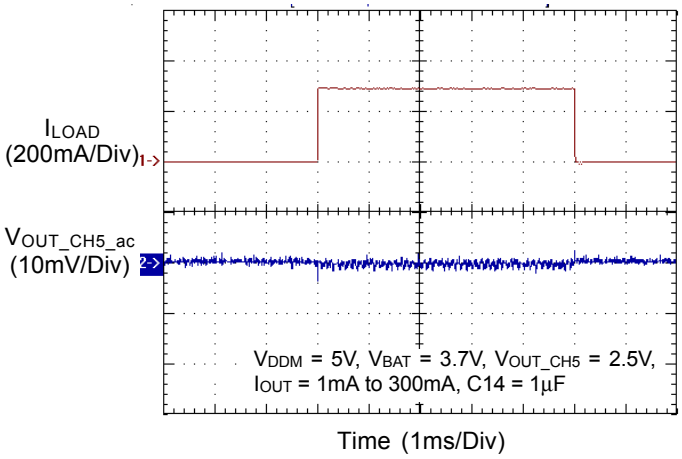
CH5 LDO Output Voltage vs. Output Current



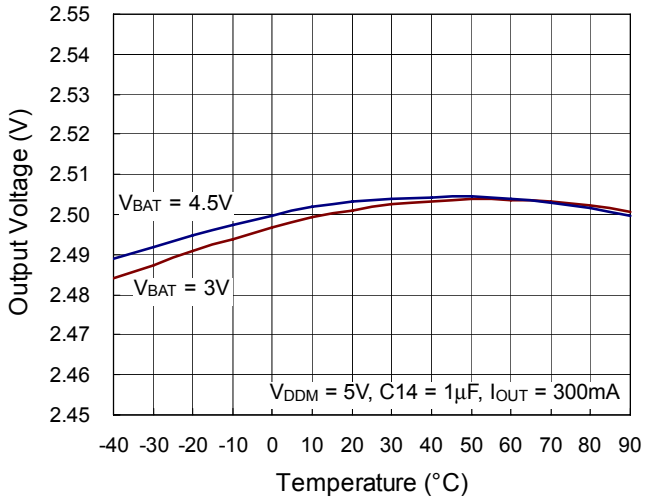
CH5 LDO Dropout Voltage vs. Output Current



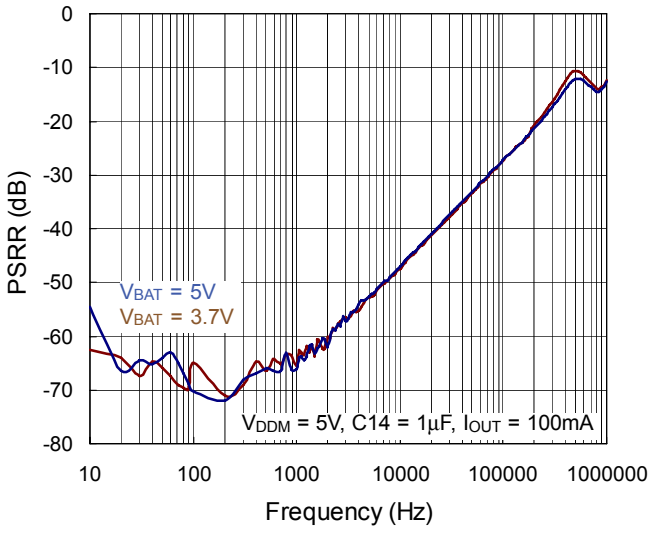
CH5 LDO Load Transient Response



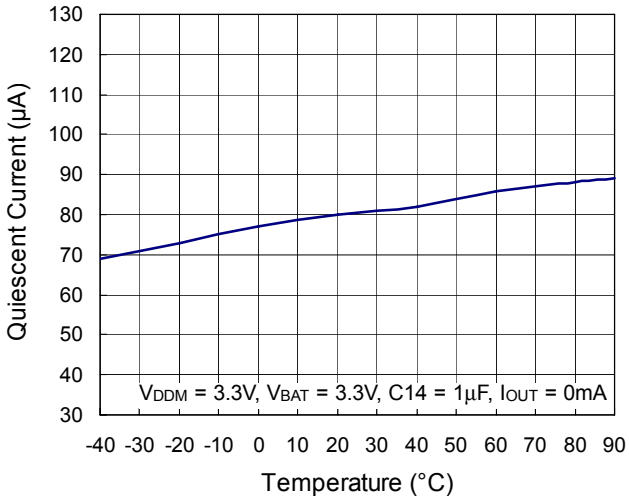
CH5 LDO Output Voltage vs. Temperature



CH5 LDO PSRR



CH5 LDO I_{PVDD5} Quiescent Current vs. Temperature



Application information

The RT9953 includes the following four DC/DC converters and one LDO to build a multiple-output power-supply system.

CH1 : Synchronous Step-Up DC/DC Converter

The CH1 is a synchronous step-up converter for motor or DSC system I/O power. The converter operates at fixed frequency and PWM Current Mode. The CH1 converter integrated internal MOSFETs, compensation network and synchronous rectifier for up to 95% efficiency.

The output voltage can be set by the following equation :

$V_{OUT\_CH1} = (1+R1/R2) \times V_{FB1}$

Where V^{FB1} is 0.8V typically.

CH2 : Synchronous Step-Up or Step-Down Selectable DC/DC Converter

The CH2 is a synchronous step-up/step-down selectable converter for motor or DSC system I/O power.

Mode setting

The CH2 of RT9953 features flexible Step-up or Step-down topology setting for either 1 x Li-ion or 2 x AA application by SEL pin. Please refer to "Electrical Characteristics" for level of Logic-High or Logic-Low. When the CH2 operates as a Step-up converter, the SEL must be set at Logic-High. If the CH2 operates at Step-down mode, the SEL must be set at Logic-Low. In addition, please note that the logic state can not be changed during operation.

Table 2. CH2 Mode Setting

SEL	CH2 Operating Mode
Logic-High	Step-Up
Logic-Low	Step-Down

Step-Up :

The converter operates at fixed frequency PWM Mode, continuous current mode (CCM), and discontinuous current mode (DCM) with internal MOSFETs, compensation network and synchronous rectifier for up to 95% efficiency.

Step-Down :

The converter operates at fixed frequency PWM mode and continuous current mode (CCM) with internal MOSFETs, compensation network and synchronous rectifier for up to 95% efficiency. The CH2 Step-down converter can be operating at 100% maximum duty cycle to extend the input operating voltage range. While the input voltage is close to the output voltage, the converter enters low dropout mode.

The output voltage can be set by the following equation :

$V_{OUT\_CH2} = (1+R3/R4) \times V_{FB2}$

Where V_{FB2} is 0.8V typically.

CH3 and CH4 : Synchronous Step-Down DC/DC Converter

The converter operates at fixed frequency PWM mode, CCM and integrated internal MOSFETs and compensation network. The CH3 and CH4 Step-down converter can be operating at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter could enter low dropout mode with low output ripple.

The output voltage can be set by the following equation :

$V_{OUT\_CH3} = (1+R5/R6) \times V_{FB3}$

$V_{OUT\_CH4} = (1+R7/R8) \times V_{FB4}$

Where V_{FB3} and V_{FB4} is 0.8V typically.

CH5 : 500mA Low Dropout, Low Noise Linear Regulator

Like any low-dropout regulator, this CH requires input and output decoupling capacitors. The CH5 linear regulator can support 500mA output current when PVDD5 > 2.7V. The typical current limit is 0.8A. If the output is shorted to ground, the Under Voltage Protection function will be triggered to shutdown the IC to prevent the part from damaging.

The output voltage can be set by the following equation :

$V_{OUT\_CH5} = (1+R9/R10) \times V_{FB5}$

Where V_{FB5} is 0.8V typically.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9953, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-24L 4x4 package, the thermal resistance θ_{JA} is 54°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (54°C/W) = 1.852W for WQFN-24L 4x4

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9953 package, the Figure 1 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

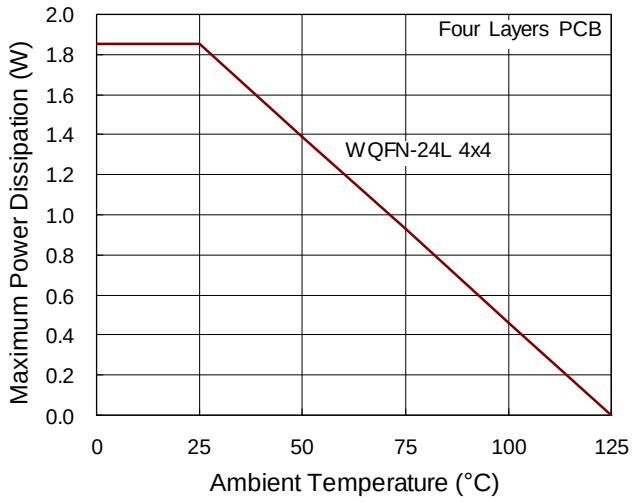


Figure 1. Derating Curves for RT9953 Package

Layout Considerations

For the best performance of the RT9953, the following PCB layout guidelines must be strictly followed :

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Place the feedback components as close as possible to the FB pin and keep these components away from the noisy devices.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- CH5 PCB trace and component had put different PCB side to avoid LX3 and LX4 switching noise.

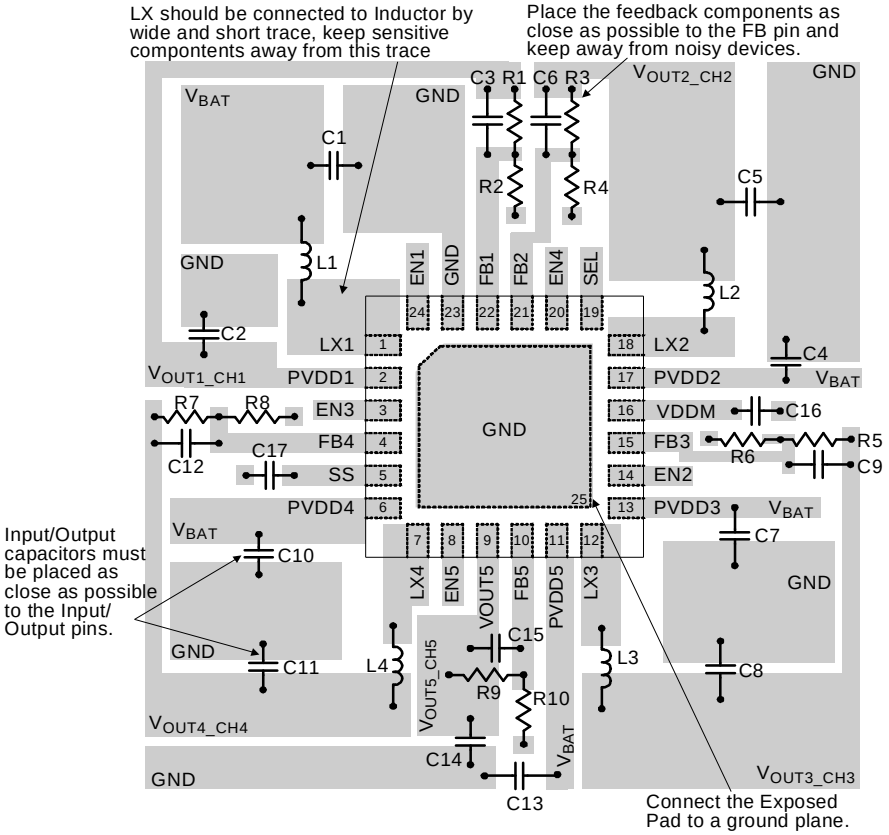
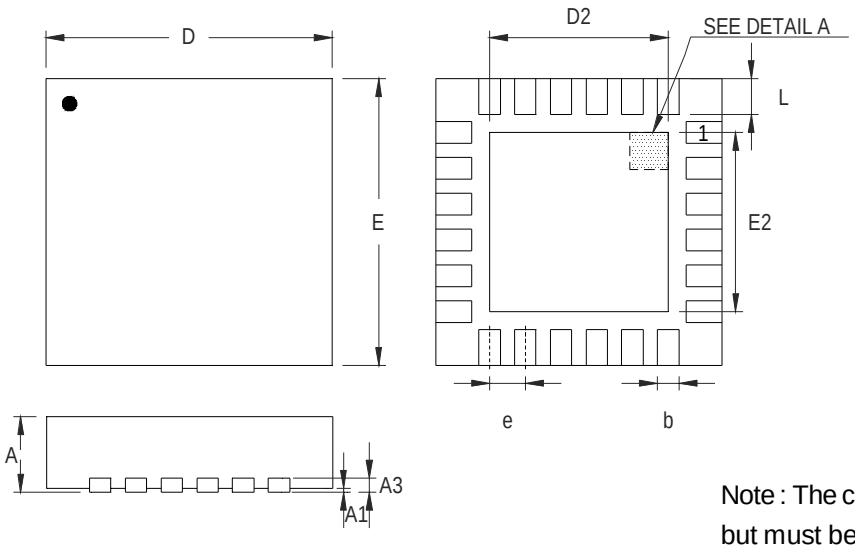


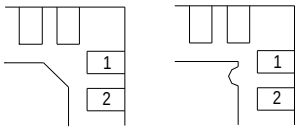
Figure 2. PCB Layout Guide

Table 3. Protection Items

	Protection type	Threshold (typical) Refer to Electrical spec	Protection methods	Delay time	Reset method
V_{DDM}	Over Voltage Protection	V_{DDM} > 6V	Disable all channels	100ms	Restart if V_{DDM} < 5.5V (with hysteresis)
CH1 Step-Up	Current Limit	N-MOSFET current > 3A	IC shutdown	100ms	V_{DDM} power reset
	PVDD1 OVP	PVDD1 > 6V	IC shutdown	No-delay	V_{DDM} power reset
CH2 Step-Up	Current Limit	N-MOSFET current > 3A	IC shutdown	100ms	V_{DDM} power reset
	PVDD2 OVP	PVDD2 > 6V	IC shutdown	No-delay	V_{DDM} power reset
CH2 Step-Down	OCP	P-MOSFET current > 1.5A	IC shutdown	100ms	V_{DDM} power reset
	UVP	FB2 < 0.4V	IC shutdown	100ms	V_{DDM} power reset
CH3 Step-Down	OCP	P-MOSFET current > 1.5A	IC shutdown	100ms	V_{DDM} power reset
	UVP	FB3 < 0.4V	IC shutdown	100ms	V_{DDM} power reset
CH4 Step-Down	OCP	P-MOSFET current > 1.5A	IC shutdown	100ms	V_{DDM} power reset
	UVP	FB4 < 0.4V	IC shutdown	100ms	V_{DDM} power reset
CH5 LDO	Current Limit	I_{OUT} (P-MOSFET current) > 0.8A	Current Limiting	No-delay	No reset
	UVP	FB5 < 0.4V	IC shutdown	100ms	V_{DDM} power reset
Thermal	Thermal shutdown	Temperature > 160°C	All channels stop switching	100ms	Temperature < 140°C

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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